5. Operating and Storage Junction Temperature Range, T$_J$

The operating and storage junction temperature, T$_J$ indicates the recommended temperature range in which a MOSFET operates reliably under specified electrical values. Most of standard MOSFETs have –55°C to +150°C temperature range like Table 5.

Table 5. OPERATING AND STORAGE JUNCTION TEMPERATURE PARAMETERS

Symbol	Parameter	Ratings	Unit
TJ			

**Figure 6. Maximum Continuous Drain Current
vs. Case Temperature**

Another constraint is caused by the current capability of a package. The I_D of FDMS86101A at the 25°C case temperature is limited by 60 A in Figure 6 due to its package current capability. Table 8 describes the maximum continuous drain current based on each condition.

Table 8. CONTINUOUS DRAIN CURRENT PARAMETERS

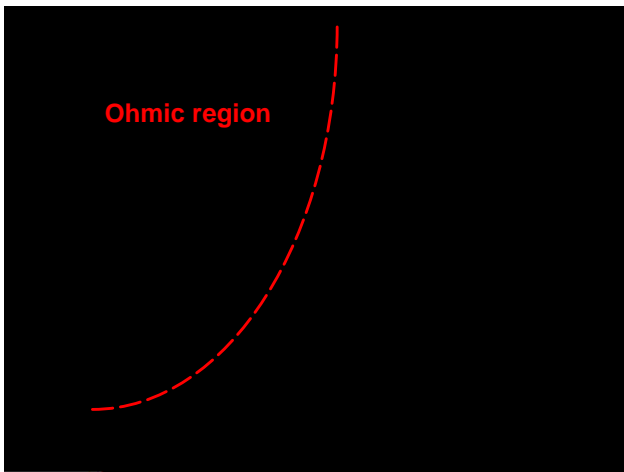| Symbol	Parameter	Ratings	Unit
I_D	Continuous Drain Current, $T_C = 25°C$	60	A
	Continuous Drain Current, $T_A = 25°C$ (Figure 5a)	13	A

Figure 8. On Region Characteristics

Figure 9 expresses the I_D as the function of the V_{GS} at given T_J and 5 V of V_{DS}. There is the crossover point among the transconductance curves at each junction temperature, which is called the Zero Temperature Coefficient, ZTC. If V_{GS} is above the ZTC point, a MOSFET has a negative temperature coefficient. It means if some cells within a MOSFET are getting hotter than others, hotter cells have a higher $R_{DS(on)}$ and their channels conduct less current, resulting in stabilizing the heat across unit cells. However, interestingly, a MOSFET has the positive temperature coefficient when operating with V_{GS} below the ZTC point. The gate threshold voltage, $V_{GS(th)}$, is reduced with the increase of junction temperature, T_J, and much more drain

For example, when FDMS86101A is conducting during 1 ms out of the 2 ms period which is the 0.5 duty cycle, the r(t) from Figure 10 is 0.5. The junction−to−ambient thermal resistance, $R_{\theta JA}$ on the minimum pad of 2 oz copper is 125°C/W from Table 6. Then the $Z_{\theta JA}(t)$ of FDMS86101A mounted on the minimum pad of 2 oz copper is 62.5°C/W by using Equation (6).

$$Z_{\theta JA}(t) = R_{\theta JA} \times r(t) = 125°C/W \times 0.5 = 65°C/W$$

So the junction temperature of FDMS86101A at $T_A = 25°C$ can be computed using Equation (7).

$$T_J = P_D \times Z_{\theta JA}(t) + T_A = 1\,W \times 62.5°C/W + 25°C = 87.5°C$$

Figure 11 provides the single−pulse maximum power dissipation as a function of the single pulse width at $T_A = 25°C$ and on the minimum pad of 2 oz copper PCB. The single−pulse maximum power dissipation can be calculated by using $Z_{\theta JA}(t)$. For instance, $Z_{\theta JA}(t)$ during the 10 ms single pulse is 1.25°C/W (125°C/W × 0.01) at $T_A = 25°C$ if the FDMS86101A is mounted on the minimum pad of 2 oz copper PCB. The single−pulse maximum power dissipation during 10 ms at $T_A = 25°C$ is 100 W.

$$P_D = \frac{T_J - T_A}{Z_{\theta JA}(t)} = \frac{150°C - 25°C}{1.25°C/W} = 100\,W$$
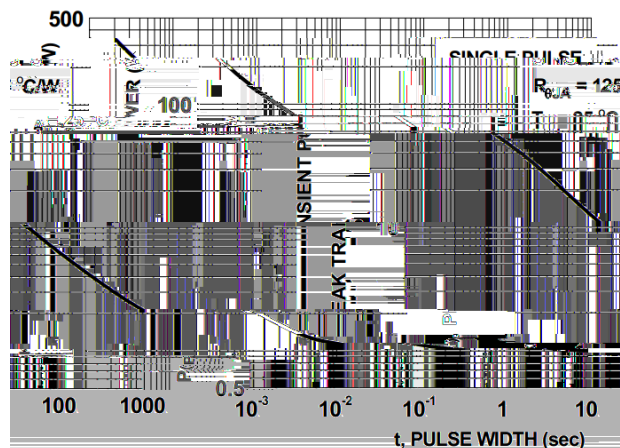

Figure 11. Single Pulse Maximum Power Dissipation

11. Single Pulse Avalanche Energy, E_{AS}

When the drain−to−source voltage, V_{DS}, exceeds the specified drain−to−source breakdown voltage, BV_{DSS}, at the turn−off state; the MOSFET breaks down and conducts the avalanche current, I_{AS}, and goes into avalanche mode. The I_{AS} through the body of the MOSFET causes the high power dissipation that can be translated to the avalanche energy, E_{AS}, and it can destroy the device. Figure 12 is the unclamped inductive switching (UIS) test circuit to show how much I_{AS} a MOSFET withstands during avalanche time, t_{AV}. The Device Under Test (DUT) is connected with an inductor in series, which induces the voltage of the counter−electromotive force. When the MOSFET is turned on for t_P time, the drain current reaches the point of I_{AS} and

the energy is charged in the inductor. Right after the t_P, the MOSFET is quickly turned off and the inductor generates the voltage of the counter−electromotive force to increase the voltage of the drain terminal referenced to the ground (V_{DS}), which is clamped to BV_{DSS}.

The charged inductor energy starts being discharged through the device for the avalanche time, t_{AV}. Figure 13 shows the waveform of I_{AS} and V_{DS} in avalanche mode testing.
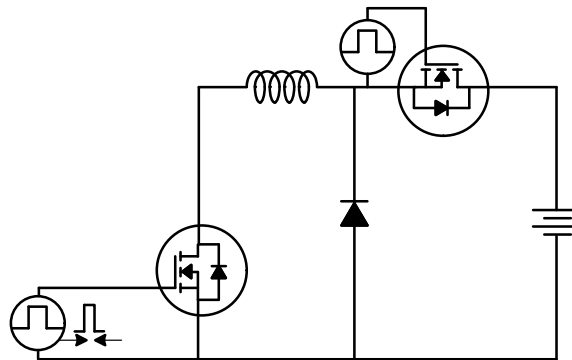

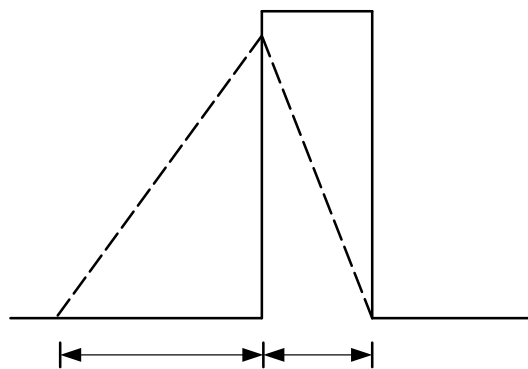**Figure 12. Unclamped Inductive Switching Test Circuit**

Figure 13. Unclamped Inductive Switching Waveforms

Figure 14 shows the relationship between t_{AV} and I_{AS} a MOSFET withstands at a given the junction temperature, T_J. There are a), b), c), and d) areas to determine whether or not the device is safe in the Unclamped Inductive Switching (UIS) mode.

a Under the boundary of various T_J, the MOSFET is within the UIS capability.

b Area between two boundaries of 125°C and 100°C of the T_J. If the starting point of the T_J is below 125°C before entering avalanche mode, the MOSFET is within the UIS capability.

c Area between two boundaries of 100°C and 25°C of the T_J. If the starting point of the T_J is below 100°C before entering avalanche mode, the MOSFET is within the UIS capability.
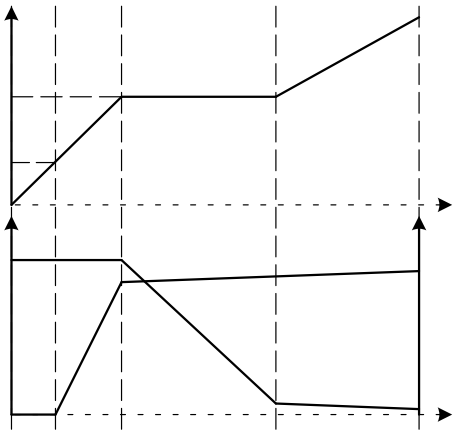
d The MOSFET is out of the UIS capability.

AN 4163/D
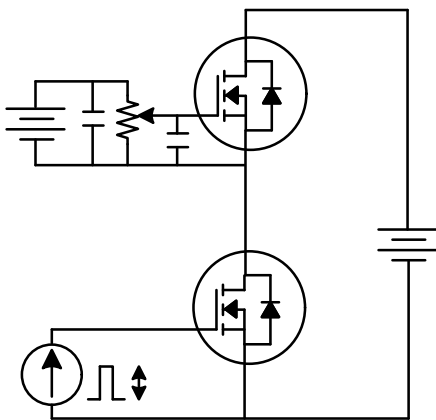
Figure 16. Gate Charge Waveforms

Figure 17. Gate Charge Test Circuit

The turn−on delay, $t_{d(on)}$, is defined as the time to charge the input capacitance, C_{iss}, before the I_D flows. The rise time, t_r, is the time to discharge output capacitance, C_{oss}, after the MOSFET conducts the I_D set by the resistor load, R_D. In the same way, the turn−off delay, $t_{d(off)}$, is the time to discharge C_{iss} after the MOSFET is turned off. The fall time, t_f, is the time to charge the output capacitance, C_{oss}, through the load resistor. Figure 19 and Figure 20 show the switching time test circuit and simple waveforms, respectively.
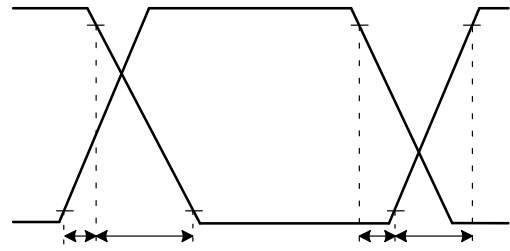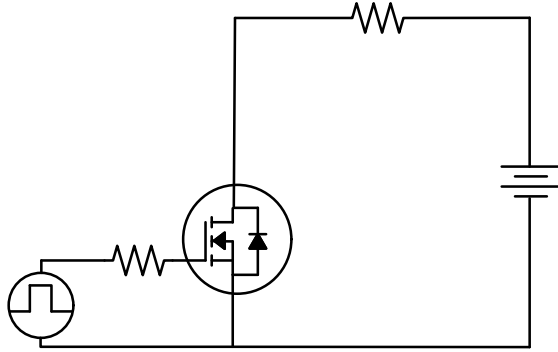

Figure 19. Switching Time Test Circuit

Figure 20. Switching Waveforms

15. Drain to Source Diode Characteristics

Like Table 14, the datasheet gives drain to source diode characteristics such as the source to drain diode forward voltage V_{SD}, the reverse recovery time t_{rr}, and the reverse recovery charge Q_{rr}.

Table 14. DRAIN TO SOURCE DIODE CHARACTERISTICS PARAMETER

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = 2.1$ A	0.74	1.20	V
		$V_{GS} = 0$ V, $I_S = 13$ A	0.81	1.30	
t_{rr}	Reverse Recovery Time	IF = 13 A, di/dt = 100 A/µs	64	102	ns
Q_{rr}	Reverse Recovery Charge		102	164	nC

The forward voltage of the intrinsic source−to−drain diode or the body diode is measured at the specific reverse drain current, I_S. Figure 21 shows the I_S as the function of body diode forward voltage, V_{SD}, at given junction temperatures, T_J. As the T_J increases, the V_{DS} is reduced at the fixed I_S due to its negative temperature coefficient.

When the body diode is reversely biased right after its forward conduction, it cannot regain the reverse blocking capability until minority charge carriers stored in the body diode are recombined. It results in the reverse−recovery current flow, I_{rr}, through the body diode. The amount of time it takes body diode to recover is the reverse−recovery time, t_{rr}. The reverse−
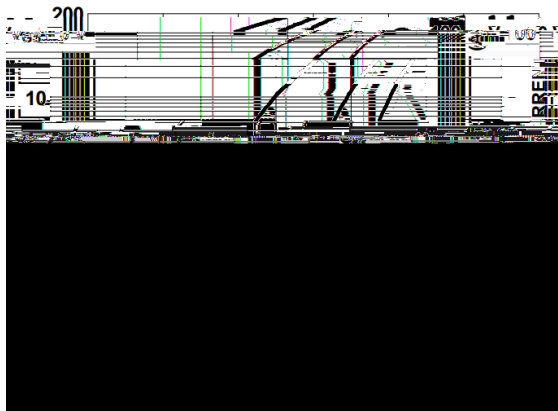

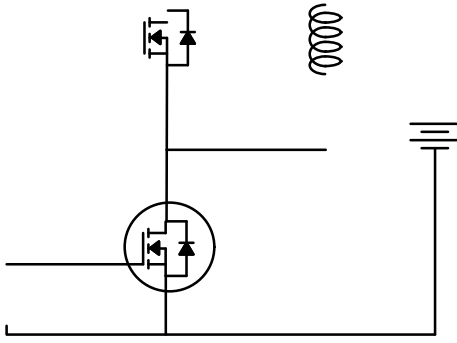**Figure 21. Source to Drain Diode Forward Voltage vs. Source Current**

Figure 22. Reverse Recovery Test Circuit

Figure 23. Reverse Recovery Test Waveforms