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FETS

Junction Field Effect Transistors (JFETs) There are two types of JFETs: an N channel type and a P channel

STRUCTURE OF A MOSFET

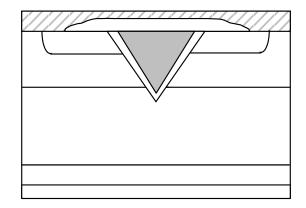
Lateral Channel Design

The drain, gate, and source terminals are placed on the surface of a silicon wafer. This is suitable for integration, but not for obtaining high power ratings because the distance between source and drain must be large to obtain better voltage blocking capability. The drain to source current is inversely proportional to the length.

Vertical Channel Design

The drain and source are placed on the opposite sides of a wafer. This is suitable for a power device, as more space can be used as source. As the length between the source and drain is reduced, it is possible to increase the drain to source current rating and increase the voltage blocking capability by growing the epitaxial layer (drain drift region).

- 1. The VMOSFET Design: the first to be commercialized, this design was has a V groove at the gate region, as shown in Figure 4 (a). Due to stability problems in manufacturing and a high electric field at the tip of the V groove, VMOSFETs were replaced by DMOSFETs.
- The DMOSFET Design: has a double diffusion structure with a P base region and a N⁺ source region, as shown in Figure 4 (b). It is the most commercially successful design.
- 3. The UMOSFET Design: As shown in Figure 4 (c), this design has a U groove at the gate region. Higher channel density reduces the on resistance as compared to the VMOSFETs and the DMOSFETs. UMOSFET designs with the trench etching process were commercialized in the 90's.



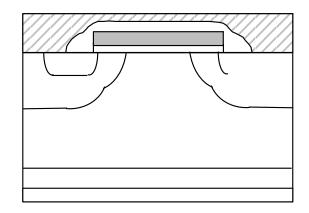


Figure 4. Vertical Channel Structure

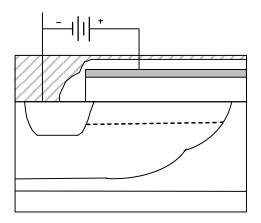
CHARACTERISTICS OF MOSFET IN ON AND OFF STATE

OFF State

 $\mathsf{BV}_{\mathsf{DSS}}$

ON State

Drain current (I_D) changes due to the increase in drain to source voltage (V_{DD}) (V_{GS} is constant). I_D starts to flow when the channel has formed and V_{DD} is supplied. When the V_{GS} is a constant value and the V_{DD} is increased, the I_D also increases linearly. As shown in the MOSFET output characteristics graph, when the real V_{DD} goes over a certain level, the rate of increase in I_D decreases slowly. Eventually, it becomes a constant value independent of V_{DD} and becomes dependent on V_{GS}.



 $Figure 9. Inversion Layer Thickness Changes due to \\ the Increase of the Drain-to-Source Voltage (V_{DD}) \\ where V_{DD1} < V_{GS} - V_{GS(th)}, V_{DD2} > V_{GS} - V_{GS(th)}, \\ I_{D2} (Saturation Current) > I_{D1}$

User's manual

Characteristics of Capacitance

The three types of parasitic capacitance are:

• Input capacitance: $C_{iss} = C_{gd}$

Cds: Capacitance between Drain and Source

The capacitance varies due to the variation of the C_{ds} thickness, which is the junction thickness of the P body and the N⁻ drift region, with the change of V_{DS}:

$$C_{ds (per unit area)} = \frac{\overline{q k_s \epsilon_o C_B}}{2 V_{DS} + \phi_B}$$

here

- q is elementary electronic charge; (= 1.9×10^{-19} [C]) k_s = silicon dielectric constant;
- $\begin{array}{l} \epsilon_{o} & \text{ is the permeability of free space} \\ (8.86 \times 10^{-14} \, [\text{F/cm}]); \end{array}$
- V_{DS} is drain to source voltage; and
- $\varphi_{\mathsf{B}} \quad \text{is diode potencial}.$

As shown in the equation above, $V_{DS} \gg \phi_B C_{ds}$ decreases as V_{DS} increases with the relationship of $C_{ds} \propto 1 - \overline{V_{DS}}$.

Characteristics of the Gate Charge

It is the amount of charge required during MOSFET turn on or turn off transient.

The types of charges are:

- Total Gate Charge: Qg (The amount of charge during $t_0 \sim t_4$)
- Gate Source Charge: Qgs (The amount of charge during $t_0 \sim t_2$)
- Gate Drain (Miller) Charge: Qgd (The amount of charge during t₂ ~ t₃)

Figure 12 shows the gate source voltage, gate source current, drain source voltage, and drain source current during turn on. They are divided into four sections to show the equivalent circuits at the diode clamped inductive load circuit.

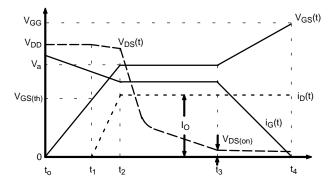


Figure 12. V_{GS}(t), I_G(t), V_{DS}(t), I_D(t) When Turned On

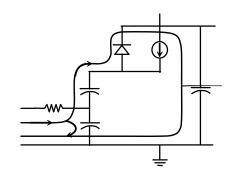


Figure 13. Equivalent Circuits of the MOSFET with Turn-on Divided into 4 Periods at the Diode-clamped Inductive Load Circuit

thickness of the gate oxide, and the gate drive voltage.

 R_A As the gate drive voltage is supplied, charges start to accumulate in N⁻ epi surface (the plate under C_{gd}) and forms a current path between the channel and the JFET region. The resistance of this accumulation region is R_A Temperature Characteristic

 g_{fs} decreases as the temperature increases due to the reduction of mobility. Equation 8 is similar to the $R_{DS(on)}$ and temperature relationship; it is possible to know the gfs changes by the changes in temperature:

$$g_{f_{5}}(T) = g_{f_{5}}(25^{\circ}C) \left(\frac{T}{300}\right)^{-2.3}$$
 (eq. 8)

where

T is absolute temperature.

Drain–Source Breakdown Voltage (BV_{DS} Breakdown Voltage Temperature Coefficient (Δ BV/ Δ TJ)

 $\mathsf{BV}_{\mathsf{DSS}}$ is the maximum drain to source voltage where the MOSFET can endure without the avalanche breakdown of the body

Power MOSFET Failure Characteristics during Inductive Turn-Off

It has the same electrical characteristics as the second breakdown of the bipolar transistor. It is independent from dv_{DS}/dt . By maintaining the gate turn off voltage constantly and changing the magnitude of the external gate resistance, the magnitude of the gate turn off current changes. This changes the dV_{DS}/dt . If dV_{DS}/dt current causes a device failure, the voltage that can lead to a second breakdown

the temperature rises, R_b is increased by the reduction of mobility. As the V_{be} decreases, the possibility of turn on of the parasitic transistor increases. As the base and the emitter are shorted by the source contact, the R_b value is very small. This occurs only if the dv/dt is enormously large.

In a false turn on, the dv/dt can be controlled externally. In a parasitic transistor's turn on, the dv/dt is determined by device design. This is the difference between these modes.

Dynamic dv/dt

If there is a sudden current interruption, such as a clamped inductive turn off in high speed switching, the device is destroyed by concurrent stresses caused by high drain current, high drain source voltage, and displacement current at the parasitic capacitance.

Diode Recovery dv/dt

This is the main cause of dv/dt failure in specific applications, such as circuits using a body drain diode. The datasheet gives the maximum value for dv/dt. Exceeding this value causes device failure due to excessive diode recovery dv/dt. Figure 22 shows a motor control circuit application with a diode recovery dv/dt problem.

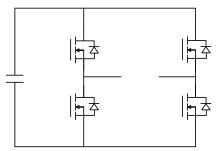


Figure 22. Motor Control Circuit

- Case Temperature (T_C): Temperature at a point of the package that has the semiconductor chip inside.
- Heat Sink Temperature (T_S)
- Ambient Temperature (T_A): Temperature of the surrounding environment of the operating device.
- Junction to Case Thermal Resistance ($R_{\theta JC}$)
- Case to Sink Thermal Resistance (R $_{\theta CS}$)
- Sink to Ambient Thermal Resistance ($R_{\theta SA}$)

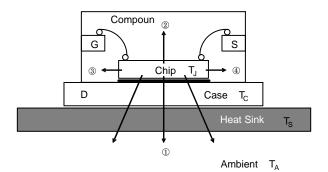


Figure 25. Thermal Discharge Path at Chip Junction

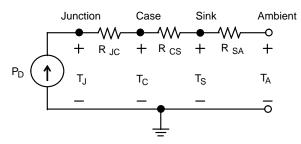


Figure 26. Circuit Based on Thermal Resistance

As shown in Figure 25, the heat produced at the chip junction normally discharges over 80% in the direction of

and about 20% in the direction of . The path of the thermal discharge is the same as the movement of the current and is represented in Figure 26 after considering thermal resistance. This is true only for DC operation. Most MOSFETs are used in switching operations with a fixed duty factor. Thermal capacitance should be taken into consideration, along with thermal resistance. The thermal resistance from the chip junction to the ambient is $R_{\theta JA}$

(junction to ambient thermal resistance(0 0 0 m2.1398 0 TD1/TT6 1 Tf.08 0 T6h5Tj/TT66.5 138.2173 423.8362 Tm()Tj/TT10 1 Tf.4797 -026

A single pulse curve determines the thermal resistance for repetitive power pulses having a constant duty factor (D), as shown in Equation 15.

$$R_{\theta JC}(t) = R_{\theta JC} \cdot D + (1 - D) \cdot S_{\theta JC}(t) \quad (eq. 15)$$

where

- $Z_{\theta,JC}(t)$ is the thermal impedance for repetitive power pulses with a duty factor of D;
- $S_{\theta JC}(t)$ is the thermal impedance for a single pulse;
- I_D is continuous drain current; and
- I_{DM} is drain current, pulsed.

As shown in Equation 16, the I_D rating is determined by the heat removal ability of the device. Figure 10 in the datasheet, maximum drain current vs. case temperature, shows increasing permissible I_D as T_C decreases.

$$I_{D}(T_{C}) = \frac{\overline{T_{Jmax} - T_{C}}}{R_{DS(on)} (T_{Jmax}) \cdot R_{\theta JC}}$$
 (eq. 16)

where

- R_{DS(on)}(T_Jmax) is the maximum value of on resistance in an appropriate drain current
 - condition $(\frac{1}{2} \cdot I_D \text{ in datasheet})$ at $T_{Jmax.}$ as maximum $R_{DS(on)}$ specified is at $T_C = 25^{\circ}C$.
- R_{DS(on)} (T_{Jmax}) could be analogized by the graph of on resistance vs. temperature;
- $\mathsf{R}_{\theta JC}$ is maximum junction to case thermal resistance; and

T_C is case temperature.

In real device applications where it is not feasible to maintain the temperature at $T_C = 25^{\circ}C$, the I_D (60 ~ 70% of I_D at $T_C = 25^{\circ}C$) at $T_C = 100^{\circ}C$ is a more usable specification.

Drain Current - Pulsed (I_{DM})

The drain current over continuous drain current rating should not go over the maximum junction temperature. The maximum upper limit is I_{DM} . I_{DM} is about four times the value of I_D , as shown in Equation 17.

$$I_{DM} = I_D (T_C = 25[^{\circ}C]) \times 4$$
 (eq. 17)

Repetitive rating: Pulse width limited by maximum junction temperature.

Total Power Dissipation (P_D), Linear Derating Factor

$$P_{D}(T_{C}) = I_{D}^{2}(T_{C}) \cdot R_{DS(on)}(T_{Jmax}) = \frac{T_{Jmax} - T_{C}}{R_{\theta JC}}$$
(eq. 18)

Linear derating factor is calculated by:

(eq. 19)

Safe Operating Areas (SOA)

SOA (FBSOA)

It defines the maximum value of the drain source voltage and drain current that guarantees safe operation when the device is at the forward bias.

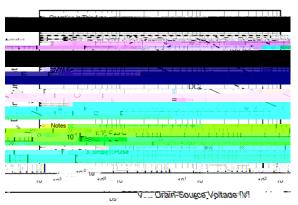


Figure 29. Maximum Safe Operating Area

Boundaries

Figure 29 shows the maximum safe operation area. In Figure 29, the right line: maximum drain source voltage rating.

The horizontal line: DC is the maximum rated continuous drain current at $T_C = 25^{\circ}$ C. For MOSFETs, excluding package limitations, maximum rated continuous drain current can be determined by the $R_{DS(on)}(T_{Jmax})$, as in Equation 20.

$$I_{D}(T_{C}) = \frac{\overline{T_{Jmax} - T_{C}}}{R_{DS(on)}(T_{Jmax}) \cdot R_{\theta JC}}$$
 (eq. 20)

Single pulse is the maximum rated drain current, pulsed:

$$I_{\rm DM} = I_{\rm D}(T_{\rm C}) \times 4 \tag{eq. 21}$$

The Upper Limit with Positive (+) Slope

The boundary where the power can be limited by the drain to source on resistance.

The Upper Limit with Negative (-) Slope

It is determined by the transient thermal impedance and the maximum junction temperature.

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