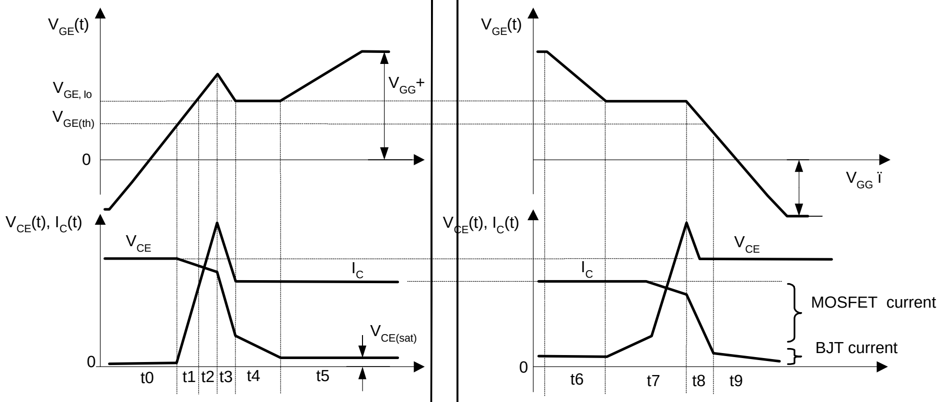
Analysis of Turn ïon Transient



(a) Turn ïon

(b) Turn ïoff

Figure 2. IGBT Switching Waveforms

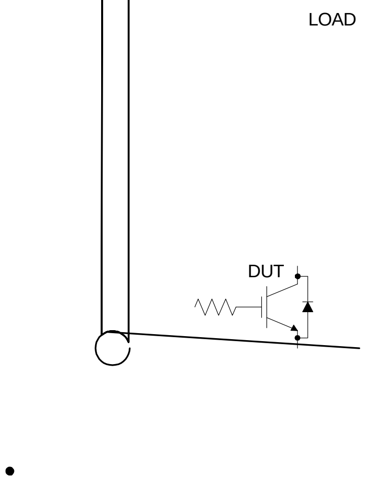


Figure 3. IGBT Switching Test Circuit

across the diode recovers and increases, while v_{CE} falls, and it falls rapidly as C_{gc} has small value when v_{CE} has high value. Due to this phenomenon, dv

Effect on State

For the same value of I_C, $V_{CE(sat)}$ is inversely related to the value of V_{GG+}. The smaller the V_{GG+}, the thinner the channel between n+ layer and ïdrift layer becomes, and the resistance in the channel increases. Due to the conductivity modulation effect not found in MOSFET, voïltage drop in the nï

(FWD) of the IGBT on the opposite side recovers reverse

When the maximum current is actually measured, one must be aware that it may be less than the calculated amount due to the falling voltage on the wire and stray inductance. When IGBTs are connected in parallel and are operated at a low frequency, low RMS current could lead to a mistaken complacency. However, under such situation, the maximum current would be twice as large, since there are 2 IGBTs in operation, and one must be careful that it could lead to the overload of the power supply of the gate drive. Wattage of the R_G can be decided with the maximum calculated amount of current.

Gate Drive Layout Considerations

Effect of Gate Line Inductance on the Induced Turnïon

Possibility of induced turnïon is greater, as the gate drive impedance is increased during turnïon and turnïoff transient due to stray inductance from the line connected with the gate. As gate impedance becomes smaller, more current flows through R_G to reduce the charging current of C_{ge}, which causes the amount of increase in V_{GE} to reduce. In order to prevent this, leakage inductance from DC power supply must be minimized, and R_G should be kept at minimum.

Power Source Stabilizing Capacitor

During IGBT switching, current flows to the gate, and at that time, supply voltage of the gate circuit can oscillate. As a result, the gate drive loss can exceed the designed amount, or it could reduce the short circuit capability. In such case, it is advised to keep PCB pattern wide and flat and use enough capacitor for supply voltage stability.

Isolation Problem

In half bridge topology and similar systems, the upper IGBT gate drive circuits must be insulated from the bottom IGBT circuits. The control board and the gate drive must also be insulated because the upper IGBT emitter free floats as the IGBT switches. As the power DC voltage rises, the insulating voltage should also rise accordingly. In general, the insulating voltage should be at least twice the rated voltage for the IGBT. In addition, care has to be taken with the noise that comes about from insulating interface. Immunity to noise differs depending on the how and where the circuits lines are placed, so wiring and placement should be designed to minimize parasitic capacitance. Parasitic capacitance should be minimized to reduce dV/dt × C coupling noise between neighboring drive circuits. When using a common transformer to provide current to both the upper and the lower gate drive, the wire must be wound to minimize combined capacitance. In using optoïcoupler, the optoïcoupler must have insulating capacity with high common mode voltage and transient noise immunity. Upper and lower, or different types of gate leads of the gate drive must not be wound together.

Wiring Pattern

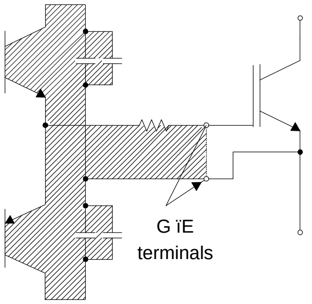


Figure 6. Gate Drive Pattern 6

The final pushïpull wiring pattern should be short and thick, and if a direct connection between the gate drive and the IGBT is not possible, then gate wire and the emitter wire could be twisted to reduce stray inductance. In addition, if the area of the loop that encompasses the final pushïpull stage, the power source pattern, R_G, and GïE terminals of the IGBT is minimized as shown in Figure 6, effect on the V_{GE}, from di_C/dt could be minimized when V_{GE+} is injected.

Common Emitter Problems

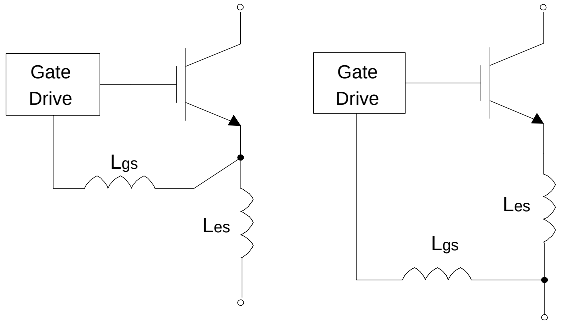


Figure 7. Common Emitter

At the time of switching, voltage is induced across the stray inductance of the power circuit because of di/dt from the main current. When control signals from the gate drive and the same path as the main current are used, gate voltage decreases during turnïon, and voltage is added to the gate voltage during turnïoff to slow the turnïon/turnïoff. As such, it is better not to share stray inductance between control emitter terminal and power emitter terminal. As such, control emitter terminal and power emitter terminal should be separate. If the two terminals are together, common emitter inductance increases to slow the switching speed and switching loss.

Voltage oscillation, slow gate voltage rise, noise immunity deterioration, gate voltage reduction, falling gate protection circuit efficiency are some of the effects of the layout. These can be solved with designs to reduce stray inductance and stray resistance such as making patterns short and thick. In addition, attention must be paid to the power circuit layout to minimize stray inductance. For example, the area of the closed loop must be minimized with DC link capacitor, load, power output, halfïbridge leg and snubbers in the case of inverter, and in the case of resistive load, line to the load should be twisted to reduce the stray inductance of the power circuit, while snubber should be strengthened depending on the amount of overïvoltage for inductive load. As the frequency increases, voltage could change due to slowing response of the dc link capacitor, so high ïspeed electrolyt cap for inverter should be used, and capacitor with better characteristics such as film capacitor should be inserted in the main cap in parallel.

Conclusion

We have examined some issues to consider in the gate

IGBT’s latch−up. It is possible to obtain short circuit time with short circuit testing of different products from many companies. In general, short circuit time becomes longer with high saturation voltage and $V_{CE(sat)}$. (In measuring $V_{CE(sat)}$, gate voltage should be enough for the minimum value of $V_{CE(sat)}$ and that level must be maintained during fault test.)

Types of Short Circuit

Short circuit can happen while IGBT’s normal function. Short circuit can be divided into two different types. The first is short−circuiting when the device was in on state, which is called “fault under load” and the second is a circumstance where the device turns on under short circuit, which is called “hard switch fault”.

Type I. Fault Under Load (FUL)

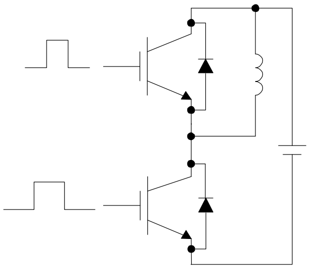


Figure 9. Fault Under Load Test Circuit

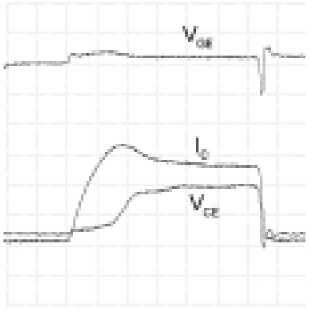


Figure 10. Fault Under Load Waveform

Fault under load (FUL) is a situation where short circuit takes place when the device is in on state, so the V_{CE} is low

Short Circuit Protection

We have discussed types of short circuits, and several ways to prevent short circuits have been reviewed. However, methods mentioned above are not fundamental ways to deal with short circuit, so there has to be a way to safely turn off the device when it short circuits.

Protecting Against Overïcurrent Condition

Overïcurrent is when more than the rated current flows through the system, and it can be classified into overïload, shortïcircuit, turnïon overïcurrent. In traditional applications, overïcurrent is possible in several cases. Generally, overïcurrent from overïload comes from inrush current, filter inrush and a rapid change in load during beginning of operation of electrical devices. In this case, we can only rely on short circuit capability of the device. Overïload, in general, lasts much longer than the IGBT’s short circuit endurance time. As such, other methods must be sought to remove the overload. Closed loop control moderates the timing signal of the gate drive pulse, to modifies the time of switching, and this is used to keep the current output at a determined level. Response control of the control loop would have to be set to the rate of changes in the current and pace of the electrical devices or filter inductance. Protection from overïcurrent due to shortïcircuit is different from turnïoff over current. In the following sections, protection from shortïcircuit would be discussed.

Protecting Against Short Circuit Current Condition

In the overload situations mentioned above, removing the closed loop does not considerably shorten the life of the IGBT. On the other hand, short circuit provides worse condition for the life of the device than overload or the overïcurrent at turnïon, and there are ground faults, terminalïtoïterminal faults. Such short circuit current bypasses the electrical devices or filter inductance and increases rapidly for IGBT to flow Conventional PWM loop controls power output, but it has no control over this type of fault. At the beginning of the fault, the IGBT must withstand with its own short circuit capability, and protection mechanism receives the fault signal to reduce the gate voltage while IGBT withstands the short circuit. However, if the fault disappears while during IGBT’s endurance time, then the IGBT must continue to function and must not turn off unnecessary devices or turn off the entire system. The most notable is the IGBT turnïon overïcurrent due to the reverse recovery current of the diode. As such, the protection circuit must be designed to return the circuit to normal operation if the fault is removed before the IGBT shuts down the system.

When conduction time increases, the border of SOA (SCSOA) decreases. Junction temperature increases

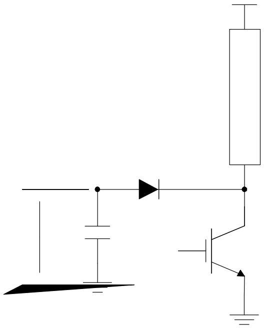


Figure 15. Short ïcircuit Sensing Circuit using De ïsaturation Method

Snubber Circuit

Types of Snubber Circuits and their Features

Snubber circuit is a supplementary circuit used in the converter circuit to reduce stress put on the power semiconductor. The ultimate goal of the snubber circuit is to improve the transient waveform. The snubber circuit suppresses overïcurrent or overïvoltage or improves dv/dt and di/dt to ease the transient waveform to reduce stress on the device. There are many uses for snubber circuits, but this discussion will center on its ability to suppress overïcurrent at turnïoff.

Snubber circuit can be divided into those connected in between the DC power supply bus and ground, and those connected to each IGBT. The first types of circuits include RC snubber circuits, charge and discharge RCD snubber circuits and dischargeïsuppressing RCD snubber circuits, and the second type includes C snubber circuits and RCD snubber circuits. The following are detailed descriptions of each snubber circuit.

RC Snubber Circuit

This snubber circuit is effective in turnïoff surge voltage and is suitable for chopper circuits. It is also effective for oscillation by parasitic reactance and dv/dt noise. However, when it is applied in large capacity IGBT, resistance for the snubber must be set low due to dissipation of heat, so it has the disadvantage of worsening loading conditions at turnïon. Loss at snubber itself is quite large, so it is not suitable for high frequency. In very large capacity IGBT circuit, it is better to use small snubber “RC snubber circuit” along with the main snubber “dischargeïsuppressing RCD snubber circuit.” When used together, it helps parasitic oscillation control of the main snubber loop. Main applications include arc welder and switching power supply.

Charge and Discharge RCD Snubber Circuit

This snubber suppresses overïvoltage at turnïoff to reduce switching losses at turnïoff, and its effectiveness in surge voltage suppression is about average. The snubber capacitor is completely discharged at turnïon, and it is fully recharged at turnïoff. Unlike the dischargeïsuppressing RCD snubber circuit below which acts as a clamp, this circuit of4e increases to present problems in controlling overïvoltage. In such large current applications, dischargeïsuppressing

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