ACTIVE CLAMP FORWARD TOPOLOGY

The active clamp forward (ACF) topology has multiple advantages compared to a traditional forward converter. The benefits of the active clamp topology can be easily maximized once the unique characteristics of this topology are fully understood. Figure 1 shows a simplified schematic of an active clamp forward topology. The transformer model (TX1) consists of an ideal transformer, magnetizing (L_{MAG}) and leakage (L_{LKG}) inductances.

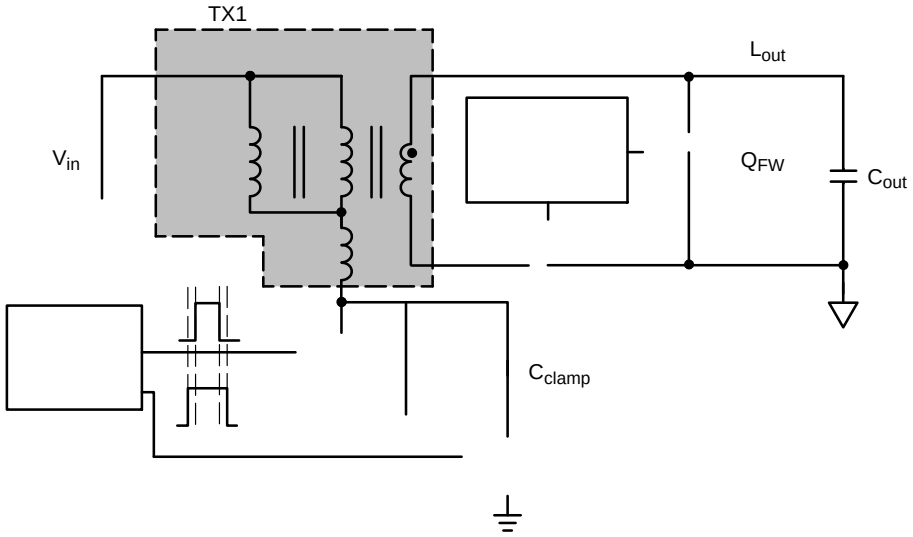


Figure 1. Active Clamp Forward Converter

$$V_{out} = \left(\frac{V_{in} - V_{DS(on)}}{N} - V_f\,(QREC)\right) \cdot D \quad \text{(eq. 2)}$$

where, N is the primary to secondary turns ratio, $V_{DS(on)}$ is the voltage drop across Q_{main}, $V_{(QREC)}$ is the voltage drop across Q_{REC}, D is the duty ratio and V_{in} is the input voltage. Equation 2) is used to select N given a target maximum duty ratio. An additional factor to consider in the selection of N is the drain voltage of the main switch (V_{DS}) during the off time as it depends on the duty ratio. Equation 3 shows the relationship between V_{DS} and D.

$$V_{DS} = \frac{V_{in}}{1 - D} \quad \text{(eq. 3)}$$

The NCP1562 Excel−based design tool (downloadable from http://www.onsemi.com). provides an easy way to evaluate the interaction between the turns ratio, duty ratio and maximum drain voltage as shown in Figure 4. The drain

$$I_{P(PK)} = \frac{I_{out} + \frac{I_{out(rip)}}{2}}{N} + \frac{V_{in} \cdot D}{L_{MAG} \cdot f_{SW}} \quad \text{(eq. 10)}$$

The main switch experiences conduction and switching losses. The conduction losses are given by Equation 11.

$$P_{con} = I_{P(rms)}^2 \cdot R_{DS(on)} \quad \text{(eq. 11)}$$

where, $R_{DS(on)}$ is the switch on resistance and $I_{P(rms)}$ is the primary rms current. The primary rms current is given by Equation 12.

$$I_{P(RMS)} = \sqrt{\left(I_{P(PK)}^2 + I_{P(PK)} \cdot I_{P(VL)} + I_{P(VL)}^2\right) \cdot \frac{D}{3}} \quad \text{(eq. 12)}$$

The turn on switching loss of the main switch is approximated by Equation 13.

$$P_{SW(Qmain)} = V_{DS} \cdot I_{P(VL)} \cdot t_{SW(on)} \cdot f$$

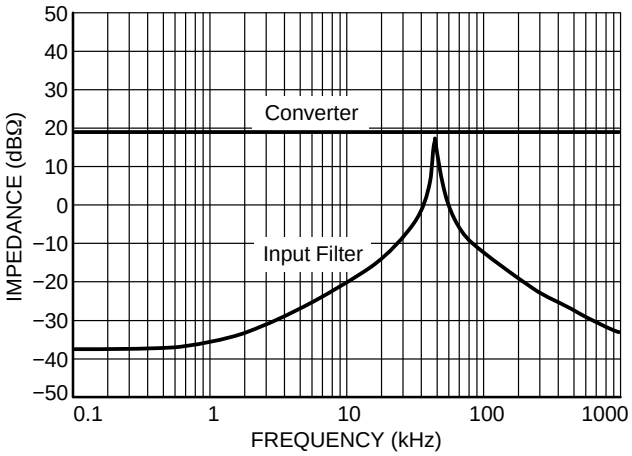


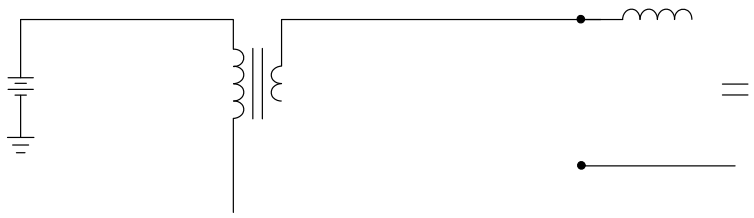
Figure 9. Input Filter Output Impedance and Approximated Converter Input Impedance

In general, if the system oscillates, the input filter output impedance can be decreased as in most cases the converter input impedance is dictated by the system specifications. This can be accomplished adding a damping network.

SYNCHRONOUS RECTIFICATION

Low output voltage converters require synchronous rectification to achieve high efficiency. If a diode is used for rectification, the forward voltage drop becomes a significant portion of the output voltage thus severely affecting the efficiency.

The active clamp topology lends itself for synchronous rectification as it has signals readily available that may be used for driving a synchronous rectifier. The synchronous rectifiers are driven from the main transformer output winding as shown in Figure 10. This configuration is known as self−driven synchronous rectification (SD−SR).



The converter high output current requires multiple MOSFETs to be used in parallel due to the high conduction losses. The number of MOSFETs for Q_{FW} and Q_{REC} is determined by calculating the losses of each one and dividing it by the maximum power dissipation given by Equation 14.

The maximum power dissipation of Q_{REC} occurs at low line and for Q_{FW} at high line. The conduction losses for Q_{REC} and Q_{FW} are given by equations 23 and 24, respectively.

$$P_{cond(REC)} = I_{out(rms)}^2 \cdot D \cdot R_{DS(on)} \quad \text{(eq. 23)}$$

$$P_{cond(FW)} = I_{out(rms)}^2 \cdot (1 - D) \cdot R_{DS(on)} \quad \text{(eq. 24)}$$

The gate charge losses of the driver and body diode conduction losses are given by 25 and 26, respectively.

$$P_{driver} = f_{SW} \cdot Q_{G(TOT)} \cdot V_{gate} \quad \text{(eq. 25)}$$

$$P_{bd} = V_{bd} \cdot I_{out} \cdot f_{SW} \cdot t_{dead} \quad \text{(eq. 26)}$$

Figure 12

FEEDBACK LOOP

The converter regulates the output voltage by adjusting the duty ratio using a negative feedback loop. If the loop is not stable, the converter will oscillate. To insure the loop is stable and has adequate transient response, the closed loop response should have a minimum phase margin of 45° under all line and load conditions. This is accomplished by shaping the open loop response using an error amplifier.

The first step is to determine the open loop frequency response of the converter. An active clamp forward converter operating in voltage mode has two poles, $p_{1,2(LC)}$, due to the output LC filter and one zero, z_{ESR}, due to the output capacitor series resistance. In addition it has two complex zeros introduced by the active clamp network. The complex zeros are not shown due to their great complexity. The complex zeros happen before the system poles $P_{1,2(AC)}$. The system crossover frequency should be selected below $P_{1,2(AC)}$ to avoid the complex poles. Equations 28 through 30 show the system poles and zeros.

$$P_{1,\,2(LC)}$$

The system open loop gain in Figure 14 Simulated Open Loop Frequency Response at the desired crossover frequency of 15 kHz is 5 dB. Therefore, the EA gain is set at −8.77 dB to achieve a gain of 0 dB at approximately 15 kHz. Resistors R20 and R21 are set at 5.9 kΩ and 16.2 kΩ, respectively. One compensation zero is placed before and one after $p_{1,2(LC)}$ at 482 Hz and 9.8 kHz, respectively. Capacitors C25 and C29 are set at 0.056 F and 1000 pF, respectively. The second pole is set at a 457 kHz setting R30 at 348 Ω. The simulated frequency response is shown in Figure 16. The simulated crossover frequency is around 15 kHz with a 60° phase margin.

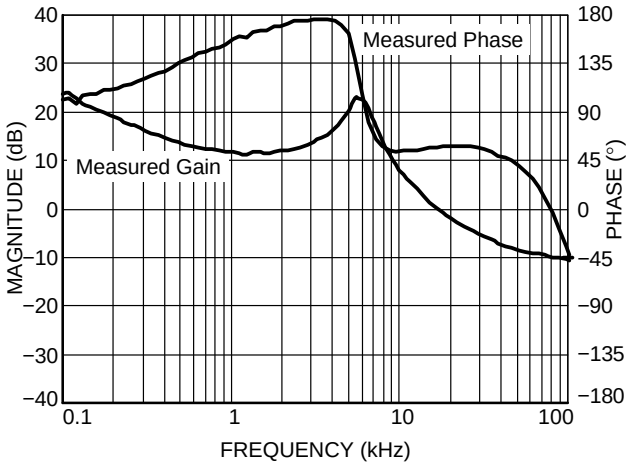
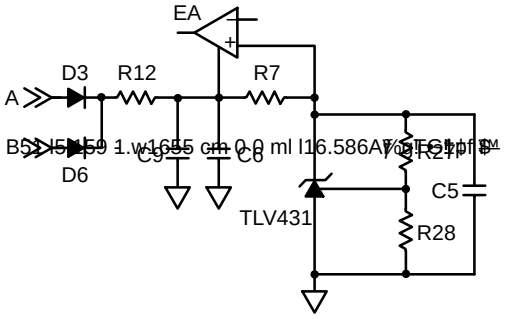


Figure 16. Simulated System Frequency Response

ERROR AMPLIFIER VOLTAGE REFERENCE

The error amplifier reference voltage ($V_{ref(EA)}$) is generated using On Semiconductor's TLV431 as shown in Figure 17.



is set at 100 Ω and C11 is set at 100 pF. The complete current sense circuit is shown in Figure 18.

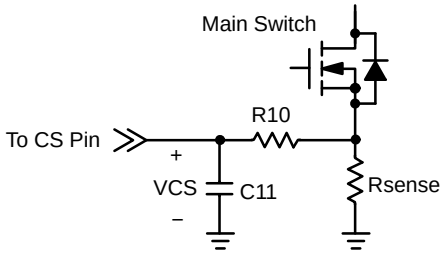


Figure 18. Current Sense Circuit

The converter enters the cycle skip current mode if a continuous over current condition is exists. Once a current limit event is detected, a 90 A current source begins charging the capacitor on the CSKIP pin. If the capacitor charges to 3 V, the converter enters a soft stop mode. A cycle skip period of 330 s is set with a 0.01 F capacitor.

Our transformer has a $V-sec_{(max)}$ of 62.4 V− sec. Selecting an arbitrarily I_{FF} of 1.75 mA, the Design Tool suggest values of 43.4 kΩ and 479 pF for R_{FF} and C_{FF}, respectively. Final values are 45.3 kΩ for R_{FF} and 470 pF for C_{FF}. As duty ratio control is very important, the tolerances for R_{FF} and C_{FF} are set at 1% and 5%, respectively.

SOFT−START

Soft−start slowly starts the converter and reduces stress during power up. The NCP1562 implements soft−start by comparing the voltage in the SS pin to the FF Ramp.

Soft−start is adjusted by placing an external capacitor, C_{SS}, between the SS pin and ground. The capacitor is charged with a constant 10 μA current source. The peak

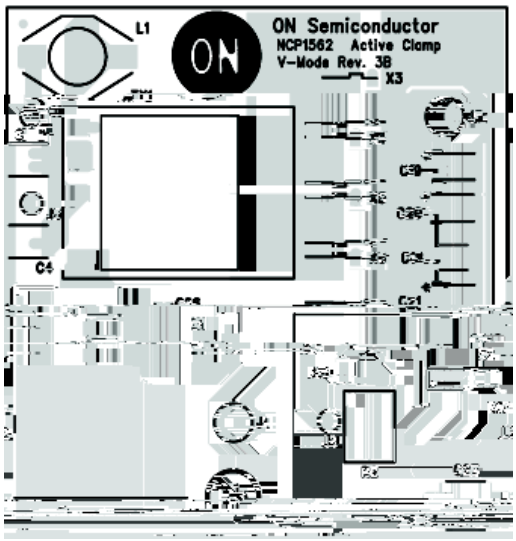


Figure 21. Layer 1 (Top)

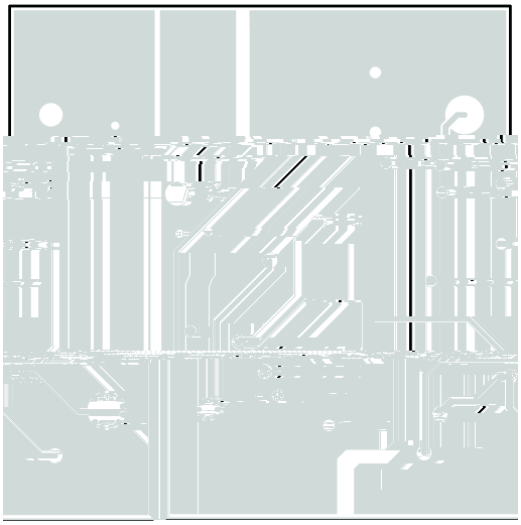


Figure 23. Inner Layer 3

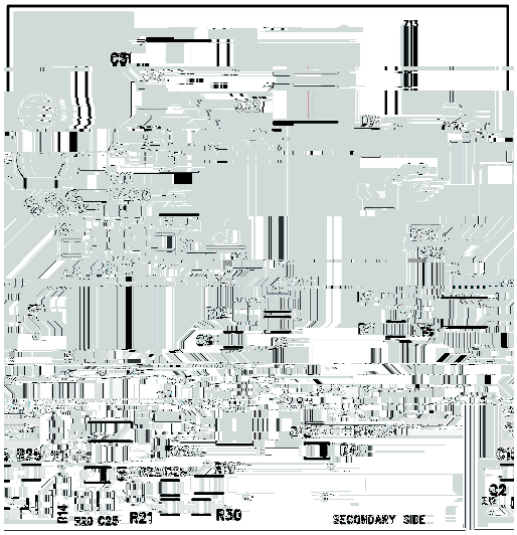


Figure 24. Layer 4 (Bottom)

Figure 22. Inner Layer 2

The layout files may be available. Please contact your sales representative for availability.

DESIGN VALIDATION

The top and bottom view of the board are shown in Figure 25 and Figure 26, respectively.

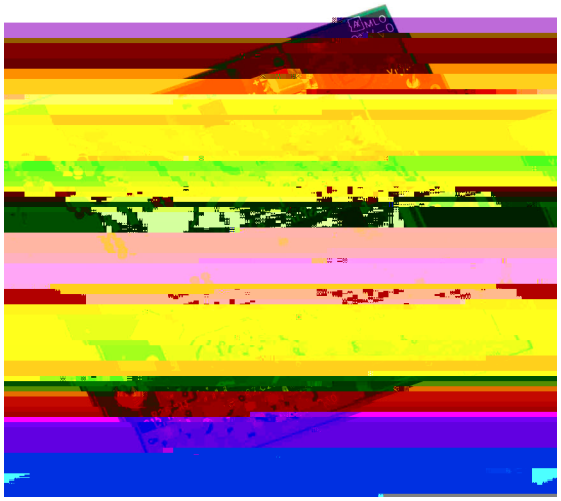
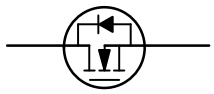
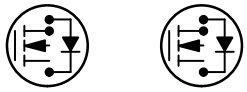


Figure 25. NCP1562 Demo Board Top View

Figure 26. NCP1562 Demo Board Bottom View

The circuit schematic is shown in Figure 27 and the bill of material is listed in Table 3.





Part	Vendor	Comments
C4532X7R2A225MT	TDK	100 V
VJ0805A102JXAAT	Vishay	50 V
VJ0805Y104KXAAT	Vishay	
C4532X5R1C226M	TDK	16 V
		25 V, 20%

If noc87.7795 650.9481 Tm[(V)22.1(ishad1 refr

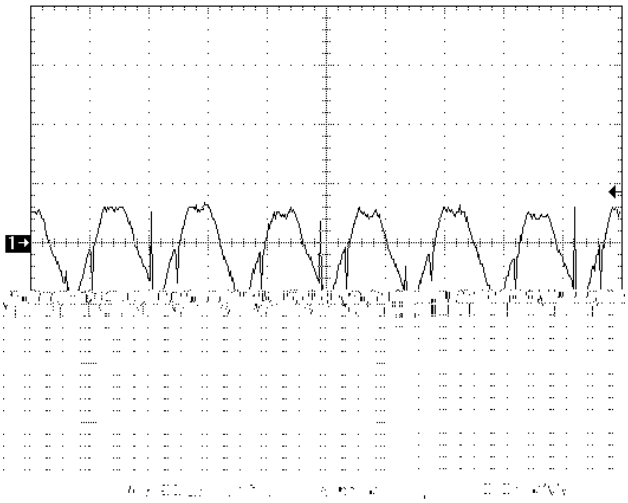


Figure 32. Output Voltage Ripple at High Line and Full Load

THERMAL PERFORMANCE

This demo board is designed to operate with airflow as in a telecom system. Airflow is required if the converter operates above 50% of its rated power. Optimum cooling is achieved when air flows from the output side to the input side.

The thermal performance of the board is evaluated using an infrared camera. Figure 33 through Figure 36 show several images of the board at full load. Images include top and bottom layers at low and high line. All images were taken with airflow from the output side to the input side.

Figure 33. Thermal Image of the Top of the Board at Low Line and Full Load Condition

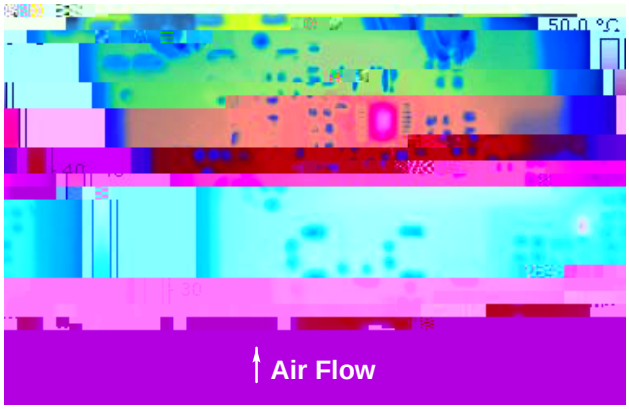


Figure 34. Thermal Image of the Bottom of the Board at Low Line and Full Load Condition

Figure 35. Thermal Image of the Top of the Board at High Line and Full Load Condition

Figure 36. Thermal Image of the Bottom of the Board at High Line and Full Load Condition

Most of the losses on the board are on the main switch and synchronous rectifiers. The synchronous rectifier losses are dominated by conduction losses. At low line, Q_{FW} has the higher duty ratio and thus the higher power dissipation as shown in Figure 33. At high line, Q_{REC} has the higher duty ratio and thus the higher power dissipation as shown in Figure 35.

The NCP1562 demo board thermal performance can be