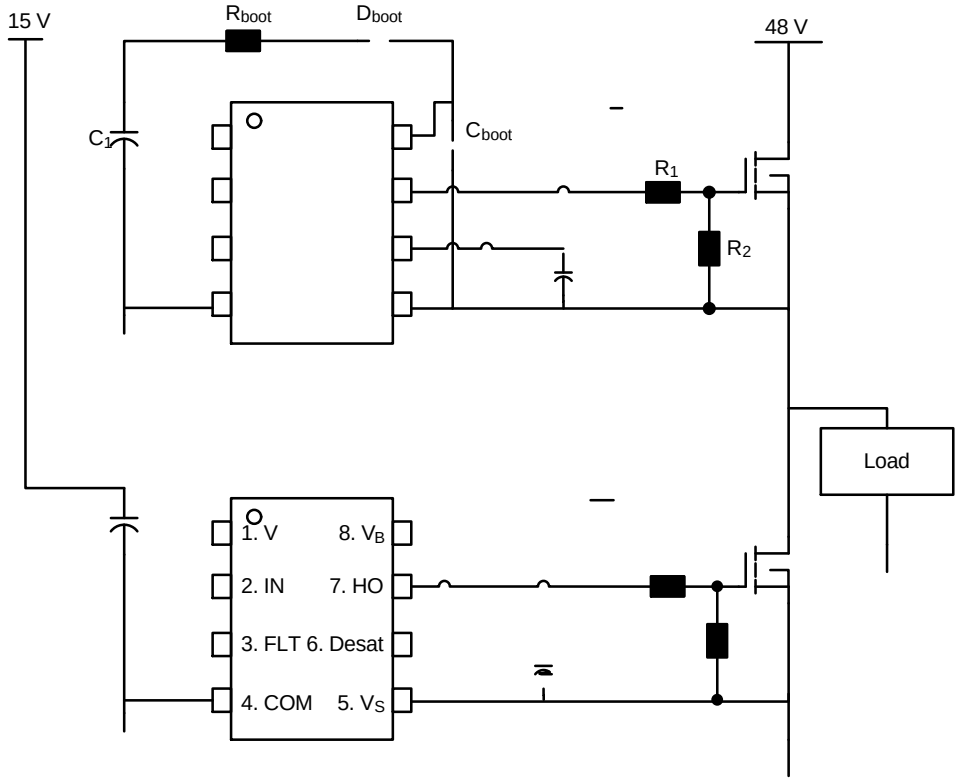

15 V
Rboot
Dboot
48 V
C1
Cboot
R1
R2
Load
1. V
8. VB
2. IN
7. HO
3. FLT
6. Desat
4. COM
5. VS

PIN FUNCTION DESCRIPTION

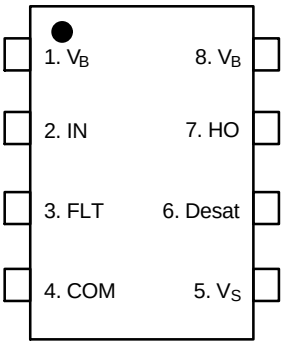


Figure 4. Pin Connection (Top View)

PIN DESCRIPTION

Pin No.	Symbol	Description
1	V_{DD}	Power supply for logic stage
2	IN	Input command
3	FLT	Bi−directional Fault pin
4	COM	Ground for logic stage
5	V_S	Floating source connection
6	Desat	Drain to Source Desaturation detection pin
7	HO	Output
8	V_B	Floating Power Supply for power stage

APPLICATION EXAMPLES

Gate Driver for 48 V DC−DC Converter Battery Switch

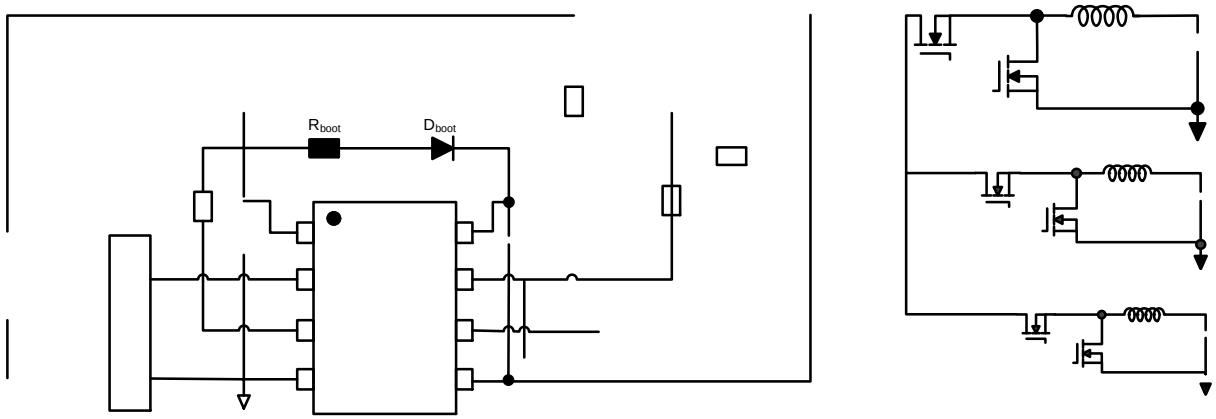
The simplified block diagram in Figure 5 shows how the FAD3171 can be used to drive a MOSFET as a battery main switch in a 48 V DC−DC converter.

The initial turn−on of the MOSFET is done through the bootstrap capacitance, initially charged by the 15 V supply. The integrated charge pump in the FAD3171 does not have enough source current capability to assure a direct energy efficient turn on of a larger die size MOSFET.

Once the MOSFET is turned on with 100% duty cycle, the bootstrap capacitance cannot charge any more through the 15 V supply and gets depleted by the continuous current sink into the gate to source resistance R_2 and by the internal leakage current of the gate driver.

The charge pump integrated in the FAD3171 turns on as soon as the bootstrap voltage drops below the charge pump turn on threshold, typ. 10.8 V. The charge pump operates and supplies current until the bootstrap voltage reaches the upper charge pump turn off threshold voltage (typ. 11.2 V) or, in case current consumption is too high, the bootstrap voltage drops to the driver turn off level of typ. 7.5 V.

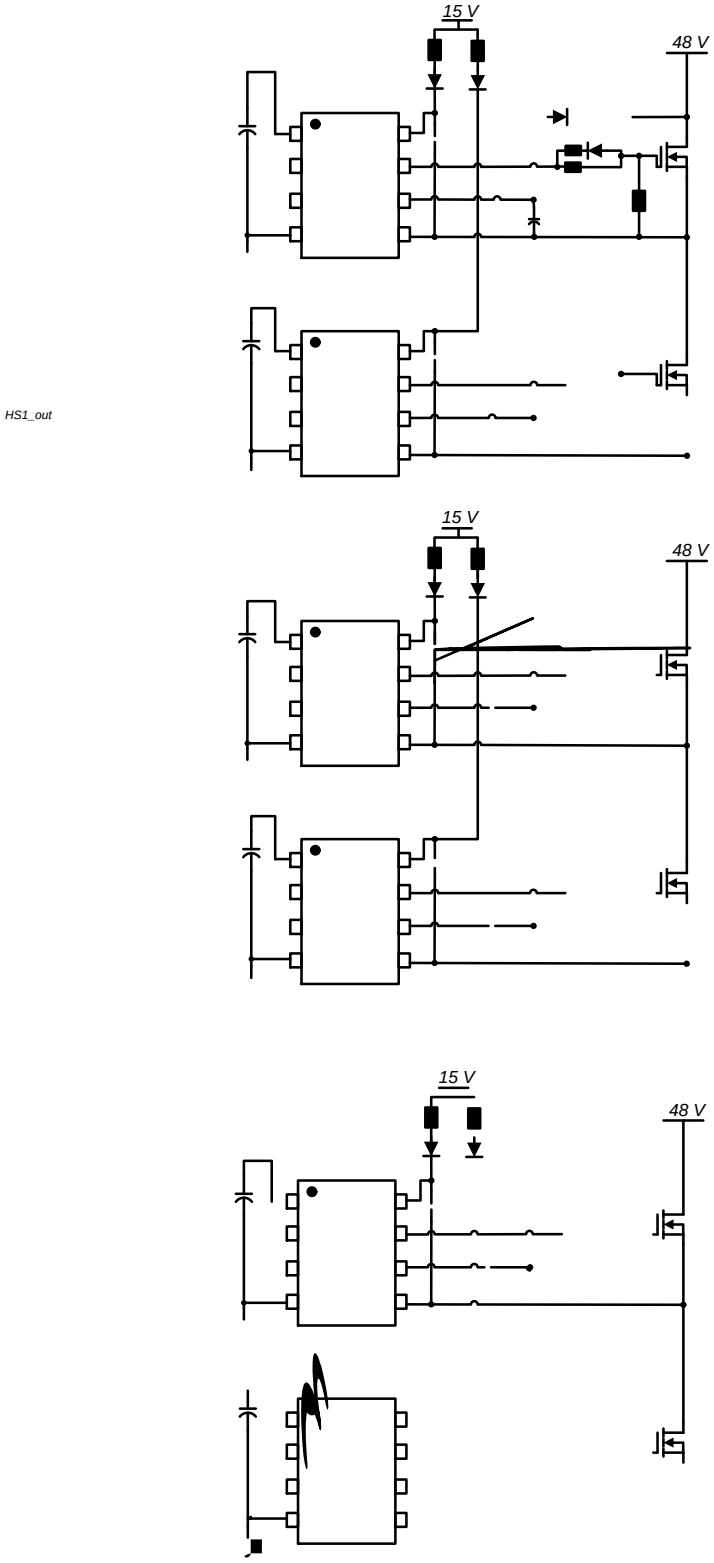
Note that to minimize the leakage current in the gate path, the resistance R_2 should not be too low. Considering the 200 μA current sourced by the charge pump at 9 V, excluding the desat current, the resistance R_2 should be greater than 47 kΩ to maintain 9 V on the gate of the MOSFET.



Example of a Fault Control Logic

The Fault control logic in Figure 8 to allow active discharge is explained below:

Figure 8. Example of Fault


15 V
48 V
HS1_out
15 V
48 V
15 V
48 V

Bootstrap Drive Circuit Operation

Both the FAD3151 and the FAD3171 normally use the bootstrap technique to achieve an elevated gate drive voltage in high side operation. This bootstrap power supply technique has the advantage of being simple and low cost. However, it has some limitations. On time of duty−cycle it is limited by the time required to refresh the charge in the bootstrap capacitor.

To overcome these limitations, the FAD3171MXA driver contains an internal charge pump that enables 100% duty cycle operation of high side power switches. When the high side switch is kept on for a long duration, the bootstrap capacitor could slowly discharge and may eventually trigger the undervoltage lockout protection and turn off the driver output. Therefore, the purpose of the charge pump is to supply the V_{BS} quiescent current necessary for the high side gate driver to operate under 100% duty cycle and to compensate for additional leakage current on the gate path.

It should be ensured that the total leakage current in the gate path does not exceed the maximum output current capability of the charge pump, $I_{CP,OUT}$.

It is important to note that the charge pump is not intended to provide gate charge during switching of a power MOSFET; rather its purpose is to only keep the MOSFET turned on. For this, it should be ensured at the system level that the high side MOSFET is not operated at very high duty cycle or, if a high duty cycle operation is required, the off time should be long enough to allow the bootstrap capacitor on high side gate driver to completely recharge. In order to minimize continuous power dissipation, the charge pump turns on only when needed, and remains off at other times.

For details on the bootstrap gate−drive circuit

iii. When P_1 turns off, the desat current flows into Cext and charges it until the voltage at the desat terminal rises to the desat threshold, Vdesat+. When Vdesat exceeds the internal Vdesat+, a fault status is triggered at the FLT pin of high side driver.

iv. The fault status is cleared when the self−check signal for high side driver is turned off.

- A malfunction of the high side desat protection circuit is detected:
  - if the high side gate driver is unable to trigger (set) a fault status on the FLT pin during self−check, or
  - if the gate driver is unable to clear this fault status at the end of self−check.
- During self−check mode of low side gate driver, the output of the high side gate driver should be turned off. The self−check sequence for low side desat protection circuit is as follows: (Please refer to the low side components in Figure 13 and the self−check sequence in Figure 14 for details.)

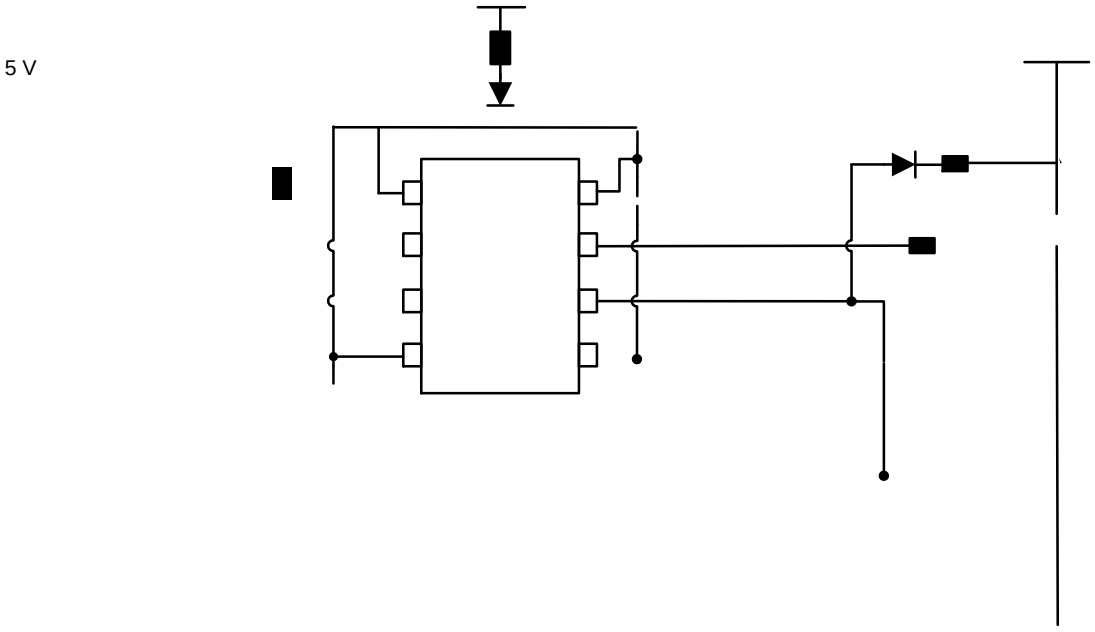
i. The microcontroller provides a low side self−check signal to turn on transistor N_2. At the same time, the output of the low side gate driver is turned on. As a result, P_1 turns off.

ii. When P_1 turns off, both the I_{CE} of N_2 and Idesat can charge Cext. In comparison to Idesat, the I_{CE} of N_2 could be significantly higher. Therefore, Cext is rapidly charged. When Vdesat is higher than Vdesat+, a fault status is triggered at the FLT pin of low side driver.

iii. The fault status is cleared when the self−check signal and the input signal for low side driver are turned off.

- A malfunction of the low side desat protection circuit is detected:
  - if the low side gate driver is unable to trigger (set) a fault status on the FLT pin during self−check, or
  - if the low side gate driver is unable to clear this fault status at the end of self−check.

NOTE: The desat self−check circuit shown for high side can also be adopted for low side. The low side desat self−check circuit shown in Figure 13 has fewer components than the self− check circuit on high side.



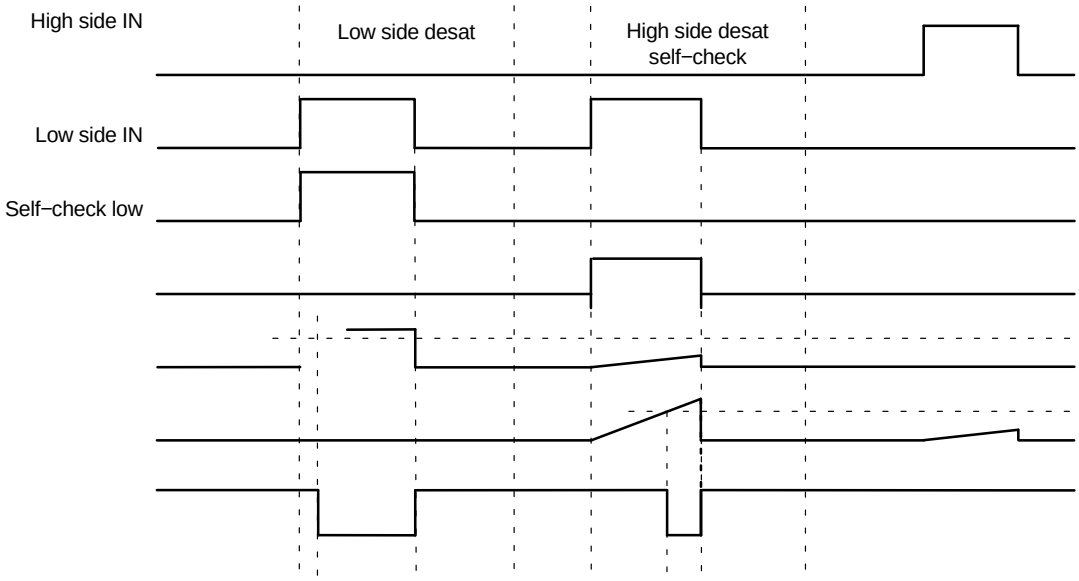


Figure 14. Self−check Sequence for High Side and Low Side Gate Driver

Table 2. FAILURE MODE ANALYSIS OF THE DESAT SELF−CHECK CIRCUIT FROM FIGURE 13

Component	Failure Mode	Effect and Diagnosis of Failure	Behavior
D_3	Open	• Does not allow P_1 to turn off during self− check; this can be detected during self− check as a fault status is triggered on the FLT pin.	Safe
	Short	No issues	Safe
P_3	Open	Does not allow P_1 to turn off during self− check; this can be detected as a fault status is triggered on the FLT pin.	Safe
	Short	• Pulls up the gate of P_1 consistently. • Causes an inadvertent triggering of the desat fault.	Safe
R_2	Open	• This can be detected during self−check. • The FLT pin is able to trigger a fault status but is unable to clear it.	Safe
	Short	• Pulls down the gate of P_1 to ground and does not allow P	