AND9764/D

NCV7685 I²C P a G d

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APPLICATION NOTE

INTRODUCTION AND DOCUMENT SCOPE

This document deals with the recommendation how to control the NCV7685 devices using I²C protocol and how to configure OTPs.

PREREQUISITES

The following guidelines are required:

- VDD supply has to be in range between 3.15 V to 5.5 V.
- Proper selection of the Pull−up resistors in respect with I²C speed, VDD supply voltage and bus capacitance.
- For Hard coding and OTP register access, the ISET pin has to be put to high.
- To Burn OTP, the VS supply has to be > 13 V.
- Every I²C message is protected by repeating address safety mechanism.
- Additional CRC may be activated based on the ERREN flag.

PULL UP RESISTOR SELECTION

Open drain I²C communication protocol needs pull−up resistors for communication. The pull−up resistors keep the I²C pins in high while there is no communication on the bus. The selection of the resistor value depends on bus capacitance, VDD supply, I²C speed and power consumption.

The equations for 400 kbps:

$$Rp(min) = \frac{VDD - 0.4}{0.003}\Omega \quad \text{(eq. 1)}$$

$$Rp(max) = \frac{300ns}{0.8473 \cdot C_B}\Omega \quad \text{(eq. 2)}$$

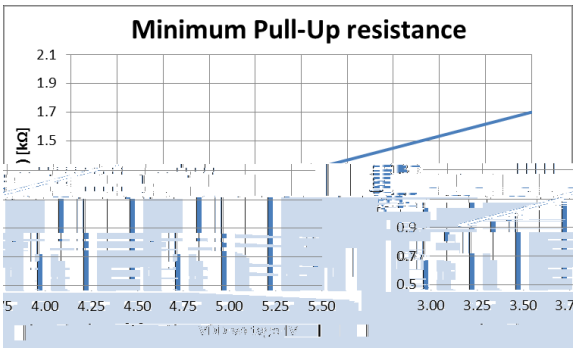


Figure 1. Rp(min) Versus VDD Voltage

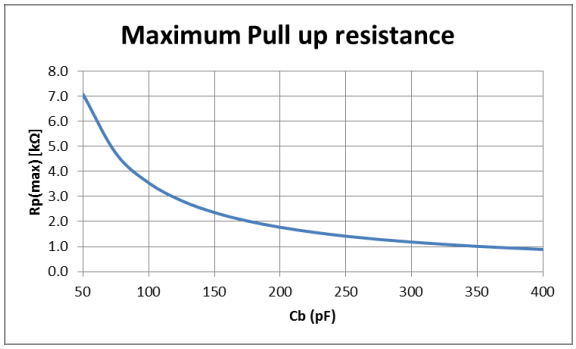


Figure 2. Rp (max) Versus Bus Capacity

For VDD = 3.3 V and bus capacity 100 pF the Pull−up resistors should be in range of 0.98 kΩ to 3.45 kΩ

FORMAT OF THE I²C FRAMES

Writing and reading data to the NCV7685 drivers uses a simple protocol: the address is written, and then data are

NCV7685 I²C ADDRESSING

The NCV7685 driver is using 7−bit I²C address. Up to 32 NCV7685 devices can be addressed using the 5−bits ADD[4:0] OTP register. The remaining two bits of the I²C address are fixed: ADD[6:5] = 11.

The default I²C address configuration of the non−zapped device is 0b1100000 = 0x60 + R/W flag which is automatically generated by μC.

Table 1. THE 1ST BYTE STRUCTURE OF I²C DEVICE ADDRESS

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	0	0	0	0	1/0

After first address byte which is automatically send by Master I²C device, the repeated address data byte has to be send. The second I²C address data byte is safety mechanism to improve the immunity of the system. This byte contains 8−bits of the data where the address (ADD[4:0]) and W = 0 flag is included in the data byte.

Table 2. THE 2ND BYTE STRUCTURE OF I²C DEVICE ADDRESS

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	0	0	0	0

This second byte is send as regular data content. The default value for not zapped device is 0xC0. The list of the all possible combinations is mentioned in the Table 3.

Table 3. LIST OF THE I²C DEVICE ADDRESS

5−bit	7−bit	8−bit
ADD [4:0] Device#	1st I²C Address byte	2nd I²C Address byte
0		

OTP PROGRAMMING

To access the Hardcoding and OTP registers the ISET pin has to be put to high; otherwise the slave device will not respond on these three OTP I^2C messages (ID_SET_OTP, ID_LOCK_OTP and ID_READ_OTP).

The I^2C address, Open Load detection modes, CRC activation, silicon ID device and channel configuration can be read/(write) by OTP messages.

The ISET pin has to be externally pulled high to the voltage between 2.5 V and 3.3 V otherwise the driver will not accept the I^2C message.

The main intention of forcing 2.5 V – 3.3 V to the ISET pin is protection against entering to the programming mode during the normal operation. And this technique is also used as chip select functionality for the End−Of−Line OTP programming procedure.

Three sets of the commands are available to access the OTP registers: ID_SET_OTP (W), ID_LOCK_OTP (W) and ID_READ_OTP(R).

The ID_SET_OTP message will write the information into shadow registers without affecting the OTP registers. The information in registers is lost when both power supplies (VDD and VS) are turned off.

The ID_LOCK_OTP message will zap the OTPs. No further change will be possible. It is necessary to have VS supply voltage higher than 13 V to ensure proper zapping procedure.

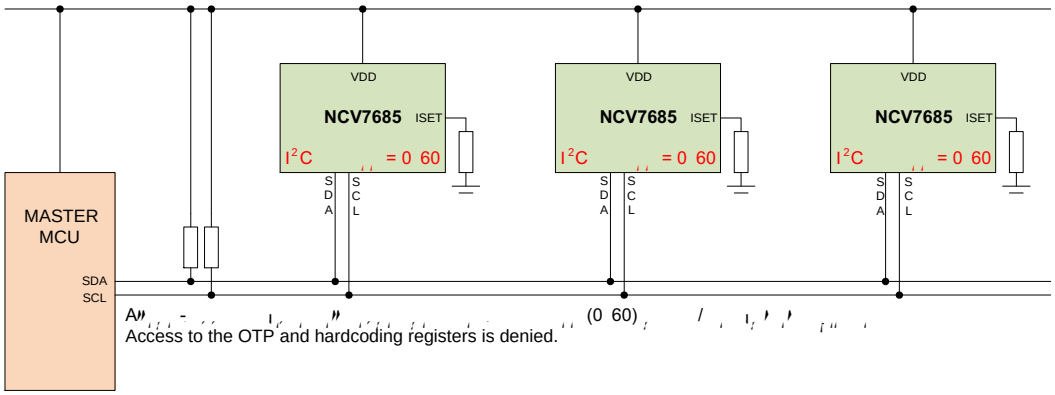
Please note that as soon as the ID_SET_OTP or ID_LOCK_OTP is processed, all other I^2C messages have to be sent with respect to the new I^2C address or CRC activation setting.

REQUIRED TIME DELAY FOR OTP ZAPPING

As soon as the ID_LOCK_OTP message is received, the I^2C acknowledge is immediately sent out to the MCU. However, the internal circuitries still requires 500 μs time delay to complete the OTP zapping of one OTP bit. Therefore, no I^2C confirmation is send. The number of OTP bits that are zapped corresponds with each change from the default values. It is needed 16.5 ms in total to successfully finish the zapping sequence of all 32 customer bits + one internal bit. The verification of the OTP banks can be done by readout of the ID_READ_OTP I^2C message after zapping delay.

CHANGING THE OTP ADDRESS ON THE SAME I^2C BUS

Every non−zapped device has the same I^2C address. To change the address, the ID_SET_OTP or ID_LOCK_OTP message with appropriate content has to be sent. It is necessary to put the ISET pin to high, to address appropriate device. The graphic representation of the End−of−Line OTP programming is shown in Figure 6.



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Access to the OTP and hardcoding registers is denied.