

# 2N6052

Preferred Device

## Darlington Complementary Silicon Power Transistors

This package is designed for general-purpose amplifier and low frequency switching applications.

### Features

- High DC Current Gain —  $h_{FE} = 3500$  (Typ) @  $I_C = 5.0$  Adc
- Collector–Emitter Sustaining Voltage — @ 100 mA  
 $V_{CEO(sus)} = 100$  Vdc (Min)
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors
- This is a Pb–Free Device\*

### MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	100	Vdc
Collector–Base Voltage	$V_{CB}$	100	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current – Continuous Peak	$I_C$	12 20	Adc
Base Current	$I_B$	0.2	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	150 0.857	W W/ $^\circ\text{C}$
Operating and Storage Temperature Range	$T_J, T_{stg}$	–65 to +200	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	1.17	$^\circ\text{C}/\text{W}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Indicates JEDEC Registered Data.

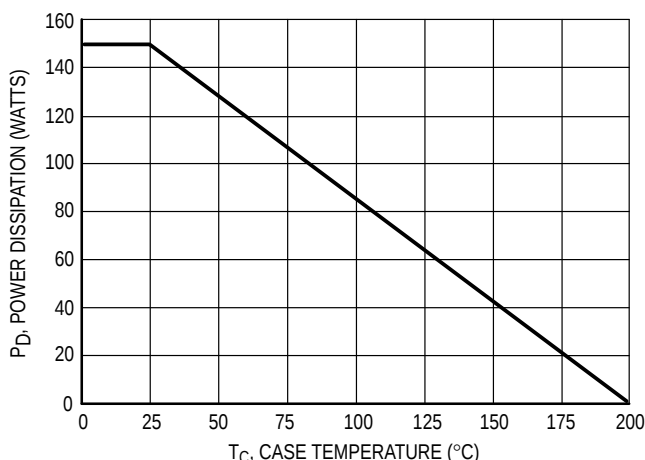


Figure 1. Power Derating



<http://onsemi.com>

**12 AMPERE  
COMPLEMENTARY SILICON  
POWER TRANSISTOR  
100 VOLTS, 150 WATTS**

### MARKING DIAGRAM

2N6052G  
AYYWW  
MEX

**TO–204AA (TO–3)  
CASE 1–07  
STYLE 1**

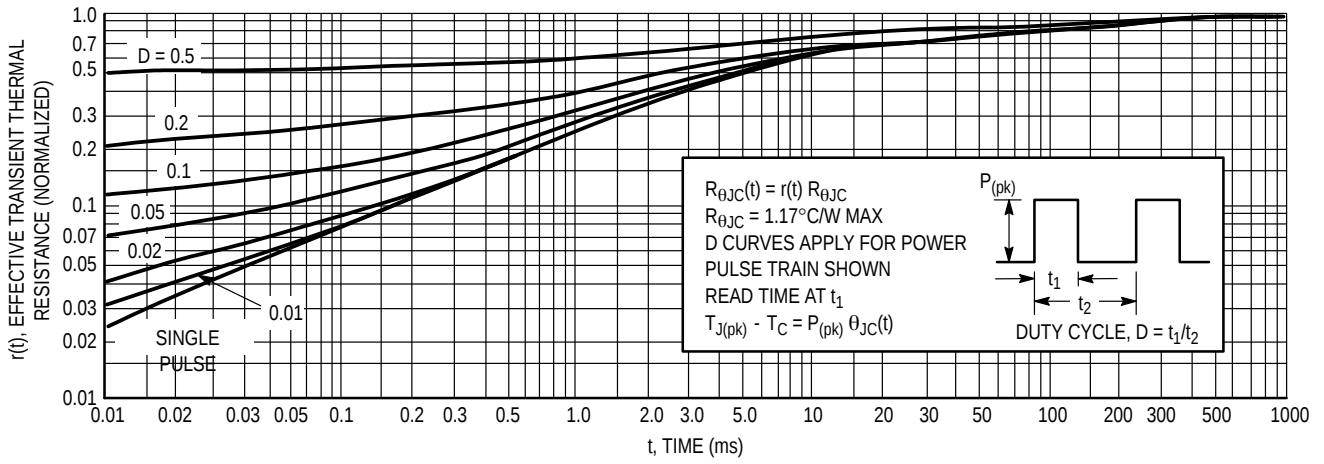
2N6052 = Device Code  
G = Pb–Free Package  
A = Location Code  
YY = Year  
WW = Work Week  
MEX = Country of Origin

Device	Package	Shipping (TO)

\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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**Figure 4. Thermal Response**

There are two limitations on the power handling ability of a transistor: average junction temperature and second

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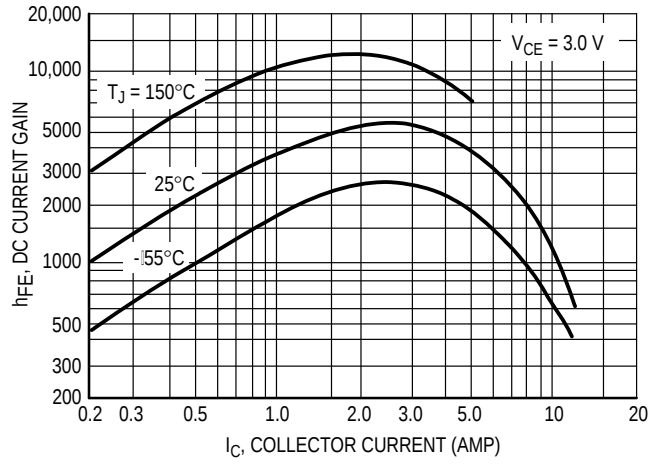


Figure 8. DC Current Gain

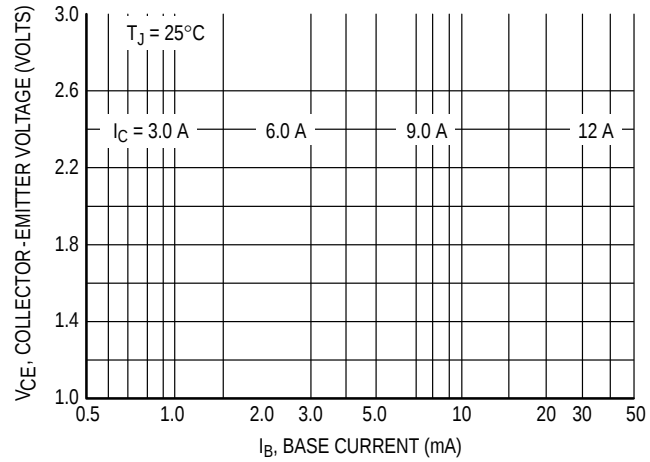


Figure 9. Collector Saturation Region

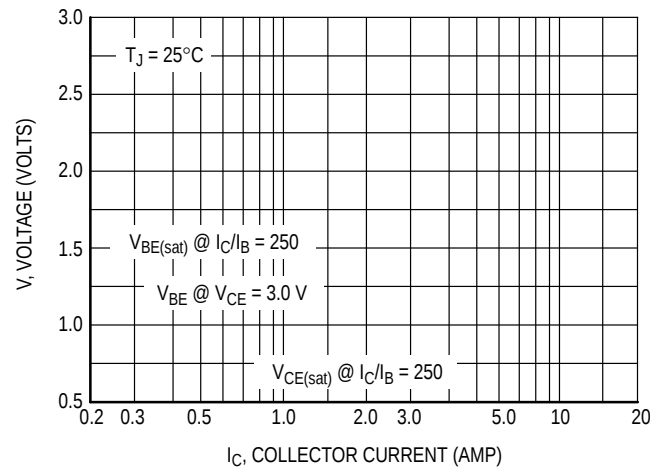
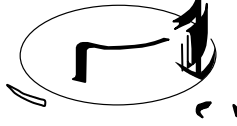


Figure 10. "On" Voltages

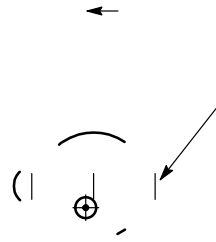
E6: 1. A E 2. E E CASE: C EC	E7: 1. A DE 2. E CASE: CA DE	E8: 1. CA DE #1 2. CA DE #2 CASE: A DE	E9: 1. A DE #1 2. A DE #2 CASE: CA DE
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TO-204 (TO-3)



S A 1:1

E8  
 1. D E A D E A C E A  
 14.5, 1982.  
 2. C D E : C  
 3. A E A D E A CA ED  
 EFE E CED -204AA E A



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