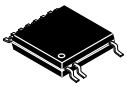
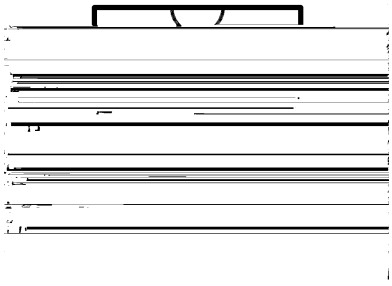
2-

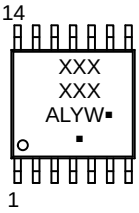
2, 2

The AC32/ACT32 contains four, 2−input OR gates.

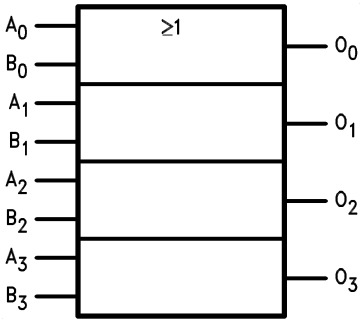
- I_{CC} Reduced by 50% on 74AC Only
- Outputs Source/Sink 24 mA
- ACT32 Has TTL−Compatible Inputs
- These are Pb−Free and Halide Free Devices







XXX	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package



A_n, B_n	Inputs
O_n	Outputs

V_{CC}	Supply Voltage		−0.5 to +6.5	V
I_{IK}	DC Input Diode Current	V_I = −0.5 V	−20	mA
		V_I = V_{CC} + 0.5 V	+20	mA
V_I	DC Input Voltage		−0.5 to V_{CC} +0.5	V
I_{OK}	DC Output Diode Current	V_O = –0.5 V	−20	mA
I_{OK}	DC Output Diode Current	V_O = V_{CC} + 0.5 V	+20	mA
V_O	DC Output Voltage		−0.5 to V_{CC} +0.5	V
I_O	DC Output Source or Sink Current		±50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin		±50	mA
T_{STG}	Storage Temperature		−65 to +150	°C
T_J	Junction temperature		140	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

V_{CC}	Supply Voltage	AC	2.0	6.0	V
		ACT	4.5	5.5	
V_I	Input Voltage		0	V_{CC}	V
V_O	Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		−40	+85	°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, AC Devices: V_{IN} from 30% to 70% of V_{CC}, V_{CC} @ 3.3 V, 4.5 V, 5.5 V		−	125	mV/ns
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACT Devices: V_{IN} from 0.8 V to 2.0 V, V_{CC} @ 4.5 V, 5.5 V		−	125	mV/ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

			°			– °	°	
		(Note 6)						
t_{PLH}	Propagation Delay	3.3	1.5	7.5	9.0	1.5	10.0	ns
		5.0	1.5	5.5	7.5	1.0	8.5	
t_{PHL}	Propagation Delay	3.3	1.5	7.0	8.5	1.0	9.0	ns
		5.0	1.5	5.0	7.0	1.0	7.5	

6. Voltage range 3.3 is 3.3 V ± 0.3 V. Voltage range 5.0 is 5.0 V ± 0.5 V.

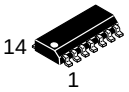
			°			– °	°	
		(Note 6)						
t_{PLH}	Propagation Delay	5.0	1.0	6.5	9.0	1.0	10.0	ns
t_{PHL}	Propagation Delay	5.0	1.0	6.5	9.0	1.0	10.0	ns

7. Voltage Range 5.0 is 5.0 V ± 0.5 V.

C_{IN}	Input Capacitance	V_{CC} = Open	4.5	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 5.0 V	20.0	pF

			†
74AC32SCX	AC32	SOIC14, Case 751EF (Pb−Free)	2500 / Tape & Reel
74AC32MTCX	AC 32	TSSOP−14 WB, Case 948G (Pb−Free)	2500 / Tape & Reel
74ACT32SC	ACT32	SOIC−14 NB, Case 751A−03 (Pb−Free)	55 Units / Tube
74ACT32SCX	ACT32	SOIC14, Case 751EF (Pb−Free)	2500 / Tape & Reel
74ACT32MTCX	ACT 32	TSSOP−14 WB, Case 948G (Pb−Free)	2500 / Tape & Reel

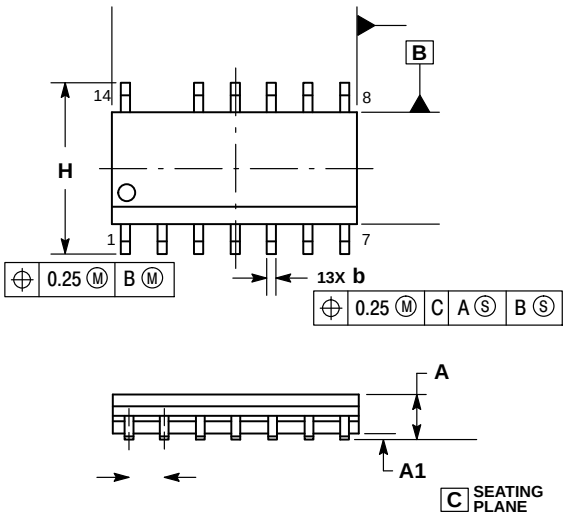
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 1:1

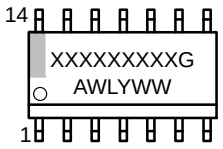
SOIC 14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

STYLES ON PAGE 2

SOIC 14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE

SOIC14