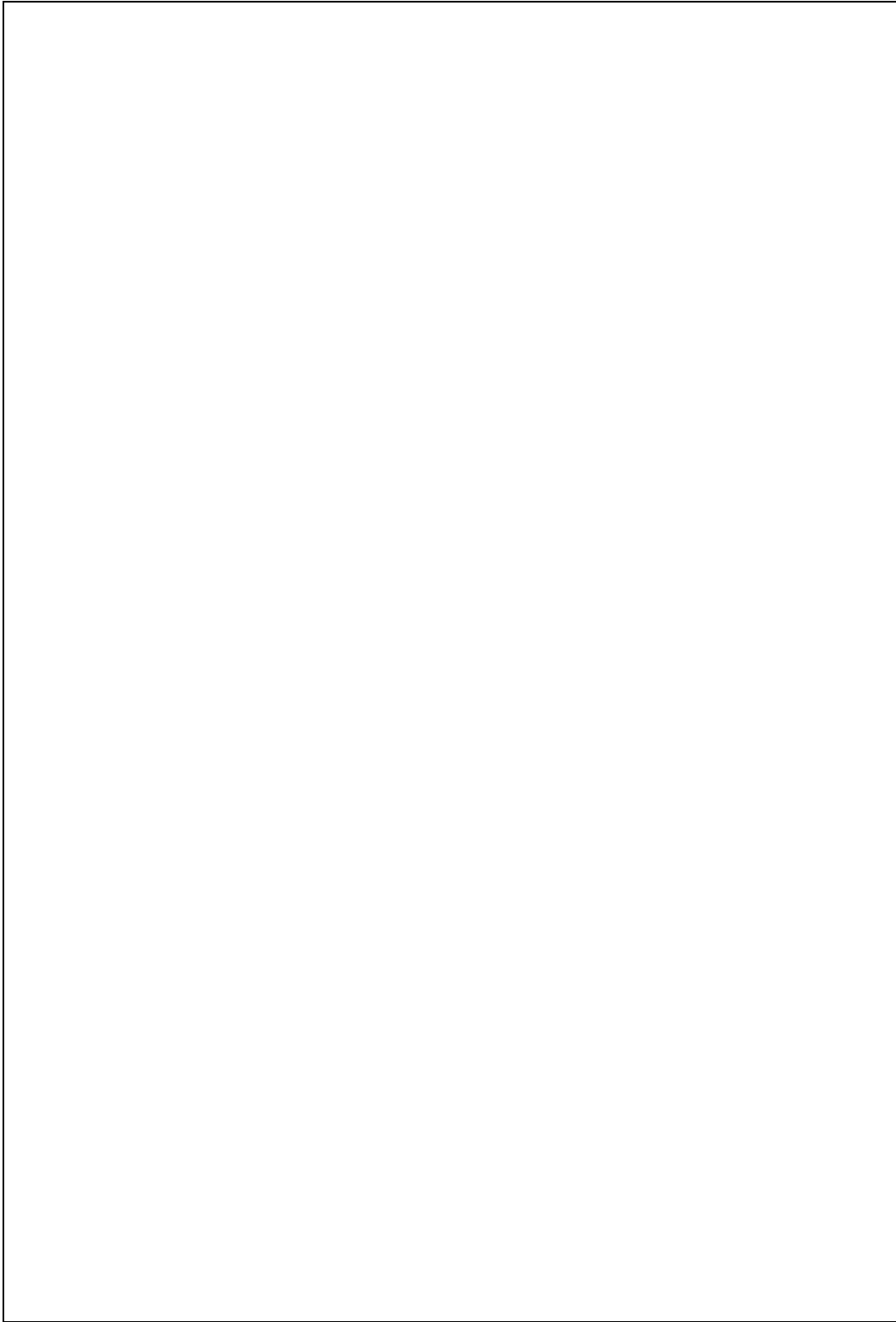


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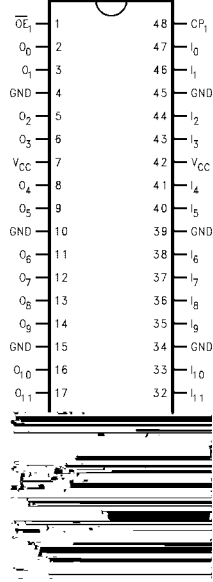
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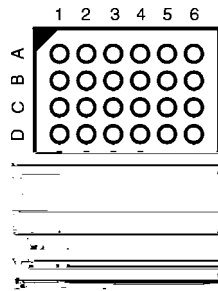


Connection Diagrams

Pin Assignment for SSOP and TSSOP



Pin Assignment for FBGA



(Top Thru View)

Pin Descriptions

Pin Names	Description
\overline{OE}_n	Output Enable Input (Active LOW)
CP_n	Clock Pulse Input
I_0-I_{15}	Inputs
O_0-O_{15}	Outputs
NC	No Connect

FBGA Pin Assignments

	1	2	3	4	5	6
A	O_0	NC	\overline{OE}_1	CP_1	NC	I_0
B	O_2	O_1	NC	NC	I_1	I_2
C	O_4	O_3	V_{CC}	V_{CC}	I_3	I_4
D	O_6	O_5	GND	GND	I_5	I_6
E	O_8	O_7	GND	GND	I_7	I_8
F	O_{10}	O_9	GND	GND	I_9	I_{10}
G	O_{12}	O_{11}	V_{CC}	V_{CC}	I_{11}	I_{12}
H	O_{14}	O_{13}	NC	NC	I_{13}	I_{14}
J	O_{15}	NC	\overline{OE}_2	CP_2	NC	I_{15}

Truth Tables

Inputs			Outputs
CP_1	\overline{OE}_1	I_0-I_7	O_0-O_7
\curvearrowright	L	H	H
\curvearrowright	L	L	L
L	L	X	O_0
X	H	X	Z

Inputs			Outputs
CP_2	\overline{OE}_2	I_8-I_{15}	O_8-O_{15}
\curvearrowright	L	H	H
\curvearrowright	L	L	L
L	L	X	O_0
X	H	X	Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 O_0 = Previous O_0 before HIGH-to-LOW of CP

Functional Description

74LCX162374

Absolute Maximum Ratings(Note 4)

Recommended Operating Conditions (Note 6)

Note 4: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 5:

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units
				Min	Max	
I _{OFF}	Power-Off Leakage Current	V _I or V _O = 5.5V	0		10	μA
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND	2.3 – 3.6		20	μA
		3.6V ≤ V _I , V _O ≤ 5.5V (Note 7)	2.3 – 3.6		±20	μA
I _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} - 0.6V	2.3 – 3.6		500	μA

Note 7: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

Symbol	Parameter	T _A = -40° to +85°C, R _L = 500Ω						Units
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		V _{CC} = 2.5V ± 0.2V		
		C _L = 50 pF		C _L = 50 pF		C _L = 30 pF		
		Min	Max	Min	Max	Min	Max	
t _{PD}	0.0056							
	LV	f 50						
		Min	Max					

Note 8: Skew is defined as the absolute value of the differences between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics**Capacitance**

AC LOADING and WAVEFORMS Generic for LCX Family

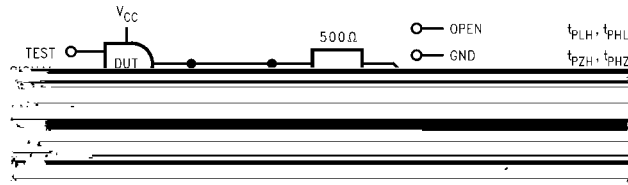
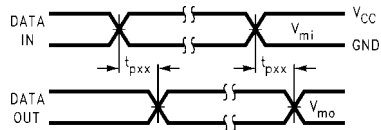


FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)

Test	Switch
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$, and $2.7V$ $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
t_{PZH} , t_{PHZ}	GND



Waveform for Inverting and Non-Inverting Functions

3-STATE Output High Enable and Disable Times for Logic

Propagation Delay, Pulse Width and t_{rec} Waveforms

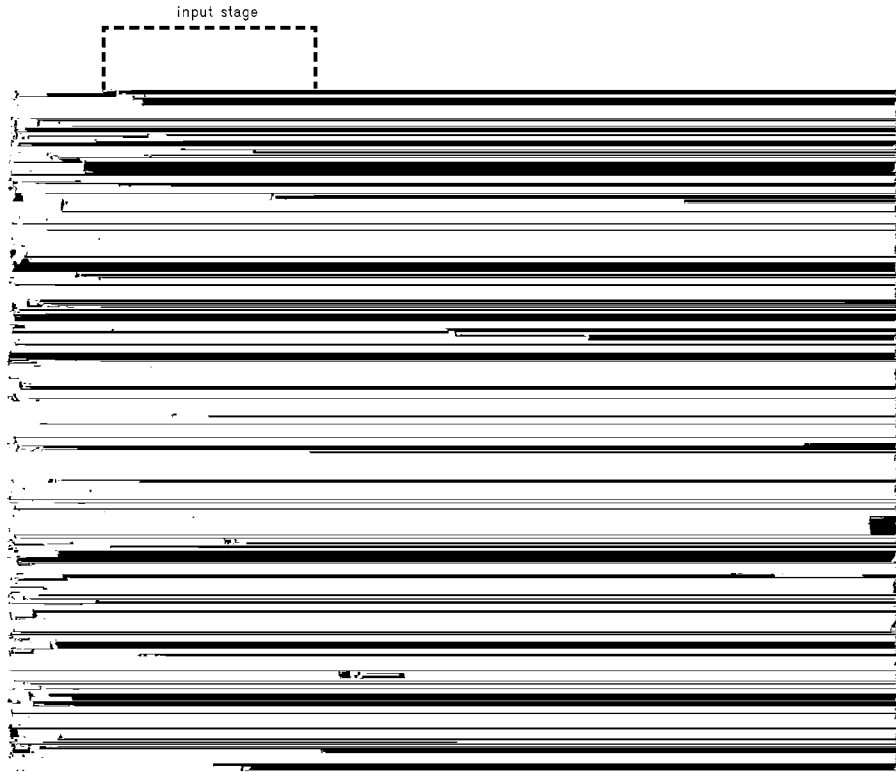
Setup Time, Hold Time and Recovery Time for Logic

3-STATE Output Low Enable and Disable Times for Logic

t_{rise} and t_{fall}

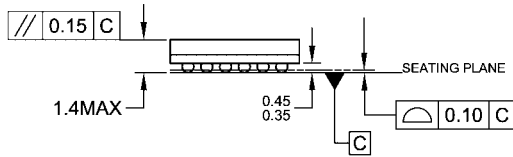
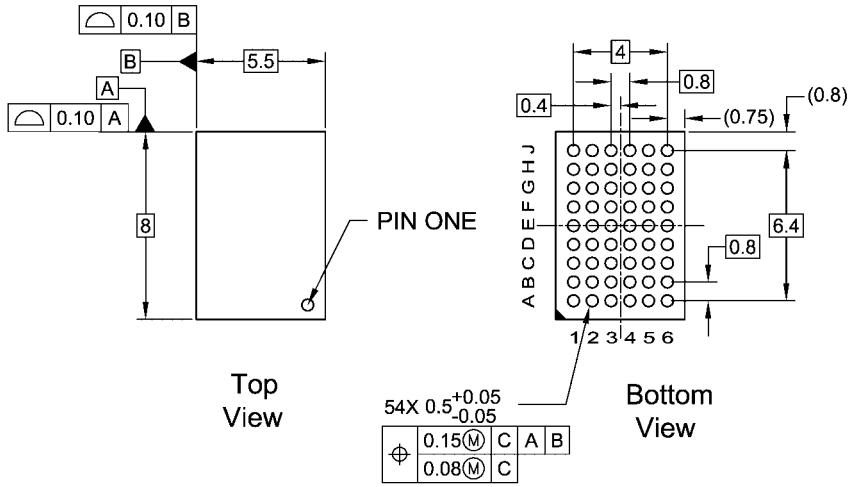
FIGURE 2. Waveforms
(Input Characteristics; $f = 1MHz$, $t_r = t_f = 3ns$)

Schematic Diagram Generic for LCX Family

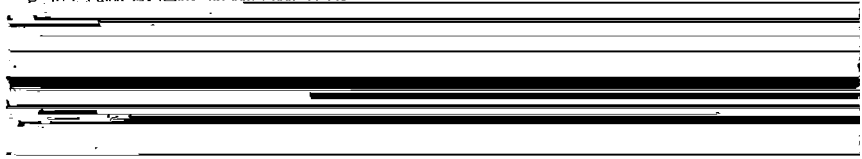


74LCX162374

Physical Dimensions inches (millimeters) unless otherwise noted



NOTES:
 A. THIS PACKAGE CONFORMS TO JEDEC M0-205
 B. ALL DIMENSIONS IN MILLIMETERS



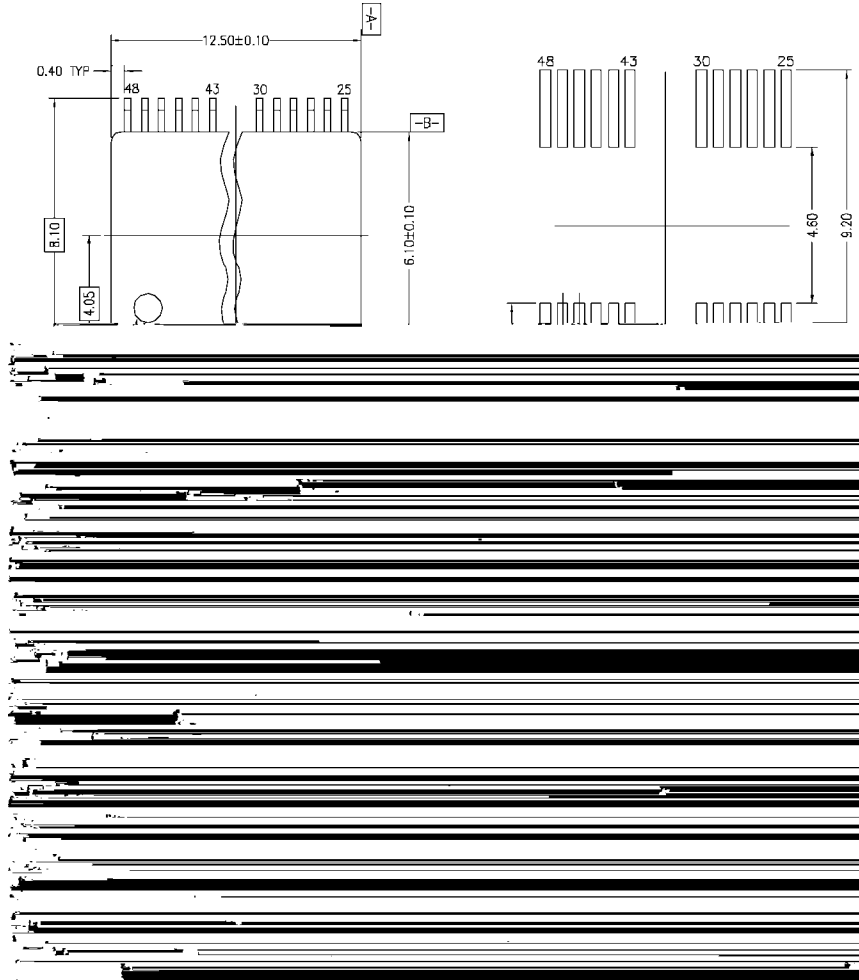
54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
 Package Number BGA54A
 Preliminary

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

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