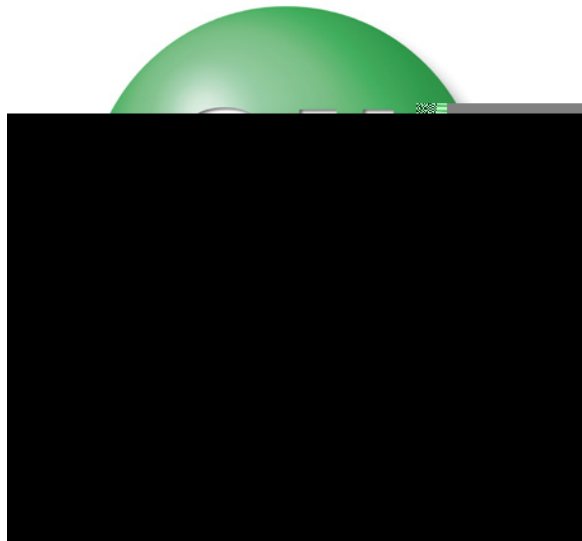




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**74LCX16373 Low Voltage 16-Bit Transparent Latch with 5V Tolerant Inputs and Outputs**

February 1994  
Revised May 2005



**Connection Diagrams**

Pin Assignment for SSOP and TSSOP

**Pin Descriptions**

**FBGA Pin Assignments**

**Truth Tables**

Pin Assignment for FBGA

**(Top Thru View)**

H = HIGH Voltage Level  
L = LOW Voltage Level  
X =

## Functional Description

The LCX16373 contains sixteen D-type latches with 3-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable ( $LE_n$ ) input is HIGH, data on

**Absolute Maximum Ratings** (Note 4)

Symbol	Parameter	Value	Conditions	Units
$V_{CC}$	Supply Voltage			

**Recommended Operating Conditions** (Note 6)

**Note 4:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 5:**  $I_O$  Absolute Maximum Rating must be observed.

**Note 6:** Unused inputs must be held HIGH or LOW. They may not float.

**DC Electrical Characteristics**

**DC Electrical Characteristics** (Continued)

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		Units
				Min	Max	
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CC</sub> or GND	2.3 – 3.6		20	μA
		3.6V ≤ V <sub>I</sub> , V <sub>O</sub> ≤ 5.5V (Note 7)	2.3 – 3.6		±20	
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	V <sub>IH</sub> = V <sub>CC</sub> - 0.6V	2.3 – 3.6		500	μA

Note 7: Outputs disabled or 3-STATE only.

**AC Electrical Characteristics**

Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C, R <sub>L</sub> = 500Ω						Units
		V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 2.5V ± 0.2V		
		C <sub>L</sub> = 50 pF		C <sub>L</sub> = 50 pF		C <sub>L</sub> = 30 pF		
		Min	Max	Min	Max	Min	Max	
t <sub>PHL</sub>	Propagation Delay	1.5	5.4	1.5	5.9	1.5	6.5	ns
t <sub>PLH</sub>	I <sub>n</sub> to O <sub>n</sub>	1.5	5.4	1.5	5.9	1.5	6.5	ns
t <sub>PHL</sub>	Propagation Delay	1.5	5.5	1.5	6.4	1.5	6.6	ns
t <sub>PLH</sub>	LE to O <sub>n</sub>	1.5	5.5	1.5	6.4	1.5	6.6	ns
t <sub>PZL</sub>	Output Enable Time	1.5	6.1	1.5	6.5	1.5	7.9	ns
t <sub>PZH</sub>		1.5	6.1	1.5	6.5	1.5	7.9	ns
t <sub>PLZ</sub>	Output Disable Time	1.5	6.0	1.5	6.3	1.5	7.2	ns
t <sub>PHZ</sub>		1.5	6.0	1.5	6.3	1.5	7.2	ns
t <sub>S</sub>	Setup Time, I <sub>n</sub> to LE	2.5		2.5		3.0		ns
t <sub>H</sub>	Hold Time, I <sub>n</sub> to LE	1.5		1.5		2.0		ns
t <sub>W</sub>	LE Pulse Width	3.0		3.0		3.5		ns
t <sub>OSSL</sub>	Output to Output Skew (Note 8)		1.0					ns
t <sub>OSLH</sub>			1.0					ns

Note 8: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSSL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

**Dynamic Switching Characteristics**

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C	Units
				Typical	
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	3.3	0.8	V
		C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5V, V <sub>IL</sub> = 0V	2.5	0.6	
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	3.3	-0.8	V
		C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5V, V <sub>IL</sub> = 0V	2.5	-0.6	

**Capacitance**

Symbol	Parameter	Conditions	Typical	Units
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = Open, V <sub>I</sub> = 0V or V <sub>CC</sub>	7	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub>	8	pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub> , f = 10 MHz	20	pF

**AC LOADING and WAVEFORMS** Generic for LCX Family

**FIGURE 1. AC Test Circuit ( $C_L$  includes probe and jig capacitance)**

**Waveform for Inverting and Non-Inverting Functions**

**Propagation Delay, Pulse Width and  $t_{rec}$  Waveforms**

**3-STATE Output Low Enable and**

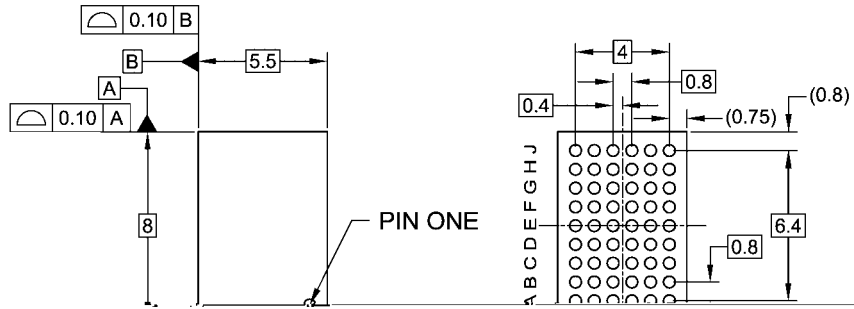
**Schematic Diagram** Generic for LCX Family



74LCX16373



**Physical Dimensions** inches (millimeters) unless otherwise noted



54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide  
Package Number BGA54A



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide  
Package Number MTD48

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