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March 1995  
Revised June 2002

## 74LCX16500

### Low Voltage 18-Bit Universal Bus Transceivers with 5V Tolerant Inputs and Outputs

#### General Description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs.

The LCX16500 is designed for low voltage (2.5V or 3.3V)  $V_{CC}$  applications with the capability of interfacing to a 5

74LCX16500 Low Voltage 18-Bit Universal Bus Transceivers with 5V Tolerant Inputs and Outputs

**Connection Diagrams**

Pin Assignment for SSOP and TSSOP

**Pin Descriptions**

**FBGA Pin Assignments**

**Truth Table** (Note 4)

Pin Assignment for FBGA

Note 4:

(Top Thru View)

### Logic Diagram

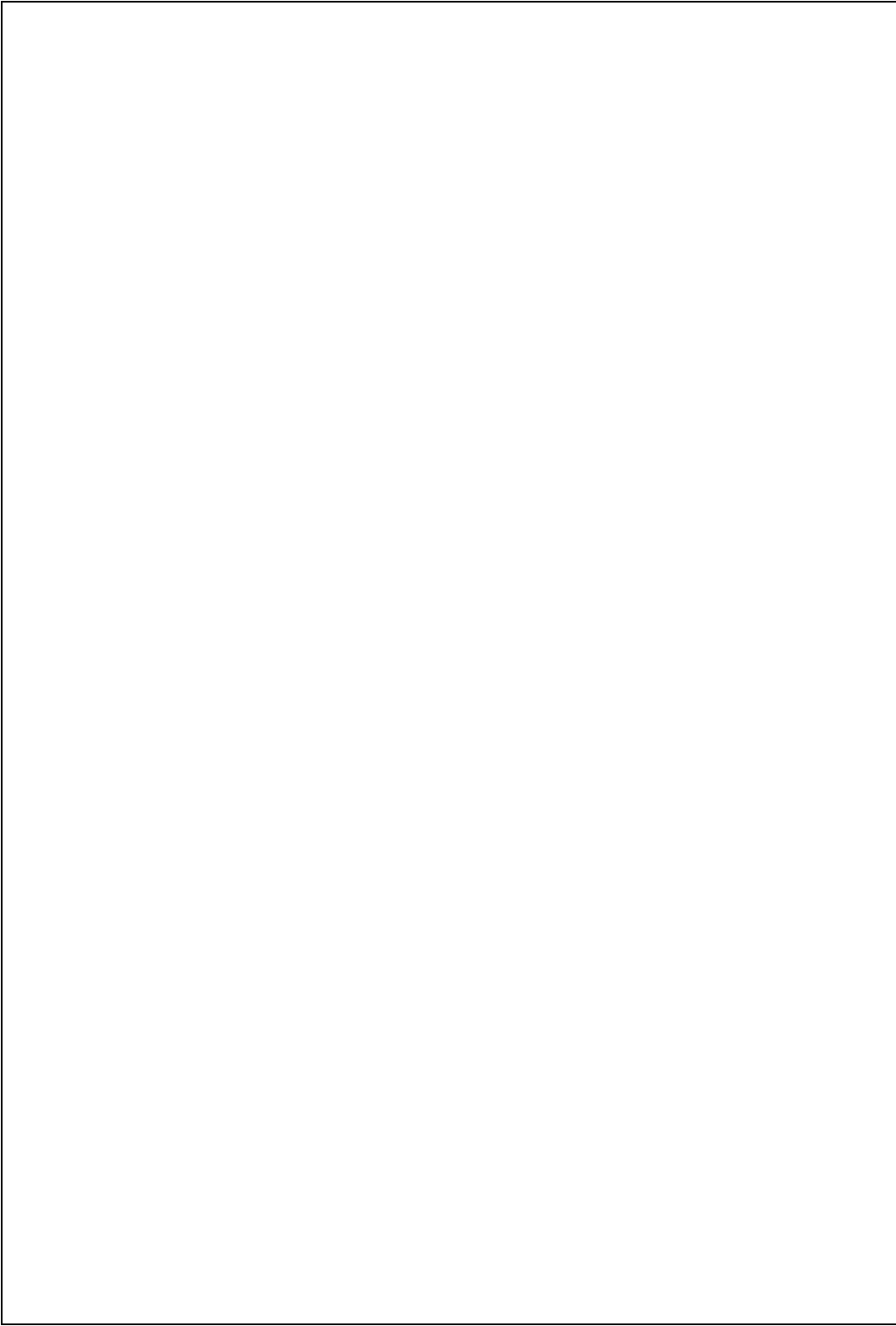


**Absolute Maximum Ratings**(Note 7)

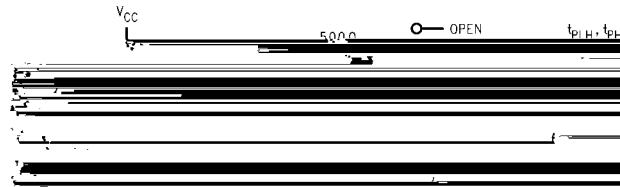
**Recommended Operating Conditions**

(Note 9)

**Note 7:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated

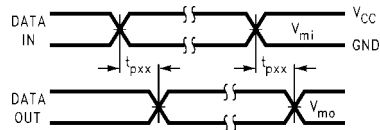


**AC LOADING and WAVEFORMS** Generic for LCX Family

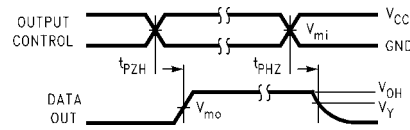


**FIGURE 1. AC Test Circuit ( $C_L$  includes probe and jig capacitance)**

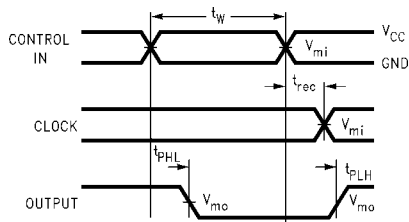
Test	Switch
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	6V at $V_{CC} = 3.3 \pm 0.3V$ , and 2.7V $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
$t_{PZH}, t_{PHZ}$	GND



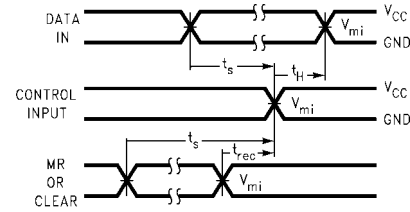
**Waveform for Inverting and Non-Inverting Functions**



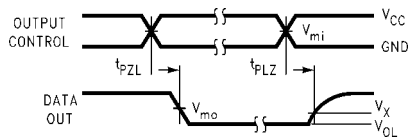
**3-STATE Output High Enable and Disable Times for Logic**



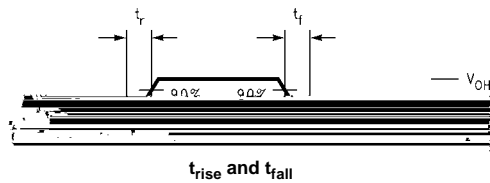
**Propagation Delay, Pulse Width and  $t_{rec}$  Waveforms**



**Setup Time, Hold Time and Recovery Time for Logic**



**3-STATE Output Low Enable and Disable Times for Logic**



**FIGURE 2. Waveforms (Input Characteristics;  $f = 1MHz$ ,  $t_r = t_f = 3ns$ )**

Symbol	$V_{CC}$		
	$3.3V \pm 0.3V$	2.7V	$2.5V \pm 0.2V$
$V_{mi}$	1.5V	1.5V	$V_{CC}/2$
$V_{mo}$	1.5V	1.5V	$V_{CC}/2$
$V_x$	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
$V_y$	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

**Schematic Diagram** Generic for LCX Family

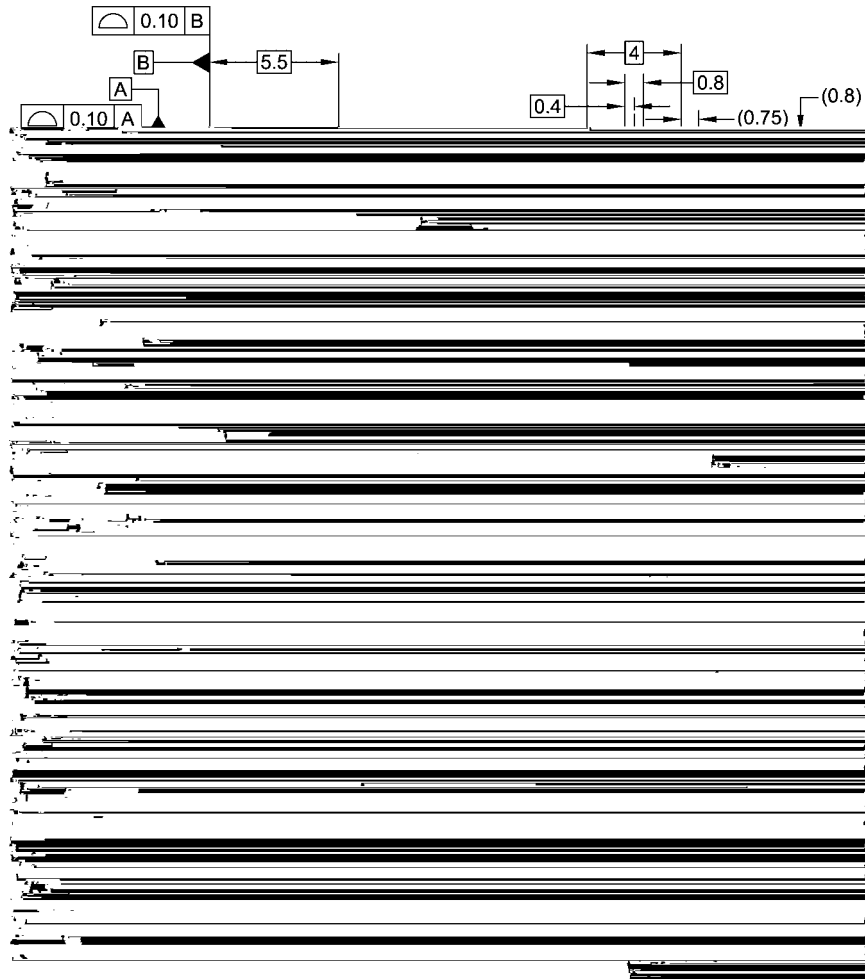


74LCX16500



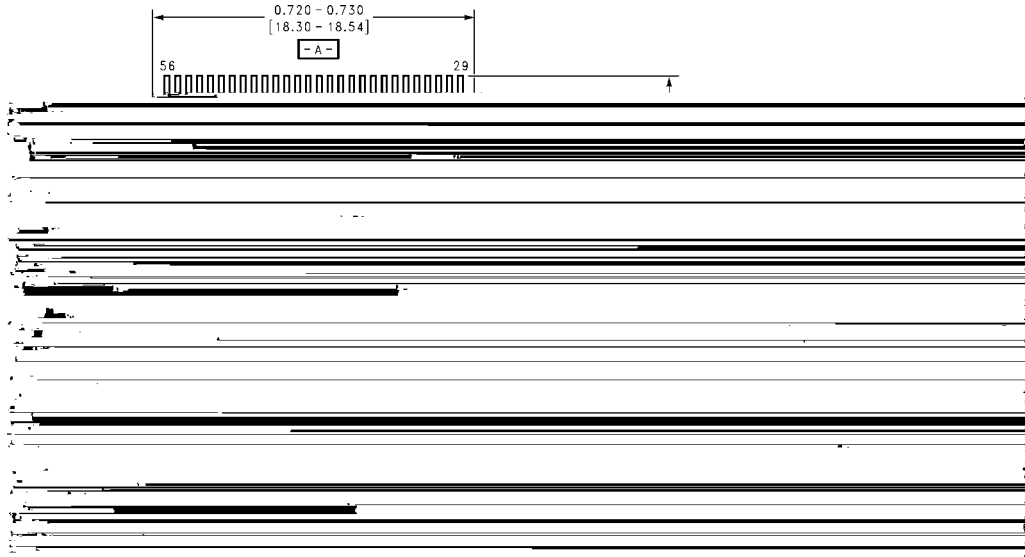
74LCX16500

**Physical Dimensions** inches (millimeters) unless otherwise noted



54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide  
Package Number BGA54A


**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide  
Package Number MS56A

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide  
Package Number MTD56

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