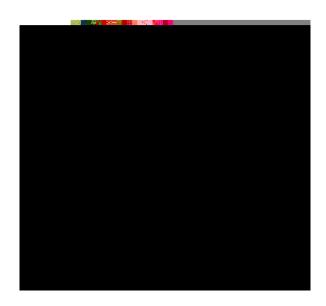


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October 1995 Revised March 2001

74LCX16501 Low Voltage 18-Bit Universal Bus Transceivers with 5V Tolerant Inputs and Outputs

General Description

The LCX16501 is an 18-bit universal bus transceiver combining D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Absolute Maximum Ratings(Note 5)

Symbol	Parameter	Value	Conditions	Units
V _{CC}	Supply Voltage	-0.5 to +7.0		V
VI	DC Input Voltage	-0.5 to +7.0		V
Vo	DC Output Voltage	-0.5 to +7.0	Output in 3-STATE	V
		-0.5 to $V_{CC} + 0.5$	Output in HIGH or LOW State (Note 6)	V
I _{IK}	DC Input Diode Current	-50	$V_I < GND$	mA
I _{OK}	DC Output Diode Current	-50	V _O < GND	mA
		+50	$V_O > V_{CC}$	ША
Io	DC Output Source/Sink Current	±50		mA
I _{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T _{STG}	Storage Temperature	_		

Recommended Operating Conditions (Note 7)

Note 5: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 6: I_O Absolute Maximum Rating must be observed.

Note 7: Unused (inputs or I/Os) must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	v _{cc}	V_{CC} $T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Units
		Conditions	(V)	Min	Max	Units
Icc	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 - 3.6		20	
		$3.6V \le V_1$, $V_2 \le 5.5V$ (Note 8)	2.3 - 3.6		+20	μΑ

ΔI_{CC} Increase in I

Note 8: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (to_Sht), or LOW-to-HIGH (to_Sht).

Dynamic Switching Characteristics

Capacitance

AC LOADING and WAVEFORMS Generic for LCX Family

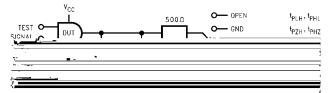
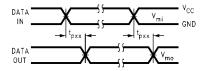
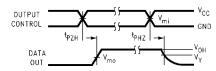


FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)

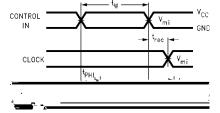
Test	Switch		
t _{PLH} , t _{PHL}	Open		
t _{PZL} , t _{PLZ}	6V at V_{CC} = 3.3 \pm 0.3V V_{CC} x 2 at V_{CC} = 2.5 \pm 0.2V		
t _{PZH} ,t _{PHZ}	GND		



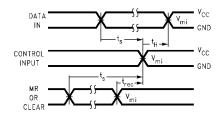
Waveform for Inverting and Non-Inverting Functions



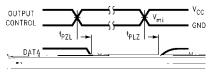
3-STATE Output High Enable and Disable Times for Logic



Propagation Delay. Pulse Width and t_{rec} Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic

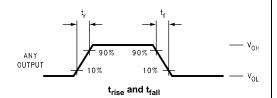
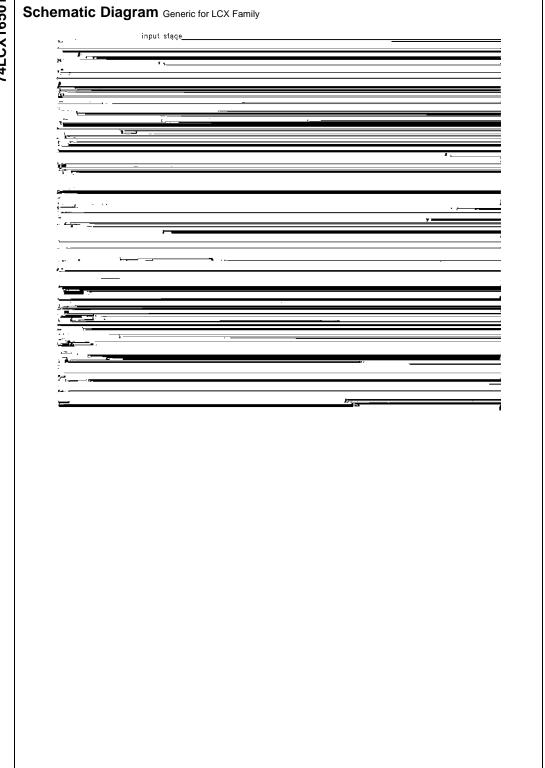
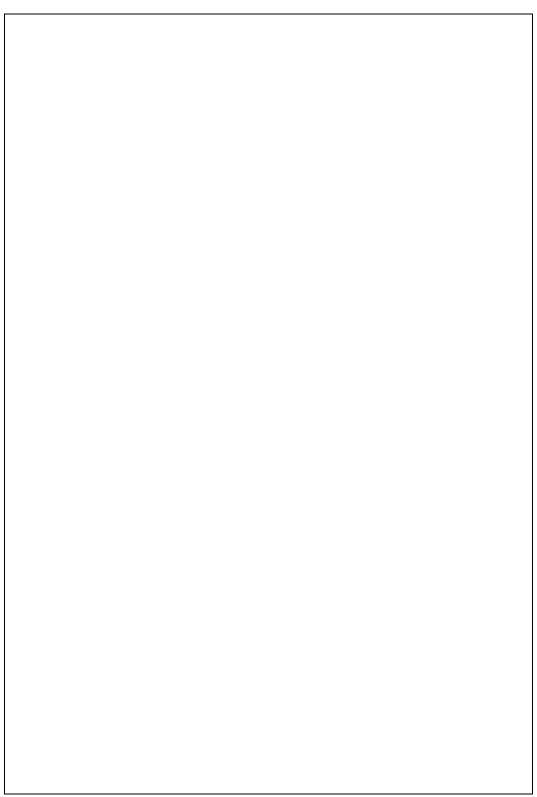
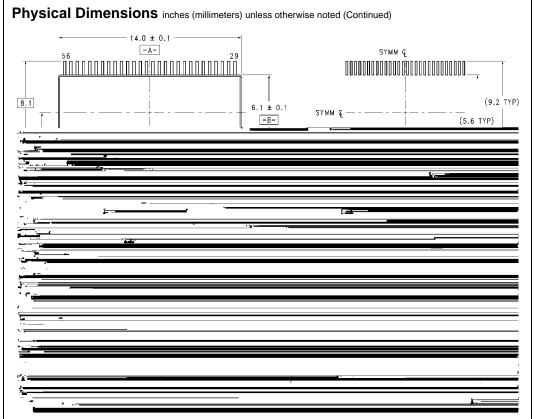


FIGURE 2. Waveforms (Input Characteristics; f =1MHz, $t_r = t_f = 3ns$)

Symbol	V _{cc}				
Cymber	$3.3V \pm 0.3V$	2.7V	2.5V ± 0.2V		
V _{mi}	1.5V	1.5V	V _{CC} /2		
V _{mo}	1.5V	1.5V	V _{CC} /2		
V _x	V _{OL} + 0.3V	$V_{OL} + 0.3V$	V _{OL} + 0.15V		
V _y	V _{OH} – 0.3V	V _{OH} – 0.3V	V _{OH} – 0.15V		







56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD56

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