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## Features

- 5V tolerant inputs and outputs
- 2.3V – 3.6V  $V_{CC}$  specifications provided
- 7.0 ns  $t_{PD}$  max ( $V_{CC} = 3.3V$ ), 10  $\mu A$   $I_{CC}$  max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- $\pm 24$  mA Output Drive ( $V_{CC} = 3.0V$ )
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V

**Note 1:** To ensure the high-impedance state during power up or down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

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## Ordering Code:

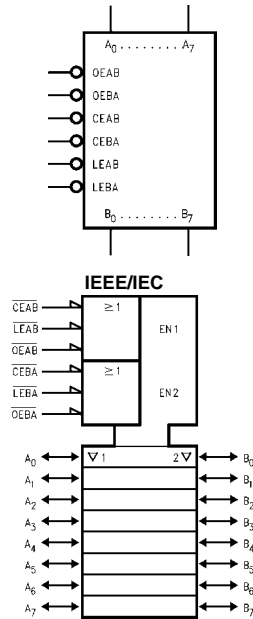
Order Number	Package Number	Package Description
74LCX543WM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74LCX543MSA	MSA24	24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Connection Diagram

## Pin Descriptions

Logic Symbols



Data I/O Control Table

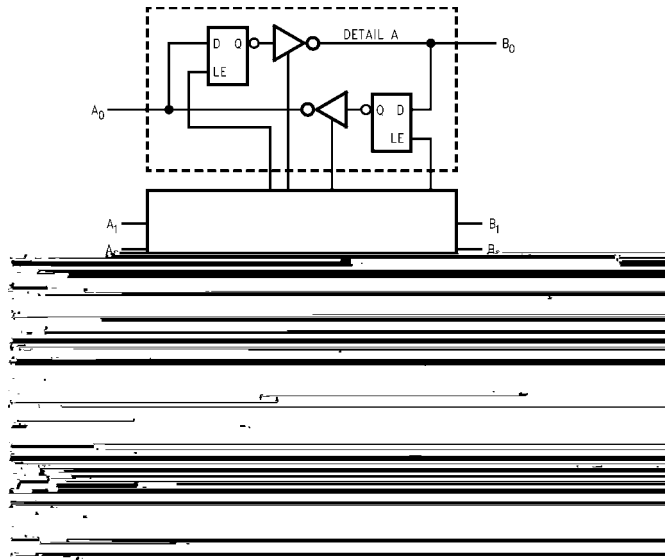
Inputs			Latch Status	Output Buffers
CEAB	LEAB	OEAB		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 A-to-B data flow shown; B-to-A flow control is the same, except using CEBA, LEBA and OEBA

Functional Description

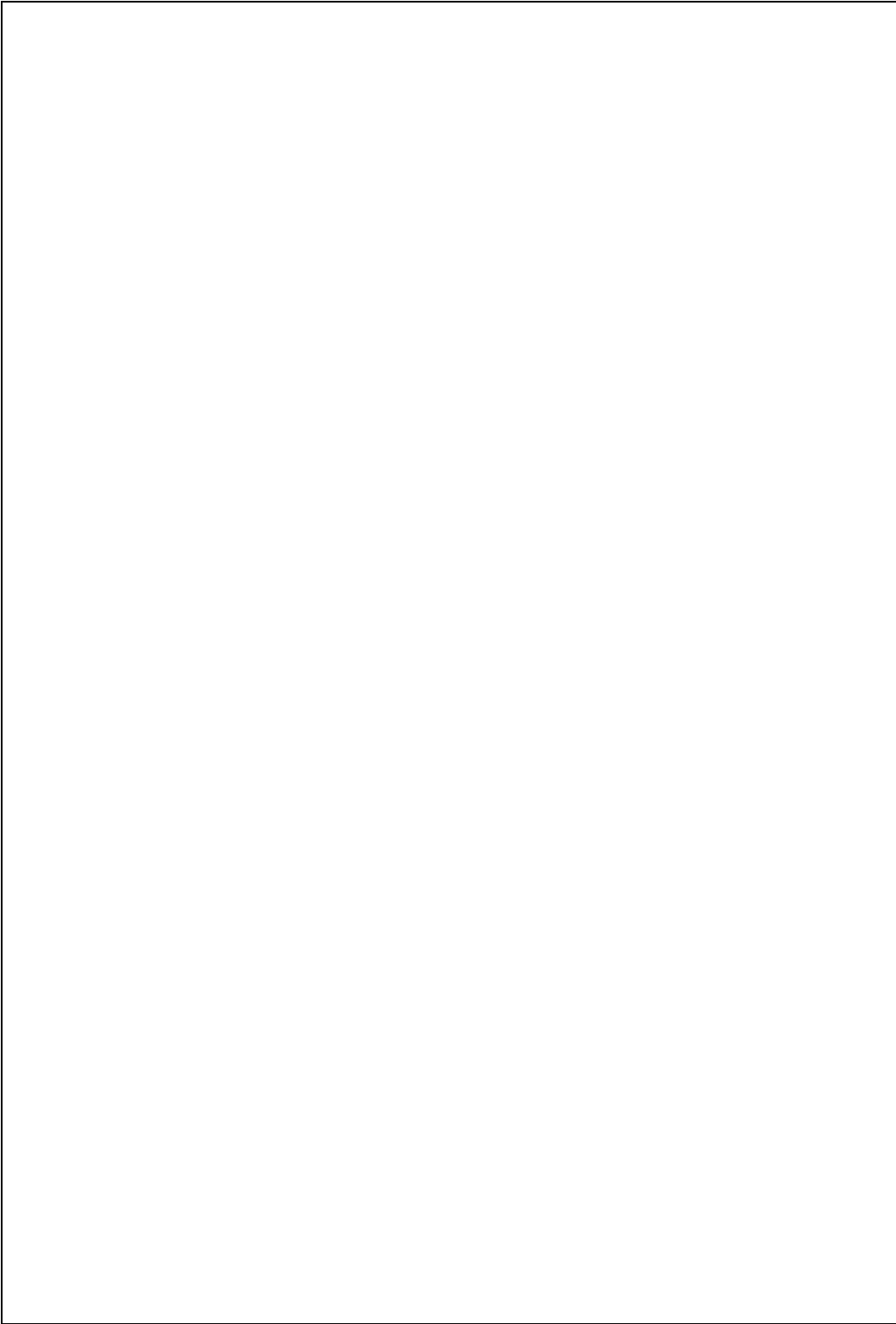
The LCX543 contains two sets of eight D-type latches, with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable (CEAB) input must be LOW in order to enter data from A<sub>0</sub>-A<sub>7</sub> or take data from B<sub>0</sub>-B<sub>7</sub>, as indicated in the Data I/O Control Table. With CEAB LOW, a LOW signal on the A-to-B Latch Enable (LEAB) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the LEAB signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With CEAB and OEAB both LOW, the 3-STATE B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the CEBA, LEBA and OEBA inputs.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

74LCX543



**DC Electrical Characteristics** (Continued)

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		Units
				Min	Max	
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CC</sub> or GND 3.6V ≤ V <sub>I</sub> , V <sub>O</sub> ≤ 5.5V (Note 5)	2.3 – 3.6		10	μA
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	V <sub>IH</sub> = V <sub>CC</sub> - 0.6V	2.3 – 3.6		±10	μA

Note 5: Outputs disabled or 3-STATE only.

**AC Electrical Characteristics**

Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C, R <sub>L</sub> = 500Ω						Units
		V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 2.5V ± 0.2V		
		C <sub>L</sub> = 50 pF		C <sub>L</sub> = 50 pF		C <sub>L</sub> = 30 pF		
		Min	Max	Min	Max	Min	Max	
t <sub>PHL</sub>	Propagation Delay	1.5	7.0	1.5	8.0	1.5	8.4	ns
t <sub>PLH</sub>	A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>	1.5	7.0	1.5	8.0	1.5	8.4	ns
t <sub>PHL</sub>	Propagation Delay	1.5	8.5	1.5	9.5	1.5	10.5	ns
t <sub>PLH</sub>	$\overline{\text{LEBA}}$ to A <sub>n</sub> or $\overline{\text{LEAB}}$ to B <sub>n</sub>	1.5	8.5	1.5	9.5	1.5	10.5	ns
t <sub>PZL</sub>	Output Enable Time	1.5	9.0	1.5	10.0	1.5	11.0	ns
t <sub>PZH</sub>	$\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$ to A <sub>n</sub> or B <sub>n</sub> $\overline{\text{CEBA}}$ or $\overline{\text{CEAB}}$ to A <sub>n</sub> or B <sub>n</sub>	1.5	9.0	1.5	10.0	1.5	11.0	ns
t <sub>PLZ</sub>	Output Disable Time	1.5	7.0	1.5	7.5	1.5	8.4	ns
t <sub>PHZ</sub>	$\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$ to A <sub>n</sub> or B <sub>n</sub> $\overline{\text{CEBA}}$ or $\overline{\text{CEAB}}$ to A <sub>n</sub> or B <sub>n</sub>	1.5	7.0	1.5	7.5	1.5	8.4	ns
t <sub>S</sub>	Setup Time, HIGH or LOW Data to $\overline{\text{LEXX}}$	2.5		2.5		4.0		ns
t <sub>H</sub>	Hold Time, HIGH or LOW Data to $\overline{\text{LEXX}}$	1.5		1.5		2.0		ns
t <sub>W</sub>	Pulse Width, Latch Enable, LOW	3.3		3.3		3.3		ns
t <sub>OSSL</sub>	Output to Output Skew		1.0					ns
t <sub>OSLH</sub>	(Note 6)		1.0					ns

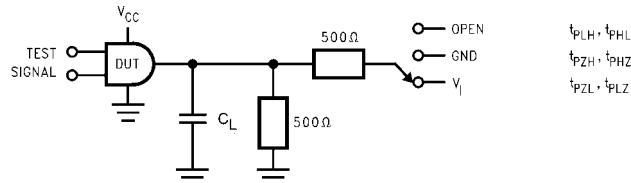
Note 6: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSSL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>).

**Dynamic Switching Characteristics**

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C	Units
				Typical	
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	3.3	0.8	V

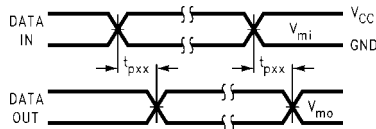
**Capacitance**

**AC LOADING and WAVEFORMS** Generic for LCX Family

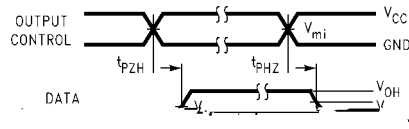


**FIGURE 1. AC Test Circuit** ( $C_L$  includes probe and jig capacitance)

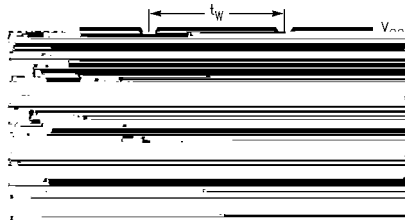
Test	Switch
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	6V at $V_{CC} = 3.3 \pm 0.3V$ $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
$t_{PZH}, t_{PHZ}$	GND



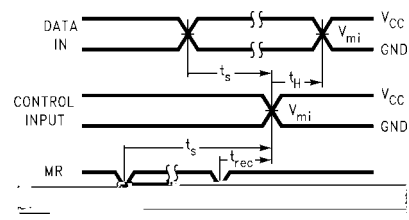
**Waveform for Inverting and Non-Inverting Functions**



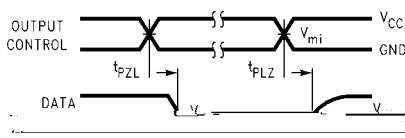
**3-STATE Output High Enable and Disable Times for Logic**



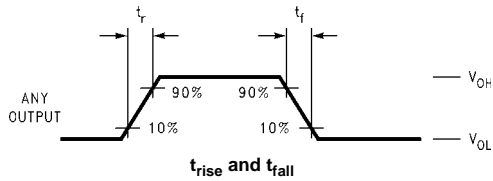
**Propagation Delay, Pulse Width and  $t_{rec}$  Waveforms**



**Setup Time, Hold Time and Recovery Time for Logic**



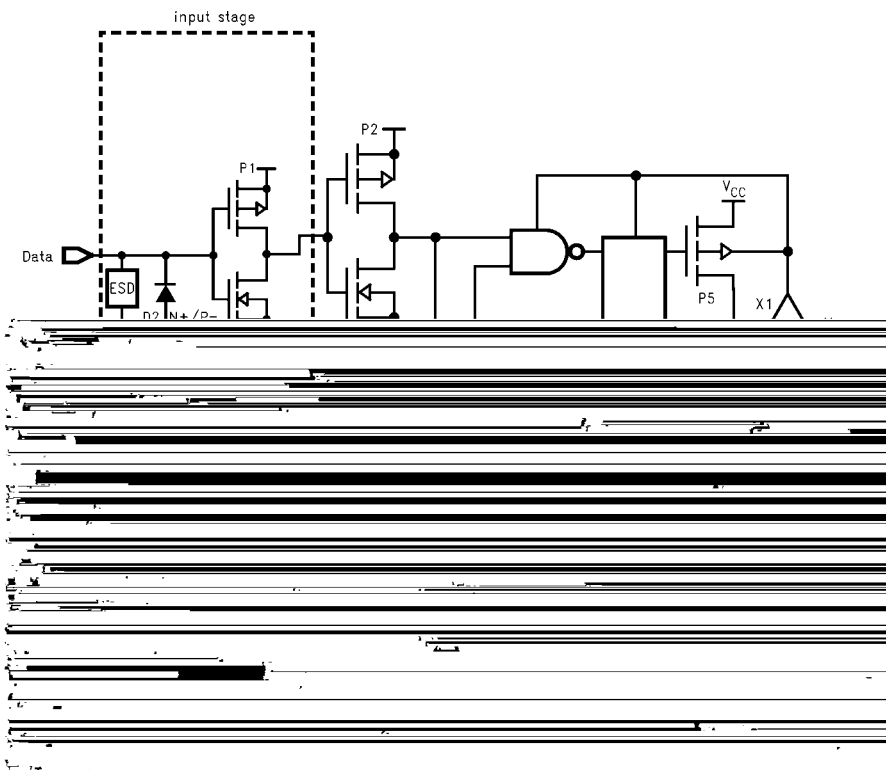
**3-STATE Output Low Enable and Disable Times for Logic**



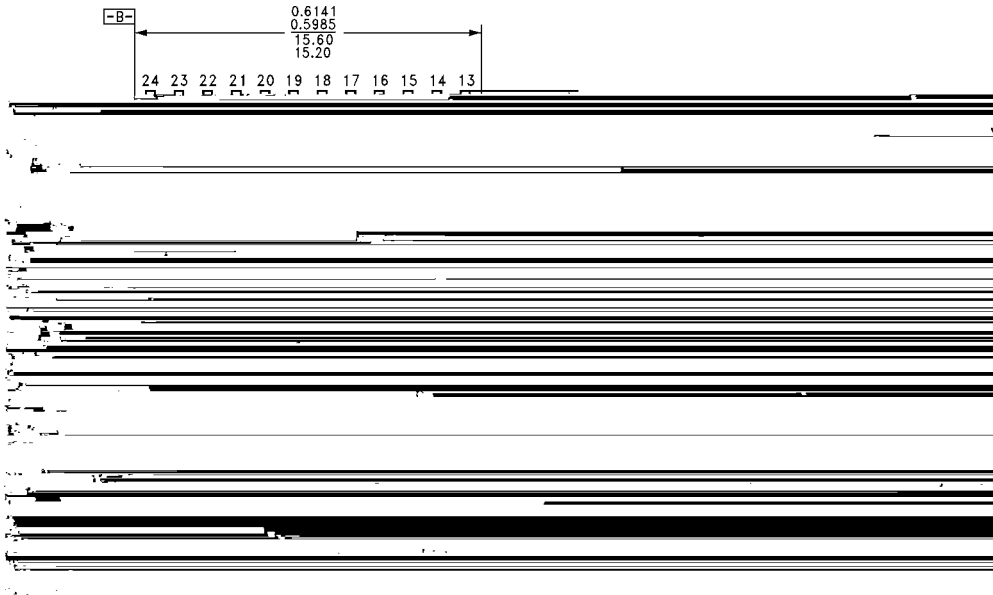
**FIGURE 2. Waveforms**  
(Input Characteristics;  $f = 1MHz, t_R = t_F = 3ns$ )

Symbol	$V_{CC}$		
	$3.3V \pm 0.3V$	2.7V	$2.5V \pm 0.2V$
$V_{mi}$	1.5V	1.5V	$V_{CC}/2$
$V_{mo}$	1.5V	1.5V	$V_{CC}/2$
$V_x$	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
$V_y$	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

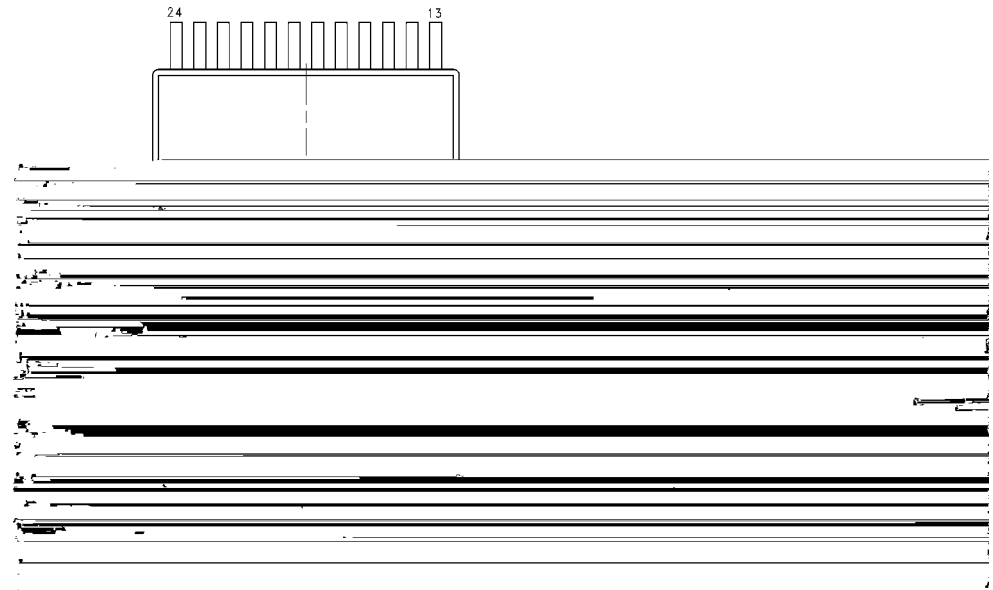
### Schematic Diagram Generic for LCX Family



**Physical Dimensions** inches (millimeters) unless otherwise noted




**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide  
Package Number M24B**



**24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide  
Package Number MSA24**



**Physical Dimensions**

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