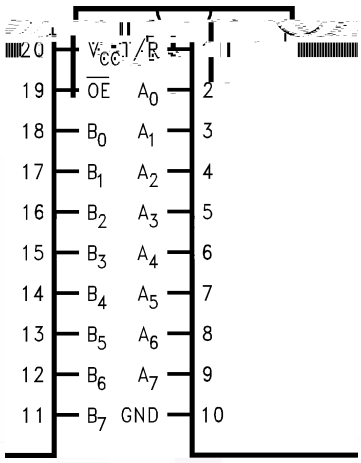
FAIRCHIL

SEMICONDUCTOR

Connection Diagram



Logic Symbol

Pin Description

Pin Names	Description
—	
/	/
A_0 A_7	A 3- A
B_0 B_7	B 3- A

Truth Table

Inputs	
OE	Outputs
=	
=	
=	
=	

Note:

2.

Logic Diagram

Absolute Maximum Ratings

Symbol	Parameter	Rating
CC	y	0.5 +7.0
	C	0.5 +7.0

Note:
3. A

Recommended Operating Conditions(4)

C

Note:
4. y y

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = –40°C to +85°C Min	Max	Units
		2.3 2.7		1.7		
		2.7 3.6		2.0		
		2.3 2.7			0.7	
		2.7 3.6			0.8	
		2.3 3.6	= 100 A	CC 0.2		
		2.3	= 4 A	1.8		
		2.7	= 4 A	2.2		
		3.0	= 6 A	2.4		
		2.7	= 8 A	2.0		
		3.0	= 12 A	2.0		
		2.3 3.6	= 100 A		0.2	
		2.3	= 4 A		0.6	
		2.7	= 4 A		0.4	
		3.0	= 6 A		0.55	
		2.7	= 8 A		0.6	
		3.0	= 12 A		0.8	
	C	2.3 3.6	0 ≤ ≤ 5.5		5.0	A
3-	A /	2.3 3.6	0 ≤ ≤ 5.5 , =		5.0	A
	- C	0	= 5.5		10	A
CC	y C	2.3 3.6	= CC		10	A
		2.3 3.6	3.6 ≤ , ≤ 5.5 (5)		10	
Δ_{CC}	CC	2.3 3.6	= CC 0.6		500	A

Note:

5. 3- A y.

AC Electrical Characteristics

T_A

Symbol	Parameter

Note:

6. y y - ( ). - ( ).

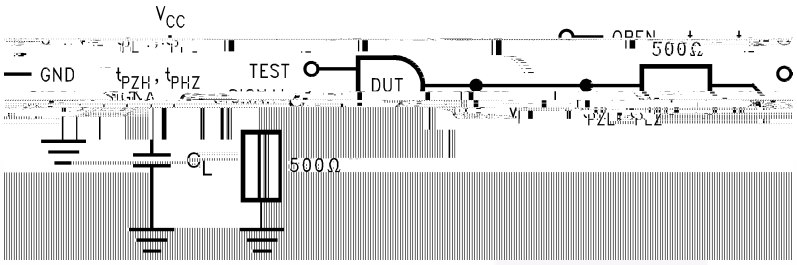
Dynamic Switching Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = 25°C Typical	Unit
	y	3.3	C = 50 , = 3.3 , = 0	0.5	
		2.5	C = 30 , = 2.5 , = 0	0.4	
	y y	3.3	C = 50 , = 3.3 , = 0	0.5	
		2.5	C = 30 , = 2.5 , = 0	0.4	

Capacitance

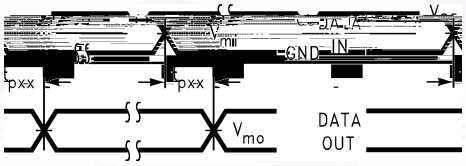
Symbol	Parameter	Conditions	Typical	Units
C	C	CC = , = 0 CC	7	
C	C	CC = 3.3 , = 0 CC	8	
C	C	CC = 3.3 , = 0 CC = 10	25	

AC Loading and Waveforms (C y)

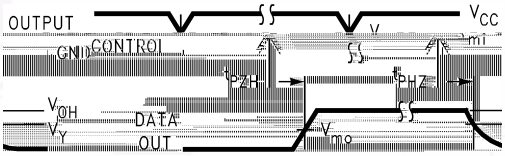


Test	Switch
,	
,	6 CC = 3.3 ± 0.3 CC 2 CC = 2.5 ± 0.2
,	

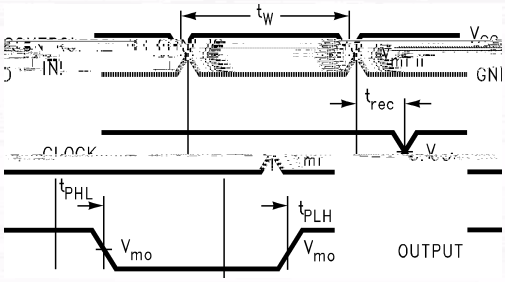
Figure 1. AC Test Circuit (C_L includes probe and jig capacitance)



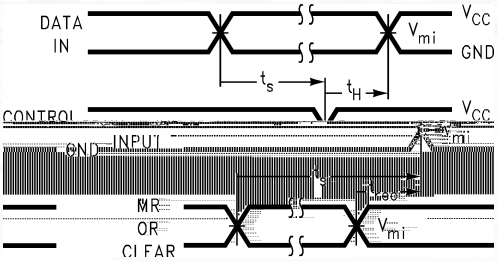
Waveform for Inverting and Non-Inverting Functions



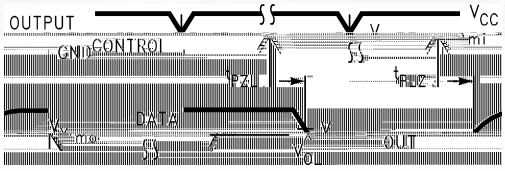
3-STATE Output High Enable and Disable Times for Logic



Propagation Delay. Pulse Width and t_{rec} Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic

t_{rise} and t_{fall}

Figure 2. Waveforms (Input Characteristics; f = 1MHz, $t_r = t_f$ = 3ns)

Physical Dimensions

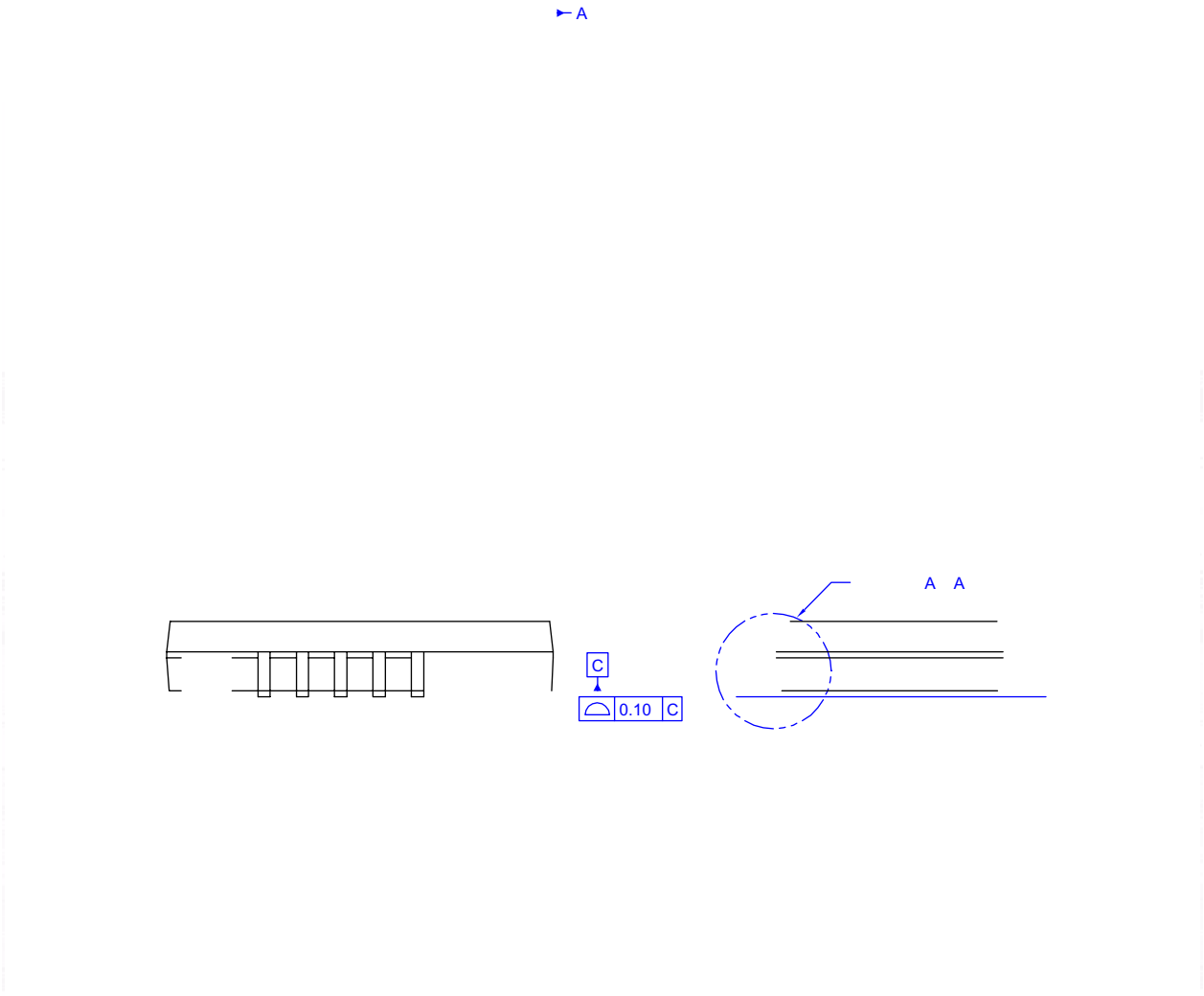


Figure 3. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

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Physical Dimensions (C)

Figure 5. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide

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Physical Dimensions (C)

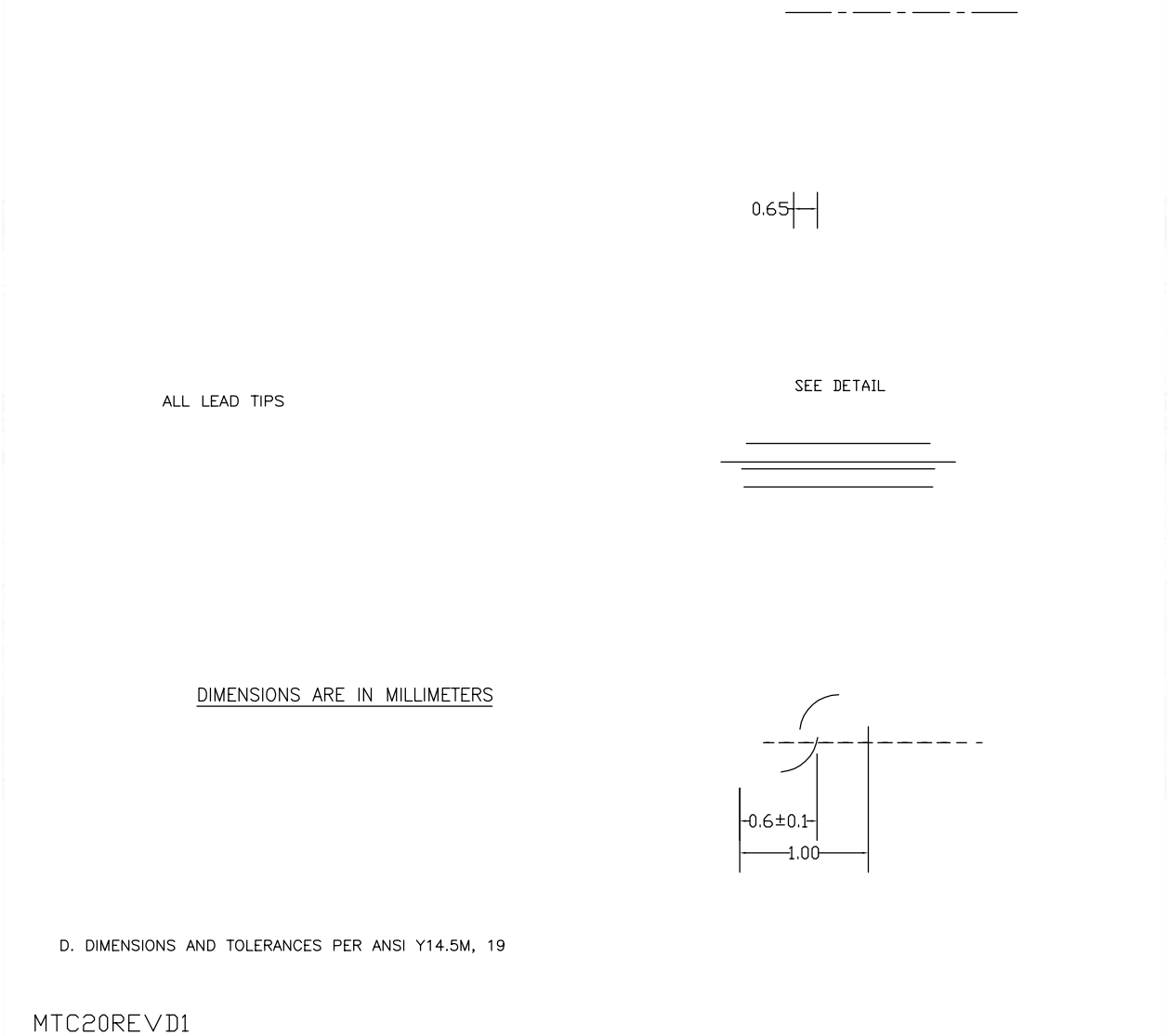

Figure 6. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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