FAIRCHILD
SEMICONDUCTOR

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Revised   20

74LVT16374 • 74LVTH16374
Low Voltage 16-Bit D-Type Flip-Flop
with 3-STATE Outputs

General Description

Connection Diagrams

Pin Assignment for SSOP and TSSOP

Pin Descriptions

FBGA Pin Assignments

Truth Tables

Pin Assignment for FBGA

(Top Thru View)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance
O_o = Previous O_o before HIGH to LOW of CP

Functional Description

The LVTTeipti.6 (I.5ipt)1(i)-3on1.4.5ipt(i)-3t33.19 Tc722.21.17 nd1.1 (e)1.4.5ipt LTIilignmergnililiignmeloit.olilgniilreililiS710s8 (.o)-3aith A8 (V(i)-2

Absolute Maximum Ratings(Note 3)

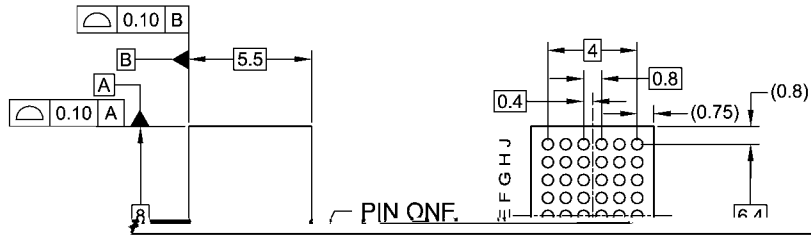| Symbol	Parameter	Value	Conditions	Units
V_{CC}				

V_{CC}

Recommended Operating Conditions

Note 3: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

**Note 4:** I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_CC (V)	T_A 40qC to 85qC Min	Max	Units	Conditions
I_CCH	Power Supply Current	3.6		0.19	mA	Outputs HIGH
I_CCL	Power Supply Current	3.6		5	mA	Outputs LOW
I_CCZ	Power Supply Current	3.6		0.19	mA	Outputs Disabled
I_CCZ	Power Supply Current	3.6		0.19	mA	V_{CC} d V_O d 5.5V, Outputs Disabled
'I_CC	Increase in Power Supply Current	3.6				

Note 5: Applies to bushold versions only (74LVTH16374).

Note 6: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 7: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 8: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 9)

Note 9: Characterized in SSOP package. Guaranteed parameter, but not tested.

Note 10: Max number of outputs defined as (n). n−1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

Note 11: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Capacitance (Note 12)

Note 12: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

Physical Dimensions inches (millimeters) unless otherwise noted

54-Ball Fine Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA54A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

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          0.620 – 0.630
          [15.75 – 16.00]
            – A –
48                              25
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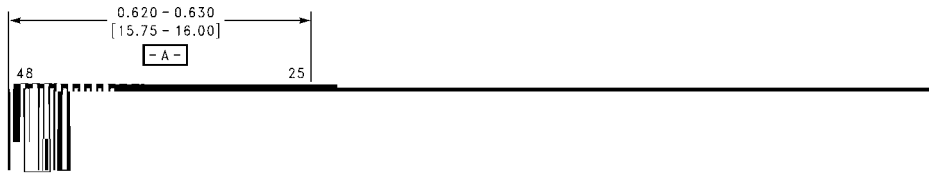
48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

LAND PATTERN RECOMMENDATION
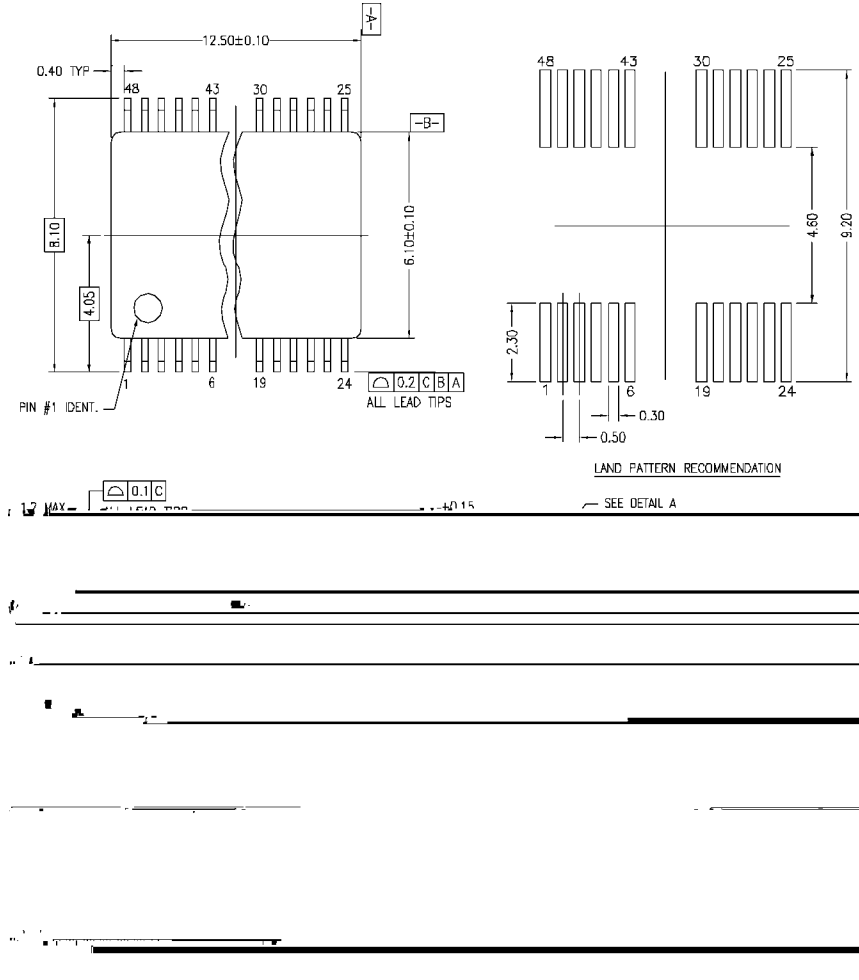
48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

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