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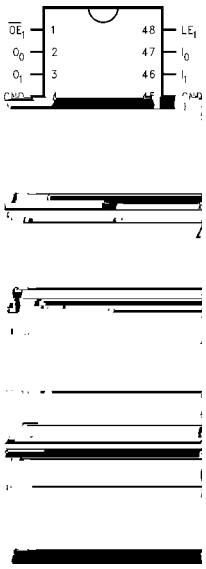
January 2000

## Connection Diagram



## Truth Tables

| Inputs | | | Outputs |
|---|---|---|---|
| $LE_1$ | $\overline{OE}_1$ | $I_0$–$I_7$ | $O_0$–$O_7$ |
| X | H | X | Z |
| H | L | L | L |
| H | L | H | H |
| L | L | X | $O_0$ |

| Inputs | | | |
|---|---|---|---|
| $LE_2$ | $\overline{OE}_2$ | $I_8$–$I_{15}$ | $O_8$–$O_{15}$ |
| X | H | X | Z |
| H | | | |
| H | L | | H |
| | L | X | $O_0$ |

H HIGH Voltage Level

L Voltage Level

(High or LOW, inputs may not float)

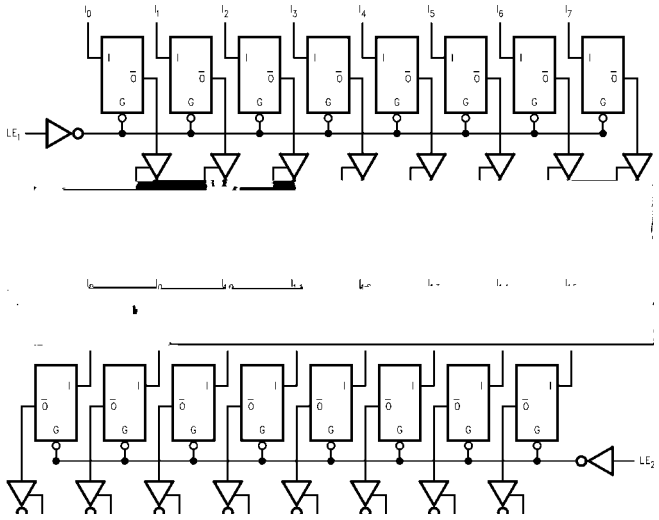
High Impedance

Previous $O_0$ before HIGH-to-LOW of Latch Enable

## Functional Description

The 74VCX162373 contains sixteen edge-triggered D-type latches with 3-STATE outputs. The device is byte controlled with each byte functioning identically but independently of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable ($LE_n$) input is HIGH, data on the $I_n$ enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its I input changes. When $LE_n$ is LOW, the latches store information that was present on the I inputs a setup time preceding the HIGH-to-LOW transition on $LE_n$. The 3-STATE outputs are controlled by the Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is LOW the standard outputs are in the 2-state mode. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 2)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | 0.5V to 4.6V |
| DC Input Voltage ($V_I$) | 0.5V to 4.6V |
| Output Voltage ($V_O$) | |
| Outputs 3-STATED | 0.5V to 4.6V |
| Outputs Active (Note 3) | 0.5V to $V_{CC}$ 0.5V |
| DC Input Diode Current ($I_{IK}$) $V_I$ 0V | 50 mA |
| DC Output Diode Current ($I_{OK}$) | |
| $V_O$ 0V | 50 mA |
| $V_O$ $V_{CC}$ | 50 mA |
| DC Output Source/Sink Current ($I_{OH}/I_{OL}$) | 50 mA |
| DC $V_{CC}$ or GND Current per Supply Pin ($I_{CC}$ or GND) | 100 mA |
| Storage Temperature Range ($T_{STG}$) | 65 C to 150 C |

## Recommended Operating Conditions (Note 4)

| | |
|---|---|
| Power Supply | |
| Operating | 1.4V to 3.6V |
| Input Voltage | 0.3V to074 Tc - 623450034 Tc 034 Tc.961 0 0 6.96267 |

**Note 2:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 3:** $I_O$ Absolute Maximum Rating must be observed.

**Note 4:** Floating or unused inputs must be held HIGH or LOW.

## DC Electrical Characteristics

## DC Electrical Characteristics (Continued)

| Symbol | Parameter | Conditions | | $V_{CC}$ (V) | Min | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OL}$ | LOW Level Output Voltage | $I_{OL}$ | 100 PA | 2.7 - 3.6 | | 0.2 | |
| | | $I_{OL}$ | 6 mA | 2.7 | | 0.4 | |
| | | $I_{OL}$ | 8 mA | 3.0 | | 0.55 | |
| | | $I_{OL}$ | 12 mA | 3.0 | | 0.8 | |
| | | $I_{OL}$ | 100 PA | 2.3 - 2.7 | | 0.2 | |
| | | $I_{OL}$ | 6 mA | 2.3 | | 0.4 | V |
| | | $I_{OL}$ | 8 mA | 2.3 | | 0.6 | |
| | | $I_{OL}$ | 100 PA | 1.65 - 2.3 | | 0.2 | |
| | | $I_{OL}$ | 3 mA | 1.65 | | 0.3 | |
| | | $I_{OL}$ | 100 PA | 1.4 - 1.6 | | 0.2 | |
| | | $I_{OL}$ | 1 mA | 1.4 | | 0.35 | |
| $I_I$ | Input Leakage Current | 0 d $V_I$ d 3.6V | | 1.4 - 3.6 | | r5.0 | PA |
| $I_{OZ}$ | 3-STATce368 _ce36728 0 Td6Obce833 517.41 Tm (I)Tj 0.0036 Tc -0.0016 Tw 6 0 0 6 153.69 5163m (I)Tj 6 0 0 9.453.69 508.8901 Tm ( )Tj /T3_0 1 Tf 0.28 0 Td (d)Tj /T1_0 | | | | | | |

**Note 5:** Outputs disabled or 3-STATE only.

## AC Electrical Characteristics (Note 6)

## AC Electrical Characteristics (Continued)

| Symbol | Parameter | Conditions | $V_{CC}$ | T |
|---|---|---|---|---|

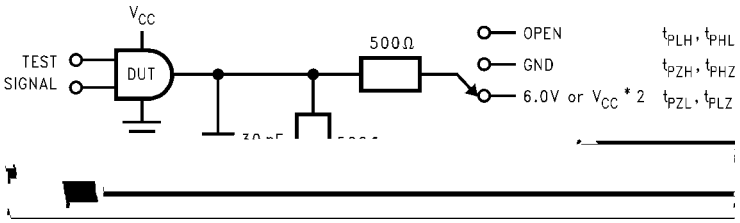
**Note 6:** For $C_L$ $50_P$F, add approximately 300 ps to the AC maximum specification.

**Note 7:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ($t_{OSHL}$) or LOW-to-HIGH ($t_{OSLH}$).

## Dynamic Switching Characteristics

## Capacitance

## AC Loading and Waveforms ($V_{CC}$ 3.3V 0.3V to 1.8V 0.15V)




| TEST | SWITCH |
|---|---|
| $t_{PLH}$, $t_{PHL}$ | Open |
| $t_{PZL}$, $t_{PLZ}$ | 6V at $V_{CC}$ 3.3 0.3V;<br>$V_{CC}$ x 2 at $V_{CC}$ 2.5 0.2V; 1.8V 0.1 V |
| $t_{PZH}$, $t_{PHZ}$ | GND |

**FIGURE 1. AC Test Circuit**

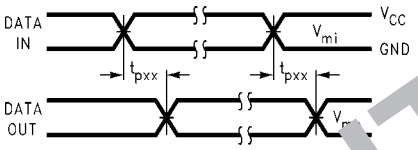



**FIGURE 2. Waveform for Inv g and Non-Inverting Functio**


**FIGURE 3. 3-STATE Output HIGH Enable and Disable Times for Low Voltage Logic**

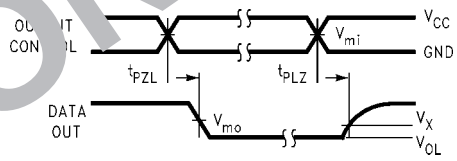



**FIGURE 4. 3-STATE Output LOW Enable and Disable Times for Low Voltage Logic**

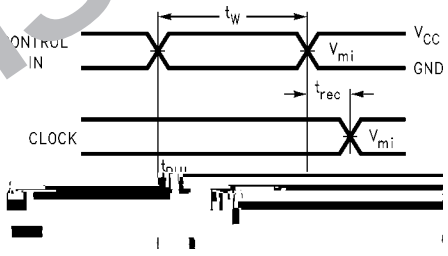



**FIGURE 5. Propagation Delay, Pulse Width and $t_{REC}$ Waveforms**

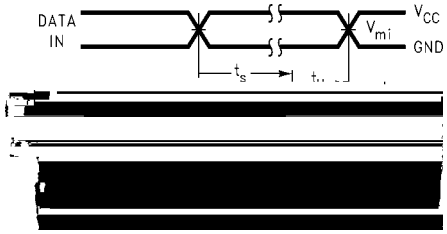



**FIGURE 6. Setup Time, Hold Time and Recovery Time for Low Voltage Logic**

| Symbol | $V_{CC}$ | | |
|---|---|---|---|
| | 3.3V 0.3V | 2.5V 0.2V | 1.8V 0.15V |
| $V_{mi}$ | 1.5V | $V_{CC}/2$ | $V_{CC}/2$ |
| $V_{mo}$ | 1.5V | $V_{CC}/2$ | $V_{CC}/2$ |
| $V_X$ | $V_{OL}$ 0.3V | $V_{OL}$ 0.15V | $V_{OL}$ 0.15V |
| $V_Y$ | $V_{OH}$ 0.3V | $V_{OH}$ 0.15V | $V_{OH}$ 0.15V |

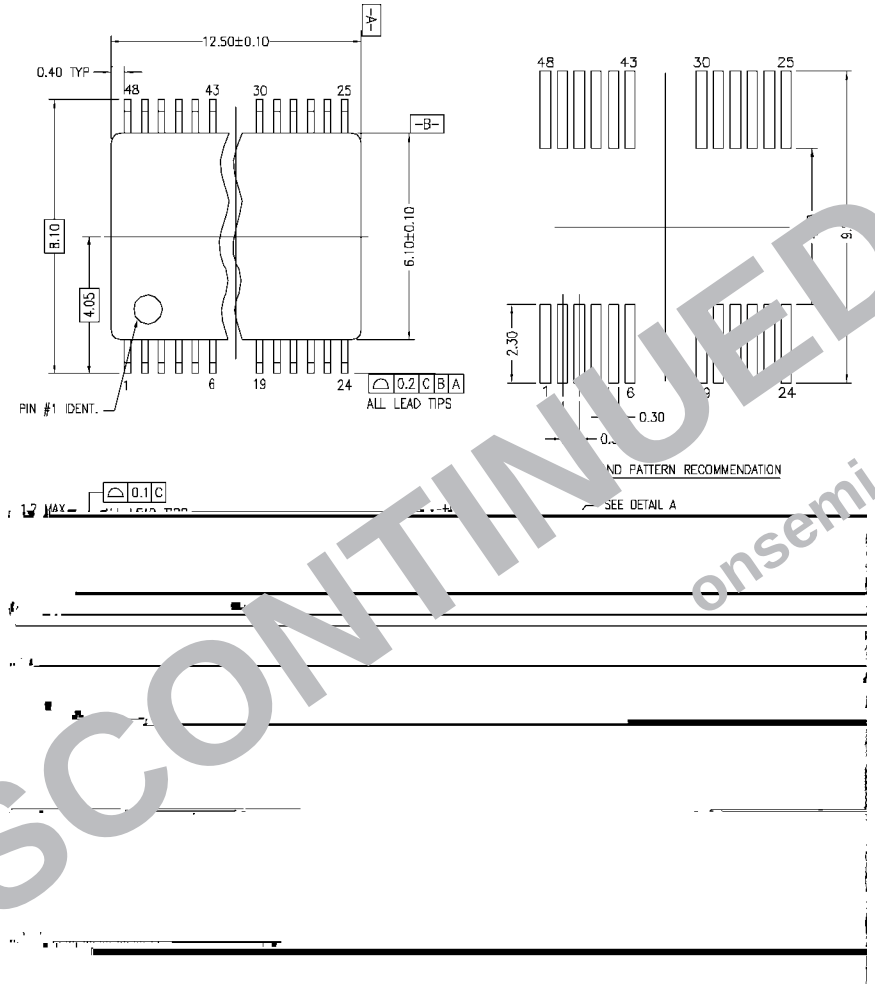
## AC Loading and Waveforms ($V_{CC}$ 1.5V 0.1V)

**FIGURE 7. AC Test Circuit**

**FIGURE 8. Waveform for Inverting and Non-Inverting Functions**

**FIGURE 9. 3-STATE Output HIGH Enable and**

## Physical Dimensions inches (millimeters) unless otherwise noted




**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide**
**Package Number MTD48**