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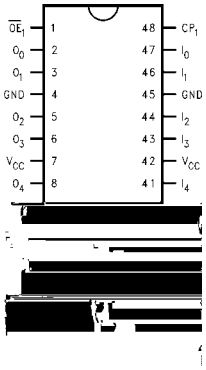
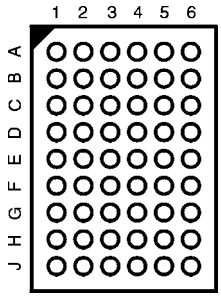
October 1997
Revised June 2005

Connection Diagrams

Pin Assignment for TSSOP



Pin Assignment for FBGA



(Top Thru View)

Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
CP_n	Clock Pulse Tf 1.03013 Tc -0.00002 Tc -0.0111 p3013 T03013 Tt2.467 -1.28

FBGA Pin Assignments

Truth Tables

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs may not float)
Z = High Impedance
O_0 = Previous O_0 before HIGH-to-LOW of CP

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7 - 3.6		0.2	
		I_{OL} = 12 mA	2.7		0.4	
		I_{OL} = 18 mA	3.0		0.4	
		I_{OL} = 24 mA	3.0		0.55	
		I_{OL} = 100 μA	2.3 - 2.7		0.2	
		I_{OL} = 12 mA	2.3		0.4	V
		I_{OL} = 18 mA	2.3		0.6	
		I_{OL} = 100 μA	1.65 - 2.3		0.2	
		I_{OL} = 6 mA	1.65		0.3	
		I_{OL} = 100 μA	1.4 - 1.6		0.2	
		I_{OL} = 2 mA	1.4		0.35	
		I_{OL} = 100 μA	1.2		0.05	
I_I	Input Leakage Current	0 ≤ V_I ≤ 3.6V	1.2 - 3.6		±5.0	μA
I_{OZ}	3-STATE Output Leakage	0 ≤ V_O ≤ 3.6V V_I = V_{IH} or V_{IL}	1.2 - 3.6		±10	μA
I_{OFF}	Power-OFF Leakage Current	0 ≤ (V_I, V_O) ≤ 3.6V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	1.2 - 3.6		20	μA
		V_{CC} ≤ (V_I, V_O) ≤ 3.6V (Note 7)	1.2 - 3.6		±20	
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7 - 3.6		750	μA

Note 7: Outputs disabled or 3-STATE only.

AC Electrical Characteristics (Note 8)

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C Min	Max	Units	Figure Number
f_{MAX}	Maximum Clock Frequency	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	250			Figures 1, 2
			2.5 ± 0.2	200			
			1.8 ± 0.15	100		ns	
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1	80			Figures 7, 8
			1.2	40			
t_{PHL}, t_{PLH}	Propagation Delay CP to O_n	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	0.8	3.0		Figures 1, 2
			2.5 ± 0.2	1.0	3.9		
			1.8 ± 0.15	1.5	7.8	ns	
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1	1.0	15.6		Figures 7, 8
			1.2	1.5	39		
t_{PZL}, t_{PZH}	Output Enable Time	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	0.8	3.5		Figures 1, 3, 4
			2.5 ± 0.2	1.0	4.6		
			1.8 ± 0.15	1.5	9.2	ns	
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1	1.0	18.4		Figures 7, 9, 10
			1.2	1.5	46		
t_{PLZ}, t_{PHZ}	Output Disable Time	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	0.8	3.5		Figures 1, 3, 4
			2.5 ± 0.2	1.0	3.8		
			1.8 ± 0.15	1.5	6.8	ns	
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1	1.0	13.6		Figures 7, 9, 10
			1.2	1.5	34		
t_S	Setup Time	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	1.8			

AC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$ Min	Max	Units	Figure Number
t_H	Hold Time	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 1.0	1.0			
			2.5 ± 0.2	1.0			Figures 1, 6
			1.8 ± 0.15	1.0		ns	
		$C_L = 15$ pF, $R_L = 2k\Omega$	1.5 ± 0.1	2.0			Figures 6, 7
			1.2	6			
t_W	Pulse Width	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 0.3	1.5			
			2.5 ± 0.2	1.5			Figures 1, 4
			1.8 ± 0.15	4.0		ns	

C_L = 0 Td (r)Tj /T1_0 1 Tf 0.002 Tc 0.56 0 Td1 Td8.85 Tm ( )Tj / Tm ( )Tj /T3_ J4e/ (i)20 (m)31 (e)TJ 15.84 0 Td (C)Tj 0 Tc 0 Tw 4.8 0 0

t

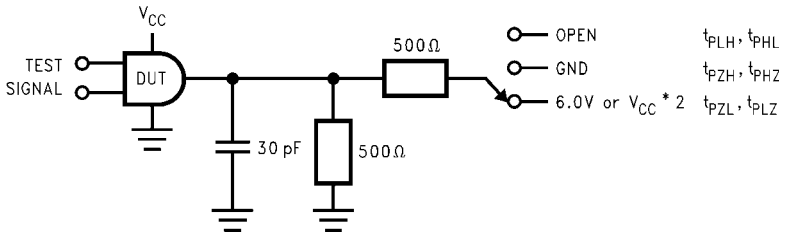
Note 8: For $C_L = 50_P$F, add approximately 300 ps to the AC maximum specification.

Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Capacitance

AC Loading and Waveforms (V_{CC} 3.3V ± 0.3V to 1.8V ± 0.15V)



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3V ± 0.3V; V_{CC} x 2V at V_{CC} = 2.5V ± 0.2V; 1.8V ± 0.15V
t_{PZH}, t_{PHZ}	GND

FIGURE 1. AC Test Circuit

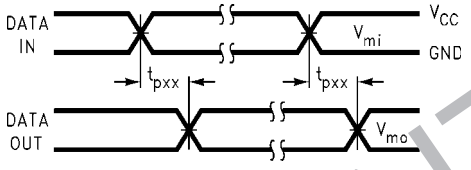


FIGURE 2. Waveform for Inverting and Non-Inverting Functions

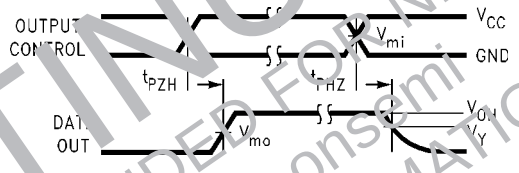


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

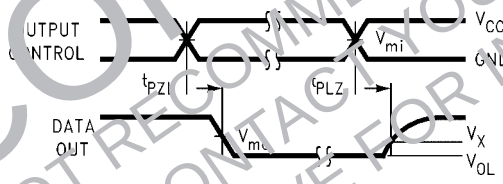


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

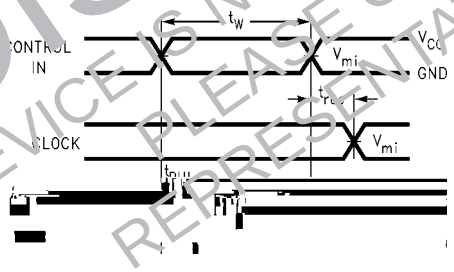


FIGURE 5. Propagation Delay, Pulse Width and t_{rec} Waveforms

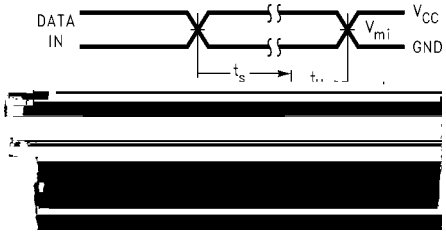


FIGURE 6. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

Symbol	V_{CC}		
	3.3V ± 0.3V	2.5V ± 0.2V	1.8V ± 0.15V
V_{mi}	1.5V	V_{CC}/2	V_{CC}/2
V_{mo}	1.5V	V_{CC}/2	V_{CC}/2
V_X	V_{OL} + 0.3V	V_{OL} + 0.15V	V_{OL} + 0.15V
V_Y	V_{OH} − 0.3V	V_{OH} − 0.15V	V_{OH} − 0.15V

AC Loading and Waveforms (V_{CC} 0.15V $\pm$ 0.1V to 1.2V)

TEST **SWITCH**

t

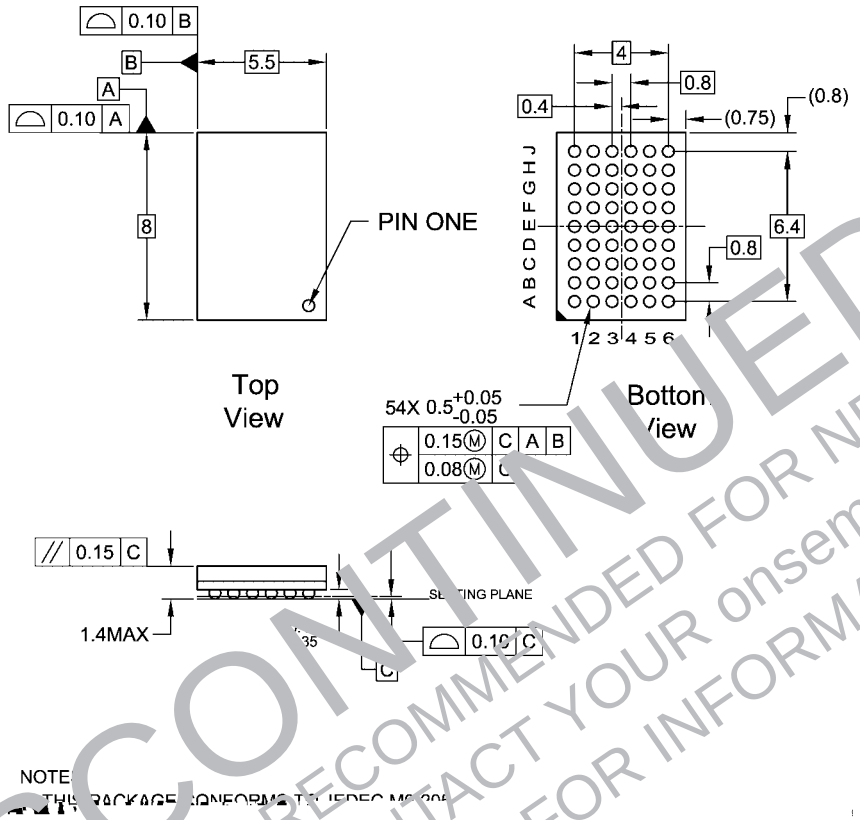
FIGURE 7. AC Test Circuit

FIGURE 8. Waveform for Inverting and Non-Inverting Functions

FIGURE 9. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

FIGURE 10. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

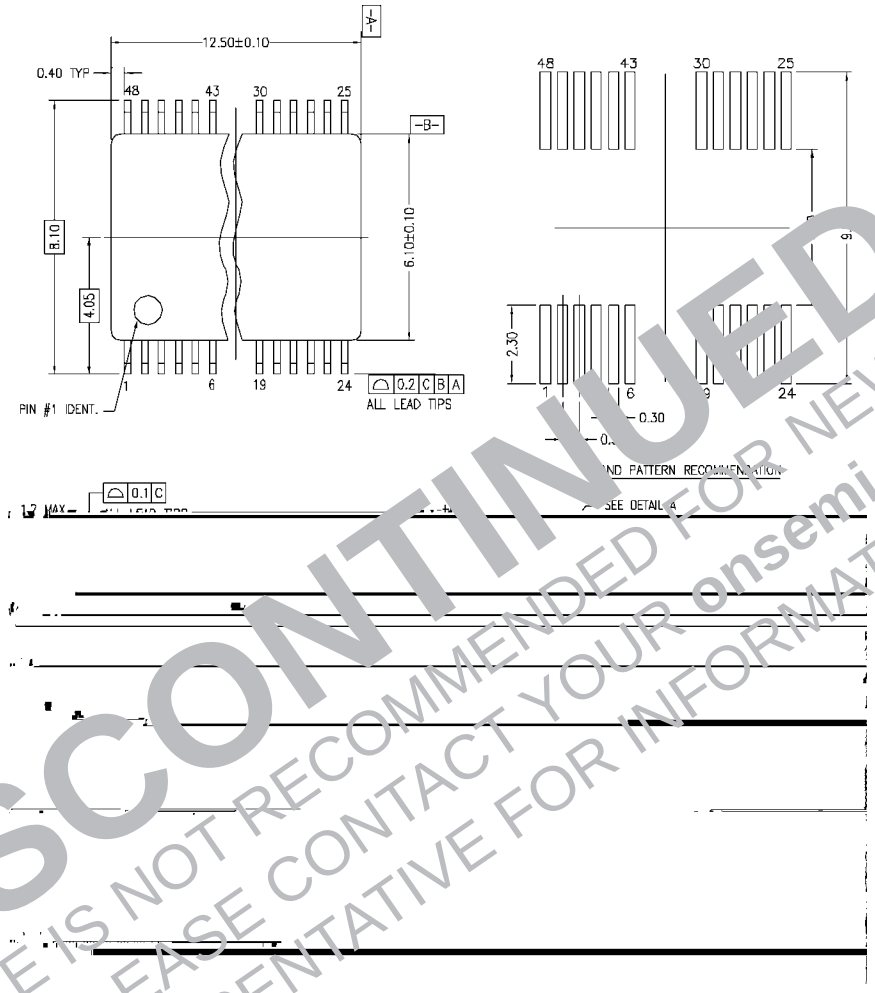
Physical Dimensions inches (millimeters) unless otherwise noted



NOTE

54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA54A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Body Width
Package Number MTD48

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