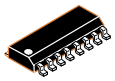
2-I M I

74 HC157



The VHC157 is an advanced high speed CMOS Quad 2−Channel Multiplexer fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It consists of four 2−input digital multiplexers with common select and enable inputs. When the $\overline{\text{ENABLE}}$ input is held “H” level, selection of data is inhibited and all the outputs become “L” level. The SELECT decoding determines whether the I 0x or I 1x inputs get routed to their corresponding outputs.

An Input protection circuit ensures that 0 V to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and on two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

- High Speed: t_{PD} = 4.1 ns (Typ.) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 4 μA (Max.) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Source 1 Data Inputs
- Enable Input
- mismatc85.0394 01 T46728 602.476 0 ou voltPIN DESCRIPTIONad 2.00q6ip0ding0 0593cmp0dinndc06.693 0 lbS6ip0ding

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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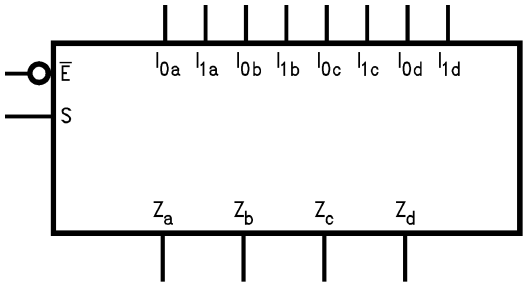
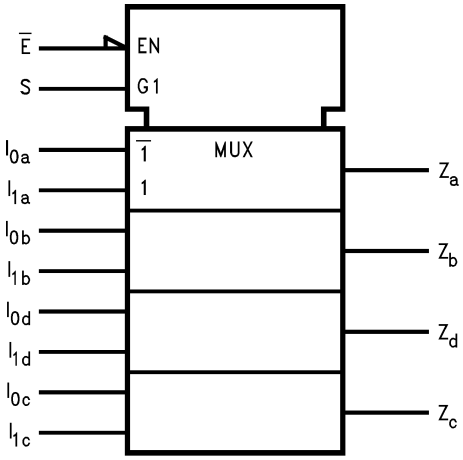
Publication Order Number:





—				
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

The VHC157 is a quad 2−input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active− LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The VHC157 is the logic implementation of a 4−pole, 2−position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

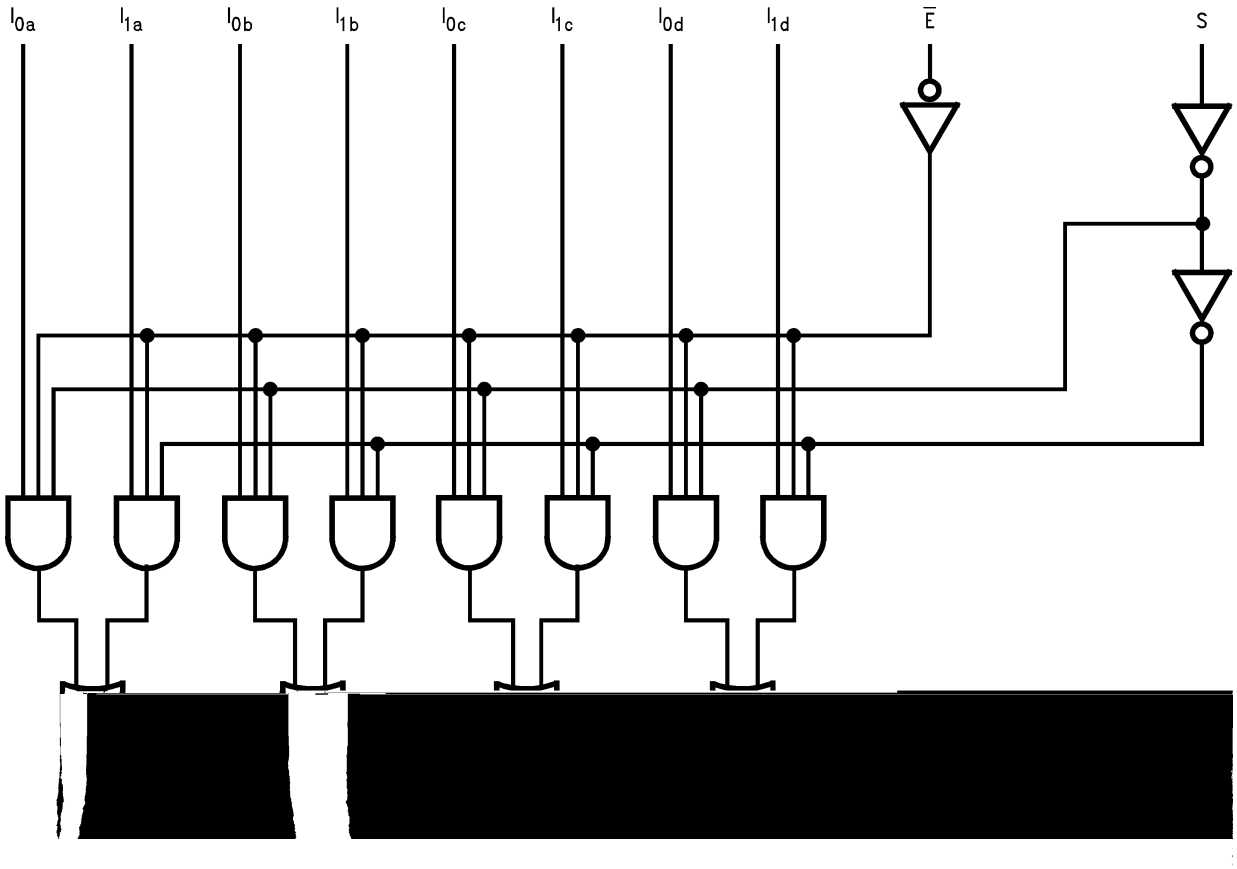
$Z_a = \overline{E} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$

$Z_b = \overline{E} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$

$Z_c = \overline{E} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$

$Z_d = \overline{E} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$

A common use of the VHC157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The VHC157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

V_{CC}	DC Supply Voltage	0.5 to +6.5	V
V_{IN}	DC Input Voltage	0.5 to +6.5	V
V_{OUT}	DC Output Voltage	0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
I_{IK}	Input Clamp Current	20	mA
I_{OK}	Output Clamp Current	±20	mA
T_{STG}	Storage Temperature Range	65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs	260	°C
T_J	Junction Temperature Under Bias	+150	°C
θ_{JA}	Thermal Resistance (Note 2) SOIC 16 QFN16 TSSOP 16	126 118 159	°C/W
P_D			

		°			°	°	
	2.0 3.0 5.5	1.50 0.7 x V_{CC}			1.50 0.7 x V_{CC}		V
	2.0 3.0 5.5			0.50 0.3 x V_{CC}		0.50 0.3 x V_{CC}	V
A	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
A A	3.0 4.5	2.58 3.94			2.48 3.80		
	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
	3.0 4.5			0.36 0.36		0.44 0.44	
	0 5.5			±0.1		±1.0	µA
	5.5			4.0		40.0	µA

			°		
(Note 3)	CL = 50 pF	5.0	0.3	0.8	V

(continued)

				°			° °	
C_{IN}	Input Capacitance	V_{CC} = Open			4	10		

CASE 485AW
ISSUE O

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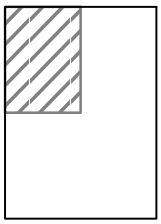
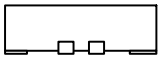




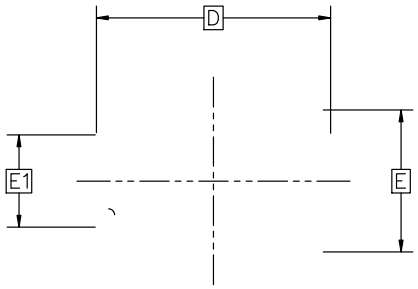
SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.1[illegible]

nm TOTAL IN EXCESS OF THE

b DIMENSION AT MAXIMUM MATE

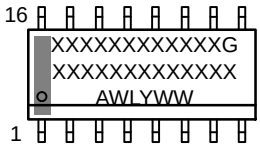


TOP VIEW

SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

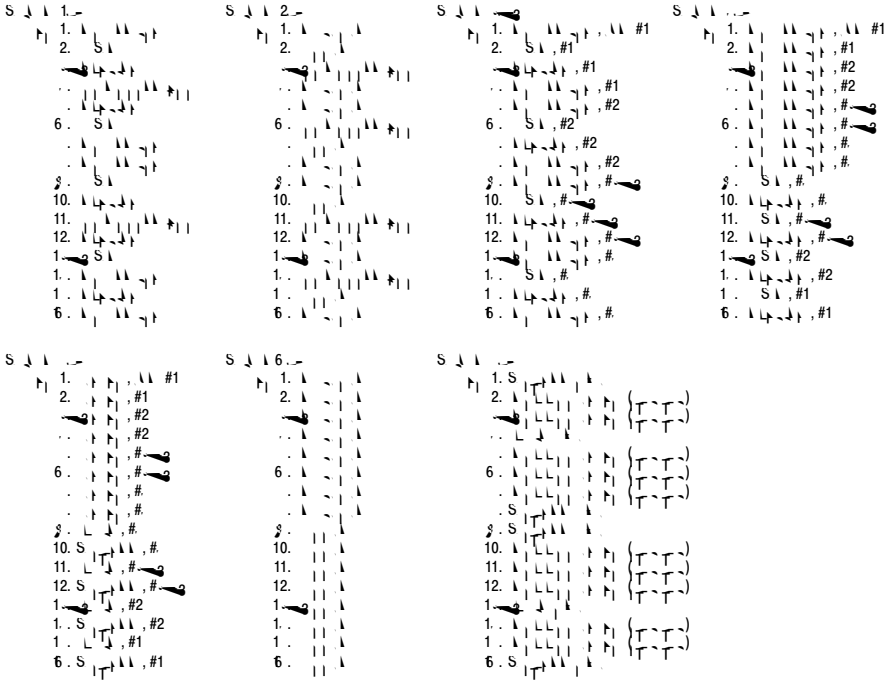
DATE 18 OCT 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



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DESCRIPTION:	**SOIC−16 9.90X3.90X1.37 1.27P**		**PAGE 2 OF 2**

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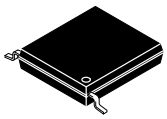

SCALE 2:1

TSSOP−16 WB
CASE 948F
ISSUE B

DATE 19 OCT 2006

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