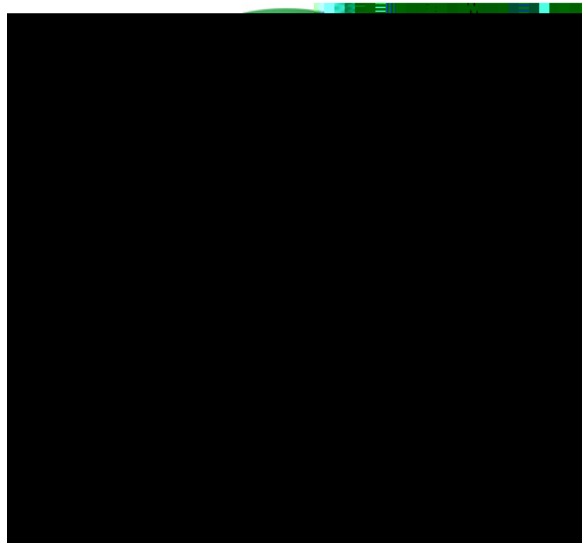




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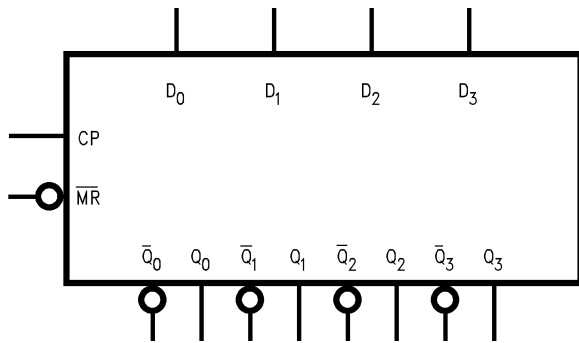


74VHC175

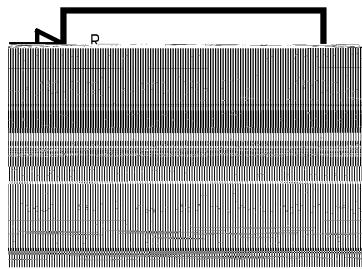


74VHC175 Quad D-Type Flip-Flop

Logic Symbol



IEEE/IEC



Functional Description

The VHC175 consists of four edge-triggered D flip-flops with individual D inputs and Q and \bar{Q} outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and \bar{Q} outputs to follow. A LOW input on the Master Reset (\bar{MR}) will force all Q outputs LOW and \bar{Q} outputs HIGH independent of Clock or Data inputs. The VHC175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

Truth Table

H = HIGH Voltage Level

L = LOW Voltage Level

t_n = Bit Time before Clock Pulse

t_{n+1} = Bit Time after Clock Pulse

Logic Diagram

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended.

DC Electrical Characteristics

Noise Characteristics

Note:

2. Parameter guaranteed by design.

Physical Dimensions

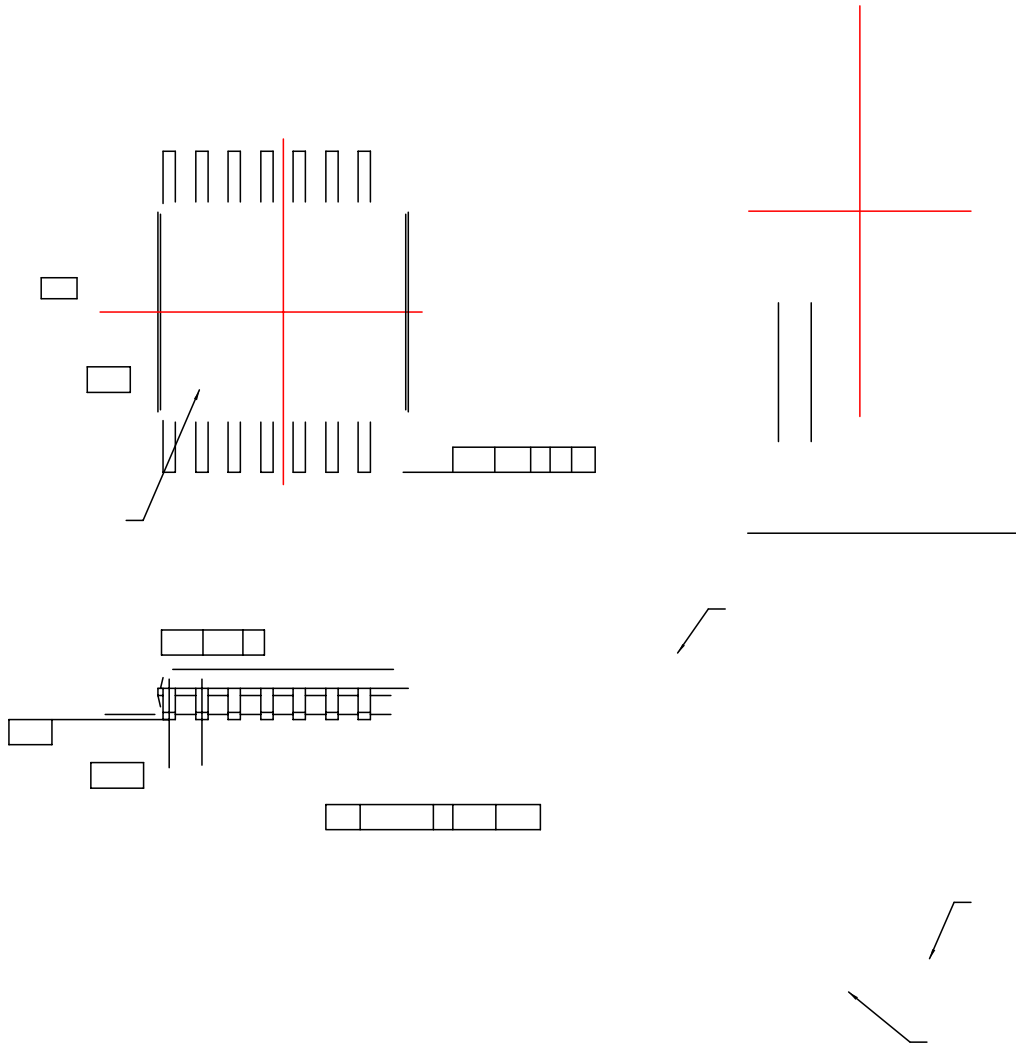
Dimensions are in millimeters unless otherwise noted.



Figure 1. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



**Figure 3. 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16**



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