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74VHCT573A
Octal D-Type Latch with 3-STATE Outputs

Features

■ High speed: $t_{PD} = 7.7$ns (Typ.) at $T_A =$

Logic Symbol

IEEE/IEC

Functional Description

The VHCT573A contains eight D-type latches with 3-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs, a setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are enabled. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode, but, this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
$\overline{OE}$	LE	D	O_n
L	H	H	H
L	H	L	L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

Logic Diagram

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Recommended Operating Conditions[5]

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Notes:

2. HIGH or LOW state. I_{OUT} absolute maximum rating must be observed.

3. When outputs are in OFF-State or when V_{CC} = 0V.

4. V_{OUT} < GND, V_{OUT} > V_{CC} (Outputs Aj /i84e Outputs Aj /i84e

DC Electrical Characteristics

Symbol	Parameter	V$_{CC}$ (V)	Conditions		T$_A$ = 25°C			T$_A$ = −40°C to +85°C		Units
					Min.	Typ.	Max.	Min.	Max.	
V$_{IH}$	HIGH Level Input Voltage	4.5			2.0			2.0		V
		5.5			2.0			2.0		
V$_{IL}$	LOW Level Input Voltage	4.5					0.8		0.8	V
		5.5					0.8		0.8	
V$_{OH}$	HIGH Level Output Voltage	4.5	V$_{IN}$ = V$_{IH}$ or V$_{IL}$	I$_{OH}$ = −50µA	4.40	4.50		4.40		V
				I$_{OH}$ = −8mA	3.94			3.80		
V$_{OL}$	LOW Level Output Voltage	4.5	V$_{IN}$ = V$_{IH}$ or V$_{IL}$	I$_{OL}$ = 50µA		0.0	0.1		0.1	V
				I$_{OL}$ = 8mA			0.36		0.44	
I$_{OZ}$	3-STATE Output Off-State Current	5.5	V$_{IN}$ = V$_{IH}$ or V$_{IL}$, V$_{OUT}$ = V$_{CC}$ or GND				±0.25		±2.5	µA
I$_{IN}$	Input Leakage Current	0–5.5	V$_{IN}$ = 5.5V or GND				±0.1		±1.0	µA
I$_{CC}$	Quiescent Supply Current	5.5	V$_{IN}$ = V$_{CC}$ or GND				4.0		40.0	µA
I$_{CCT}$	Maximum I$_{CC}$/Input	5.5	V$_{IN}$ = 3.4V, Other Inputs = V$_{CC}$ or GND				1.35		1.50	mA
I$_{OFF}$	Output Leakage Current (Power Down State)	0.0	V$_{OUT}$ = 5.5V				0.5		5.0	µA

Noise Characteristics

Symbol	Parameter	V$_{CC}$ (V)	Conditions	T$_A$ = 25°C		Units
				Typ.	Limits	
V$_{OLP}$[6]	Quiet Output Maximum Dynamic V$_{OL}$	5.0	C$_L$ = 50pF	1.2	1.6	V
V$_{OLV}$[6]	Quiet Output Minimum Dynamic V$_{OL}$	5.0	C$_L$ = 50pF	−1.2	−1.6	V
V$_{IHD}$[6]	Minimum HIGH Level Dynamic Input Voltage	5.0	C$_L$ = 50pF		2.0	V
V$_{ILD}$[6]	Maximum LOW Level Dynamic Input Voltage	5.0	C$_L$ = 50pF		0.8	V

Note:
6. Parameter guaranteed by design.

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.

0.496 − 0.512
(12.598 − 13.005)

20 19 18 17 16 15 14 13 12 11

0.394 − 0.419

Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions (Continued)
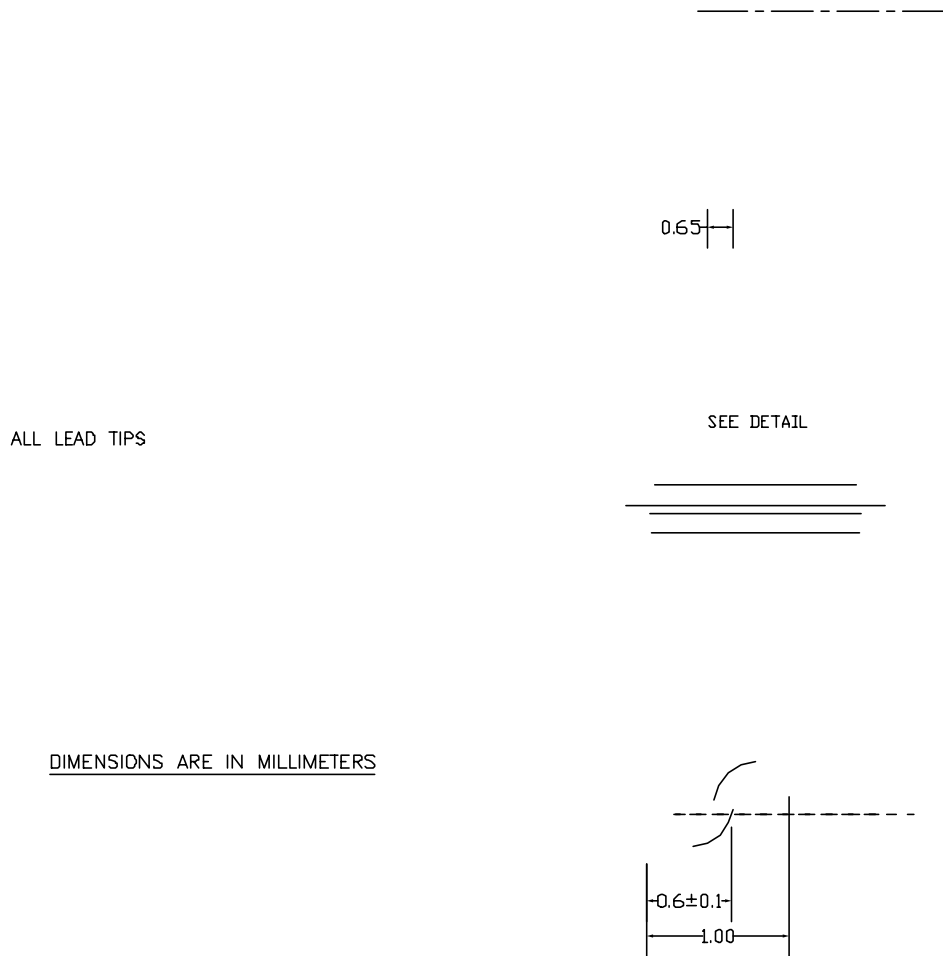Dimensions are in millimeters unless otherwise noted.

DIMENSION

M20DREVC

**Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D**

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.

0.65

SEE DETAIL

ALL LEAD TIPS

DIMENSIONS ARE IN MILLIMETERS

0.6±0.1

1.00

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 198

MTC20REVD1

Figure 3. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

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