- Microprocessor-Based Office Equipment
- Test Equipment and Measuring Instruments

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

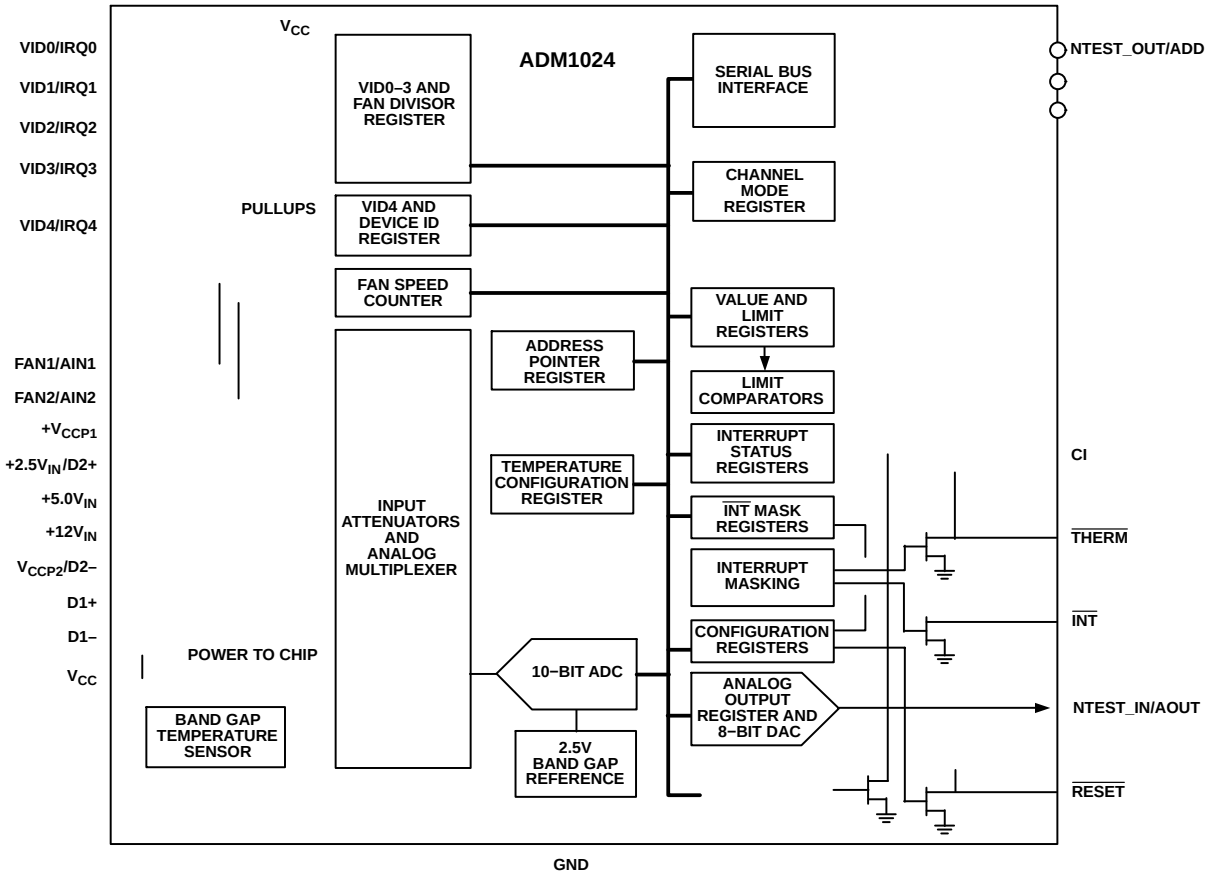


Figure 1. Functional Block Diagram

Table 3. PIN ASSIGNMENT

Pin No.	Mnemonic	Description
1	NTEST_OUT/ADD	Digital I/O. Dual function pin. This is a three-state input that controls the two LSBs of the Serial Bus Address. This pin functions as an output when doing a NAND test.
2	$\overline{\text{THERM}}$	Digital I/O. Dual function pin. This pin functions as an interrupt output for temperature interrupts only, or as an interrupt input for fan control. It has an on-chip 100 kΩ pullup resistor.
3	SDA	Digital I/O. Serial bus bidirectional data. Open-drain output.
4	SCL	Digital Input. Serial bus clock.
5	FAN1/AIN1	Programmable Analog/Digital Input. 0 V to 2.5 V analog input or digital (0 to V_{CC}) amplitude fan tachometer input.
6	FAN2/AIN2	Programmable Analog/Digital Input. 0 V to 2.5 V analog input or digital (0 to V_{CC}) amplitude fan tachometer input.
7	CI	Digital I/O. An active high input from an external latch that captures a Chassis Intrusion event. This line can go high without any clamping action, regardless of the powered state of the ADM1024. The ADM1024 provides an internal open drain on this line, controlled by Bit 6 of Register 40h or Bit 7 of Register 46h, to provide a minimum-21.8126 36.858126 36.m amplit refer mi this 126 0 036929165 Tc.0156 Tw[(lais)-5. lineas

Table 4. ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}, V_{CC}

Table 4. ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted. (Note 1 and 2))

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OPEN-DRAIN SERIAL DATABUS OUTPUT (SDA)					
Output Low Voltage, V_{OL}	I_{OUT} = −3.0 mA, V_{CC} = 2.85 V −3.60 V	−	−	0.4	V
High Level Output Leakage Current, I_{OH}	$V_{OUT} = V_{CC}$	−	0.1	100	A
SERIAL BUS DIGITAL INPUTS (SCL, SDA)					
Input High Voltage, V_{IH}		2.2	−	−	V
Input Low Voltage, V_{IL}		−	−	0.8	V
Hysteresis	eakage Current, I				

TYPICAL PERFORMANCE CHARACTERISTICS

General Description

- Value and Limit Registers: The results of analog voltage inputs, temperature, and fan speed measurements are stored in these registers, along with their limit values.
- Analog Output Register: The code controlling the analog output DAC is stored in this register.
- Chassis Intrusion Clear Register: A signal latched on the chassis intrusion pin can be cleared by writing to this register.

Serial Bus Interface

Control of the ADM1024 is carried out via the serial bus. The ADM1024 is connected to this bus as a slave device, under the control of a master device, e.g., ICH.

The ADM1024 has a 7-bit serial bus address. When the device is powered up, it will do so with a default serial bus address. The 5

ADM1024

ADM1024

A-to-D Converter

These inputs are multiplexed into the on-chip, successive approximation, Analog-to-Digital Converter (ADC). This has a resolution of eight bits. The basic input range is 0 V to 2.5 V, which is the input range of AIN1 and AIN2, but five of the inputs have built-in attenuators to allow measurement of 2.5 V, 5.0 V, 12 V, and the processor core voltages V_{CCP1} and V_{CCP2} without any external components. To allow for the tolerance of these supply voltages, the ADC produces an output of 3/4 full scale (decimal 192) for the nominal input voltage, and so has adequate headroom to cope with overvoltages. Table 7 shows the input ranges of the analog inputs and output codes of the ADC.

Table 8. TEMPERATURE DATA FORMAT

Temperature	Digital Output
−128°C	1000 0000
−125°C	1000 0011
−100°C	1001 1100
−75°C	1011 0101
−50°C	

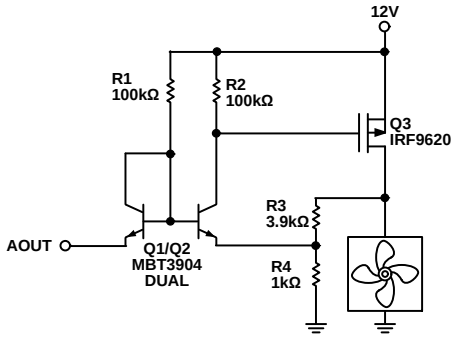


Figure 22. Discrete Fan Drive Circuit with P-Channel MOSFET, Single Supply

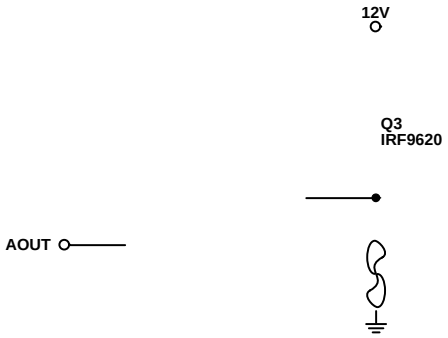


Figure 23. Discrete Fan Drive Circuit with P-Channel MOSFET, Dual Supply

voltage dividers and analog components, will provide best performance but is not mandatory.

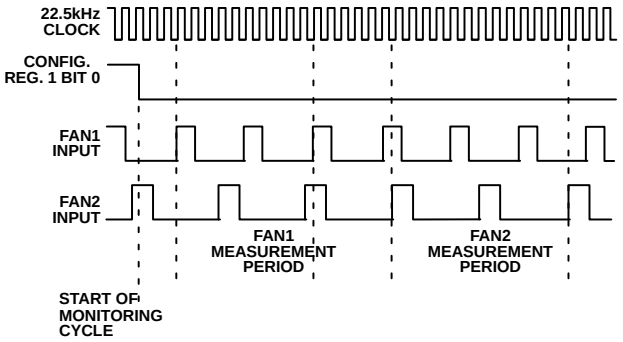


Figure 29. Fan Speed Measurement

The monitoring cycle begins when a one is written to the Start Bit (Bit 0), and a zero to the $\overline{\text{INT}}$_Clear Bit (Bit 3) of the Configuration Register. $\overline{\text{INT}}$_Enable (Bit 1) should be set to one to enable the $\overline{\text{INT}}$ output. The measurement begins on the rising edge of a fan tachometer pulse, and ends on the next−butone rising edge. The fans are monitored sequentially, so if only one fan is monitored, the monitoring time is the time taken after the Start Bit for it to produce two complete tachometer cycles or for the counter to reach full scale, whichever occurs sooner. If more than one fan is monitored, the monitoring time depends on the speed of the fans and the timing relationship of their tachometer pulses. This is illustrated in Figure 30. Once the fan speeds have been measured, they will be stored in the Fan Speed Value Registers and the most recent value can be read at any time. The measurements will be updated as long as the monitoring cycle continues.

To accommodate fans of different speed and/or different numbers of output pulses per revolution, a prescaler (divisor) of 1, 2, 4, or 8 may be added before the counter. The default value is 2, which gives a count of 153 for a fan running at 4400 rpm, producing two output pulses per revolution.

The count is calculated by the equation:

$$\text{Count} = \frac{22.5 \times 10^3 \times 60}{\text{RPM} \times \text{Divisor}} \qquad \text{(eq. 8)}$$

For constant speed fans, fan failure is normally considered to have occurred when the speed drops below 70% of nominal, which would correspond to a count of 219. Full scale (255) would be reached if the fan speed fell to 60% of its nominal value. For temperature−controlled variable speed fans, the situation will be different.

Table 9 shows the relationship between fan speed and time per revolution at 60%, 70%, and 100% of nominal rpm for fan speeds of 1100, 2200, 4400, and 8800 rpm, and the divisor that would be used for each of these fans, based on two tachometer pulses per revolution.

FAN1 and FAN2 Divisors are programmed into Bits 4 to 7 of the VID0–3/Fan Divisor Register.

Table 9. FAN SPEEDS AND DIVISORS

		Time Per				
Divisor RPM	**Nominal RPM**	**Rev (ms)**	**70% RPM**	**Rev 70% (ms)**	**60% RPM**	**Rev 60% (ms)**
÷ 1	8800	6.82	6160	9.74	5280	11.36
÷ 2	4400	13.64	3080	19.48	2640	22.73
÷ 4	2200	27.27	1540	38.96	1320	45.44
÷ 8	1100	54.54	770	77.92	660	90.90

Limit Values

Fans in general will not over-speed if run from the correct voltage, so the failure condition of interest is under-speed due to electrical or mechanical failure. For this reason only, low speed limits are programmed into the limit registers for the fans. It should be noted that, since fan period rather than speed is being measured, a fan failure interrupt will occur when the measurement exceeds the limit value.

Monitoring Cycle Time

The monitoring cycle time depends on the fan speed and number of tachometer output pulses per revolution. Two complete periods of the fan tachometer output (three rising edges) are required for each fan measurement. Therefore, if the start of a fan measurement just misses a rising edge, the measurement can take almost three tachometer periods. In order to read a valid result from the fan value registers, the total monitoring time allowed after starting the monitoring cycle should, therefore, be three tachometer periods of FAN1 plus three tachometer periods of FAN2 at the lowest normal fan speed.

Although the fan monitoring cycle and the analog input monitoring cycle are started together, they are not synchronized in any other way.

Fan Manufacturers

Manufacturers of cooling fans with tachometer outputs are listed below:

NMB Tech
9730 Independence Ave.
Chatsworth, California 91311
Phone: 818−341−3355; Fax: 818−341−8207

Model	Frame Size	Airflow CFM
2408NL	2.36 in sq × 0.79 in; (60 mm sq × 20 mm)	9–16
2410ML	2.36 in sq × 0.98 in; (60 mm sq × 25 mm)	14–25
3108NL	3.15 in sq × 0.79 in; (80 mm sq × 20 mm)	25–42
3110KL	3.15 in sq × 0.98 in; (80 mm sq × 25 mm)	25–40

Mechatronics Inc.
P.O. Box 613
Preston, WA 98050
800−453−4569

operate as level-triggered interrupt inputs, with VID0/IRQ0 to VID2/IRQ2 being active low and VID3/IRQ3 and VID4/IRQ4 being active high. The individual interrupt inputs can be enabled or masked by setting or clearing Bits 4 to 6 of the Channel Mode Register and Bits 6 and 7 of Configuration Register 2 (address 4Ah). These interrupt inputs are not latched in the ADM1024, so they do not require clearing as do bits in the Status Registers. However, the external interrupt source should be cleared once the interrupt has been services, or the interrupt request will be reasserted.

Interrupt Clearing

Reading an Interrupt Status Register will output the contents of the Register, then clear it. It will remain cleared until the monitoring cycle updates it, so the next read operation should not be performed on the register until this has happened, or the result will be invalid. The time taken for a complete monitoring cycle is mainly dependent on the time taken to measure the fan speeds, as described earlier.

The $\overline{\text{INT}}$ output is cleared with the $\overline{\text{INT}}$_Clear bit, which is Bit 3 of the Configuration Register, without affecting the contents of the Interrupt (INT) Status Registers.

Interrupt Status Mirror Registers

Whenever a bit in one of the Interrupt Status Registers is updated, the same bit is written to duplicate registers at addresses 4Ch and 42h. These registers allow a second management system to access the status data without worrying about clearing the data. The data in these registers is for reading only and has no effect on the interrupt output.

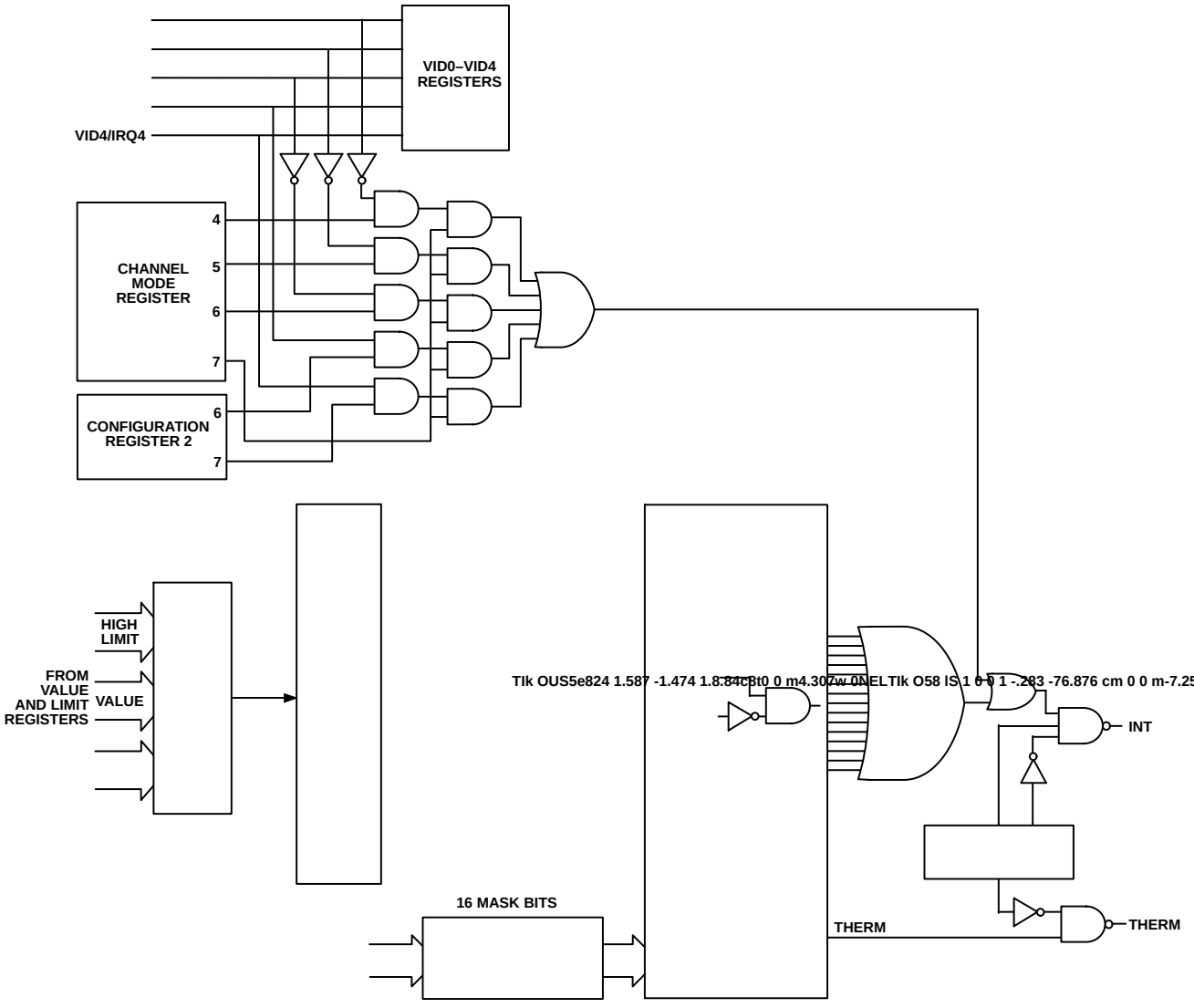


Figure 32. Interrupt Register Structure

Temperature Interrupt Modes

The ADM1024 has two distinct methods of producing interrupts for out−of−limit temperature measurements from the internal or external sensors. Temperature errors can generate an interrupt on the $\overline{\text{INT}}$ pin along with other interrupts, but there is also a separate $\overline{\text{THERM}}$ pin that generates an interrupt only for temperature errors.

temperature limits are stored in a separate register that is not cleared by reading the status register. In this case, $\overline{\text{THERM}}$ can only be cleared by setting Bit 0 of Configuration Register 2.

$\overline{\text{THERM}}$ will be cleared automatically if the temperature falls at least 5 degrees below the limit for three consecutive measurements.

ACPI Mode

In ACPI mode, $\overline{\text{THERM}}$ responds only to the hardware temperature limits at addresses 13h, 14h, 17h, and 18h, not to the software-programmed limits.

Figure 35. $\overline{\text{THERM}}$ Output in ACPI Mode

Configuration Register initialization is accomplished by setting Bit 7 of the Configuration Register high. This bit automatically clears after being set.

Using the Configuration Registers

Control of the ADM1024 is provided through two configuration registers. The ADC is stopped upon powerup, and the $\overline{\text{INT}}$_Clear signal is asserted, clearing the $\overline{\text{INT}}$ output. The Configuration Registers are used to start and stop the ADM1024; enable or disable interrupt outputs and modes, and provide the initialization function described above.

Bit 0 of Configuration Register 1 controls the monitoring loop of the ADM1024. Setting Bit 0 low stops the monitoring loop and puts the ADM1024 into a low power mode thereby reducing power consumption. Serial bus communication is still possible with any register in the ADM1024 while in low power mode. Setting Bit 0 high starts the monitoring loop.

Bit 1 of Configuration Register 1 enables or disables the $\overline{\text{INT}}$ Interrupt output. Setting Bit 1 high enables the $\overline{\text{INT}}$ output; setting Bit 1 low disables the output.

Bit 2 of Configuration Register 1 enables or disables the $\overline{\text{THERM}}$ output. Setting Bit 1 high enables the $\overline{\text{INT}}$ output; setting Bit 1 low disables the output.

Bit 3 of Configuration Register 1 is used to clear the $\overline{\text{INT}}$ interrupt output when set high. The ADM1024 monitoring function will stop until Bit 3 is set low. Interrupt Status register contents will not be affected.

Bit 4 of Configuration Register 1 causes a low going 45 ms (typ) pulse at the $\overline{\text{RESET}}$ pin (Pin 12).

Bit 6 of Configuration Register 1 is used to clear an interrupt at the $\overline{\text{THERM}}$ output when it is set to 1.

Bit 7 of Configuration Register 1 is used to start a Configuration Register Initialization when it is set to 1.

Bit 0 of Configuration Register 2 is used to mask temperature interrupts at the $\overline{\text{INT}}$ output when it is set to 1. The $\overline{\text{THERM}}$ output is unaffected by this bit.

Bits 1 and 2 of Configuration Register 2 lock the values stored in the Local and Remote Fan Control Registers at addresses 13h and 14h. The values in these registers cannot be changed until a power-on reset is performed.

Bit 3 of Configuration Register 2 selects the $\overline{\text{THERM}}$ interrupt mode. The default value of 0 selects one−time mode. Setting this bit to 1 selects ACPI mode.

Starting Conversion

The monitoring function (analog inputs, temperature, and fan speeds) in the ADM1024 is started by writing to Configuration Register 1 and setting Start (Bit 0) high. The $\overline{\text{INT}}$_Enable (Bit 1) should be set to 1, and INT Clear (Bit 3) set to 0 to enable interrupts. The $\overline{\text{THERM}}$enable bit (Bit 2) should be set to 1 and the $\overline{\text{THERM}}$ Clear bit (Bit 6) should be set to 0 to enable temperature interrupts at the $\overline{\text{THERM}}$ pin. Apart from initially starting together, the analog measurements and fan speed measurements proceed independently, and are not synchronized in any way.

The time taken to complete the analog measurements depends on how they are configured, as described elsewhere. The time taken to complete the fan speed measurements depends on

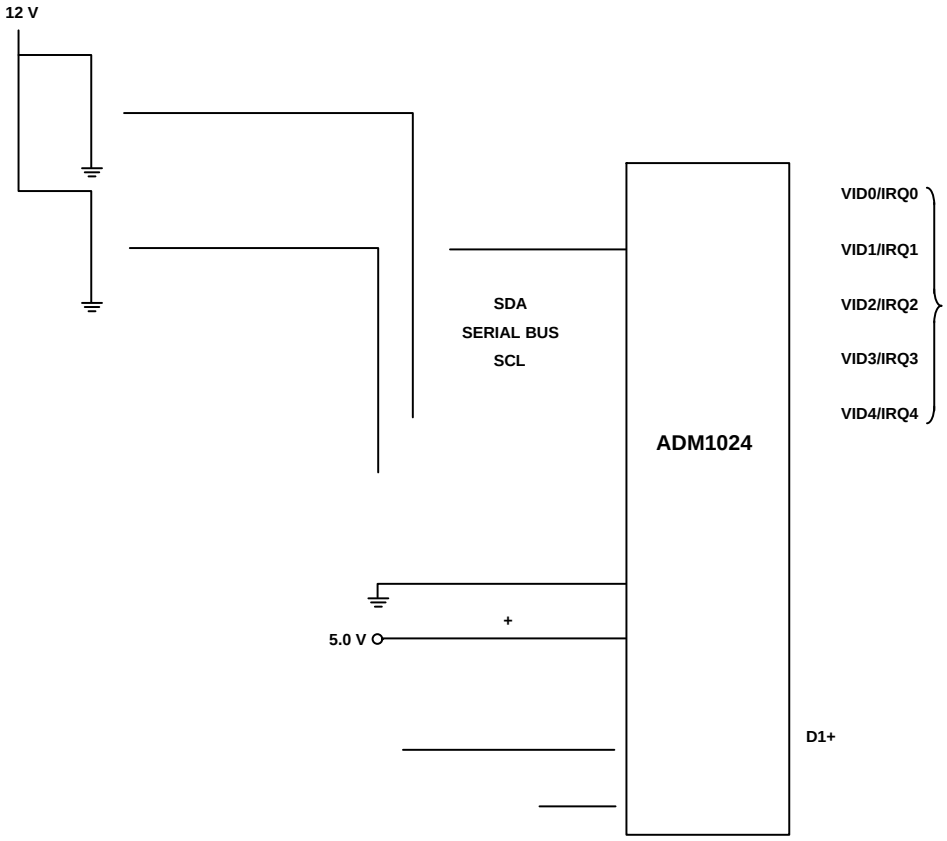


Figure 37. Application Circuit

ADM REGISTERS

Table 10. ADDRESS POINTER REGISTER

Bit	Name	R/W	Description
7–0	Address Pointer	W	Address of ADM1024 registers. See the following tables for details.

Table 11. LIST OF REGISTERS

Hex Addr	Description	Power-on Value (Binary Bit 7−0)	Notes
13h	Internal Temperature Hardware Trip Point	= 70°C	Can be written only if the write once bit in Configuration Register 2 has not been set. Values higher than 70°C will have no affect as the fixed trip point in register 16h will be reached first.
14h	External Temperature Hardware Trip Point	= 85°C	Can be written only if the write once bit in Configuration Register 2 has not been set. Values higher than 85°C will have no affect as the fixed trip point in register 17h will be reached first.
15h	Test Register		

Table 11. LIST OF REGISTERS

Hex Addr	Description	Power-on Value (Binary Bit 7−0)	Notes
34h	12 V Low Limit	Indeterminate	
35h	V_{CCP2} High Limit	Indeterminate	
36h	V_{CCP2} Low Limit	Indeterminate	
37h	Ext. Temp1 High Limit	Indeterminate	Stores high limit for a diode sensor connected to Pins 13 and 14.
38h	Ext. Temp1 Low Limit	Indeterminate	Stores low limit for a diode sensor connected to Pins 13 and 14.
39h	Internal Temp. High Limit	Indeterminate	Stores the high limit for the internal temperature reading.
3Ah	Internal Temp. Low Limit	Indeterminate	Stores the low limit for the internal temperature reading.
3Bh	A_{IN1}/FAN1 High Limit	Indeterminate	Stores high limit for AIN1 or FAN1, depending on the configuration of Pin 5.
3Ch	A_{IN2}/FAN2 High Limit	Indeterminate	Stores high limit for AIN2 or FAN2, depending on the configuration of Pin 6.
3Dh	Reserved	Indeterminate	
3Eh	Company ID Number	0100 0001	This location will contain the company identification number (Read Only).
3Fh	Revision Number	0001 nnnn	Last four bits of this location will contain the revision number of the part (Read Only).
40h	Configuration Register 1	0000 1000	See Table 10
41h	Interrupt INT Status Register 1	0000 0000	See Table 11
42h	Interrupt INT Status Register 2	0000 0000	See Table 12
43h	INT Mask Register 1	0000 0000	See Table 13
44h	INT Mask Register 2	0000 0000	See Table 14
46h	Chassis Intrusion Clear Register	0000 0000	See Table 15
47h	VID0–3/Fan Divisor Register	0101 (VID3–VID0)	See Table 16
49h	VID4 Register	1000 000 (VID4)	See Table 17
4Ah	Configuration Register 2	0000 0000	See Table 18
4Ch	Interrupt Status Register Mirror 1	0000 0000	See Table 19
4Dh	Interrupt Status Register Mirror 2	0000 0000	See Table 20

Table 12. REGISTER 16H, CHANNEL MODE REGISTER (POWER-ON DEFAULT, 00H)

Bit	Name	R/W	Description
0	FAN1/A_{IN1}	R/W	Clearing this bit to 0 configures Pin 5 as FAN1 input. Setting this bit to 1 configures Pin 5 as AIN1. Power−on default = 0.
1	FAN2/A_{IN2}	R/W	Clearing this bit to 0 configures Pin 6 as FAN2 input. Setting this bit to 1 configures Pin 6 as AIN2. Power−on default = 0.
2	2.5 V, V_{CCP2}/D2	R/W	Clearing this bit to 0 configures Pins 17 and 18 to measure V_{CCP2} and 2.5 V. Setting this bit to 1 configures Pins 17 and 18 as an input for a second remote temperature−sensing diode. Power−on default = 0.
3	Int. V_{CC}	R/W	Clearing this bit to 0 sets the measurement range for the internal V_{CC} measurement to 3.3 V. Setting this bit to 1 sets the internal V_{CC} measurement range to 5.0 V. Power−on default = 0.
4	IRQ0 EN	R/W	Setting this bit to 1 enables Pin 24 as an active high interrupt input, provided Pins 20 to 24 have been configured as interrupts by setting Bit 7 of the Channel Mode Register. Power−on default = 0.
5	IRQ1 EN	R/W	Setting this bit to 1 enables Pin 23 as an active high interrupt input, provided Pins 20 to 24 have been configured as interrupts by setting Bit 7 of the Channel Mode Register. Power−on default = 0.
6	IRQ2 EN	R/W	Setting this bit to 1 enables Pin 22 as an active high interrupt input, provided Pins 20 to 24 have been configured as interrupts by setting Bit 7 of the Channel Mode Register. Power−on default = 0.
7	VID/IRQ	R/W	

Table 13. REGISTER 40H, CONFIGURATION REGISTER 1 (POWER-ON DEFAULT, 08H)

Bit	Name	R/W	Description
0	START	R/W	Logic 1 enables startup of ADM1024; Logic 0 places it in standby mode. Caution: The outputs of the interrupt pins will not be cleared if the user writes a 0 to this location after an interrupt has occurred (see “$\overline{\text{INT}}$ Clear” bit). At startup, limit checking functions and scanning begins. Note, all high and low limits should be set into the ADM1024 prior to turning on this bit (Power−On Default = 0).
1	$\overline{\text{INT}}$_Enable	R/W	Logic 1 enables the $\overline{\text{INT}}$_output. 1 = Enabled 0 = Disabled (Power−On Default = 0).
2	$\overline{\text{THERM}}$ Enable	R/W	0 = $\overline{\text{THERM}}$ disabled 1 = $\overline{\text{THERM}}$ enabled
3	$\overline{\text{INT}}$_Clear	R/W	During Interrupt Service Routine (ISR), this bit is asserted Logic 1 to clear $\overline{\text{INT}}$ output without affecting the contents of the Interrupt Status Register. The device will stop monitoring. It will resume upon clearing of this bit. (Power−On Default = 0)
4	$\overline{\text{RESET}}$	R/W	Setting this bit generates a low going 45 ms reset pulse at Pin 12. This bit is self−clearing and power−on default is 0.
5	Reserved	R/W	Default = 0
6	$\overline{\text{THERM}}$ CLR	R/W	A 1 clears the $\overline{\text{THERM}}$ output without changing the Status Register contents.
7	Initialization	R/W	Logic 1 restores power−on default values to the Configuration Register, Interrupt Status Registers, Interrupt Mask Registers, Fan Divisor Register, and the Temperature Configuration Register. This bit automatically clears itself since the power−on default is 0.

Table 14. REGISTER 41H, INTERRUPT STATUS REGISTER 1 (POWER-ON DEFAULT, 00H)

Bit	Name	R/W	Description
0	2.5 V/External Temp2 Error	Read only	A 1 indicates that a High or Low limit has been exceeded.
1	V_{CCP1} Error	Read only	A 1 indicates that a High or Low limit has been exceeded.

Table 16. REGISTER 43H, $\overline{\text{INT}}$ INTERRUPT MASK REGISTER 1 (POWER-ON DEFAULT, 00H)

Bit	Name	R/W	Description
0	2.5 V/Ext. Temp2	R/W	A 1 disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
1	V_{CCP1}	R/W	A 1 disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
2	V_{CC}	R/W	A 1 disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
3	5.0 V	R/W	A 1 disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
4	Int. Temp	R/W	A 1 disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
5	Ext. Temp1	R/W	A 1 disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
6	FAN1/A_{IN1}	R/W	

Table 21. REGISTER 4AH, CONFIGURATION REGISTER 2 (POWER-ON DEFAULT, [7:0] = 0X00H)

Bit	Name	R/W	Description
0	Thermal $\overline{\text{INT}}$ Mask	R/W	Setting this bit masks the thermal interrupts for the $\overline{\text{INT}}$ output ONLY. The $\overline{\text{THERM}}$ output will still be generated, regardless of the setting of this bit.
1	Ambient Temp Fan Control Register Write Once Bit	R/W once	Writing a 1 to this bit will lock in the values set into the ambient temperature automatic fan control register 13h. This register will not be able to be written again until a reset is performed (either POR, Hard Reset, or Soft Reset).
2	Remote Temp Fan Control Register Write Once Bit	R/W once	Writing a 1 to this bit will lock in the values set into the remote temperature automatic fan control register 14h. This register will not be able to be written again until a reset is performed (either POR, Hard Reset, or Soft Reset).
3	$\overline{\text{THERM}}$	R/W	If this bit is 0, the $\overline{\text{THERM}}$ output operates in default mode.
	Interrupt Mode		If this bit is 1, the $\overline{\text{THERM}}$ output operates in ACPI mode.
4, 5	Reserved	Read only	Reserved
6	IRQ3 EN	R/W	Setting this bit to 1 enables Pin 21 as an active high interrupt input, provided Pins 20 to 24 have been configured as interrupts by setting Bit 7 of the Channel Mode Register. Power−on default = 0.
7	IRQ4 EN	R/W	Setting this bit to 1 enables Pin 20 as an active high interrupt input, provided Pins 20 to 24 have been configured as interrupts by setting Bit 7 of the Channel Mode Register. Power−on default = 0.

Table 22. REGISTER 4CH, INTERRUPT STATUS REGISTER 1 MIRROR (POWER-ON DEFAULT, [7:0] = 00H)

Bit	Name	R/W	Description
0	2.5 V/Ext. Temp2 Error	Read only	A 1 indicates that a High or Low limit has been exceeded.
1	V_{CCP1} Error	Read only	A 1 indicates that a High or Low limit has been exceeded.
2	V_{CC} Error	Read only	A 1 indicates that a High or Low limit has been exceeded.
3	5.0 V Error	Read only	A 1 indicates that a High or Low limit has been exceeded.
4	Internal Temp Error	Read only	A 1 indicates that a temperature interrupt has been set, or that a High or Low limit has been exceeded.
5	External Temp1 Error	Read only	A 1 indicates that a temperature interrupt has been set, or that a High or Low limit has been exceeded.
6	FAN1/A_{IN1} Error	Read only	A 1 indicates that a High or Low limit has been exceeded.
7	FAN2/A_{IN2} Error	Read only	A 1 indicates that a High or Low limit has been exceeded.

Table 23. REGISTER 4DH, INTERRUPT STATUS REGISTER 2 MIRROR (POWER-ON DEFAULT, [7:0] = 00H) (Note 1)

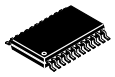
Bit	Name	R/W	Description
0	12 V Error	Read only	A 1 indicates a High or Low limit has been exceeded.
1	V_{CCP2} Error	Read only	A 1 indicates a High or Low limit has been exceeded.
2	Reserved	Read only	Undefined.
3	Reserved	Read only	Undefined.
4	Chassis Error	Read only	A 1 indicates Chassis Intrusion has gone high.
5	$\overline{\text{THERM}}$ Interrupt	Read only	Indicates that $\overline{\text{THERM}}$ pin has been pulled low by an external source.
6	D1 Fault	Read only	Short or Open−Circuit Sensor Diode D1.
7	D2 Fault	Read only	Short or Open−Circuit Sensor Diode D2.

1. An error that causes continuous interrupts to be generated may be masked in its respective mask register, until the error can be alleviated.

Table 24. ORDERING INFORMATION

Device Order Number	Temperature Range	Package Type	Shipping†
ADM1024ARUZ−REEL			

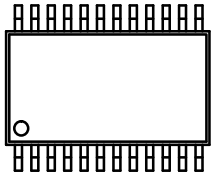
TSSOP24 7.8x4.4, 0.65P



SCALE 1:1

DIM	MILLIMETERS MIN	MAX
A	---	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E1	4.30	4.50
e	0.65	
L	0.50	0.75
L2	0.25	
M	0°	8°

GENERIC
MARKING DIAGRAM*



ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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