Product Preview

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Features

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Applications

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See detailed ordering and

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

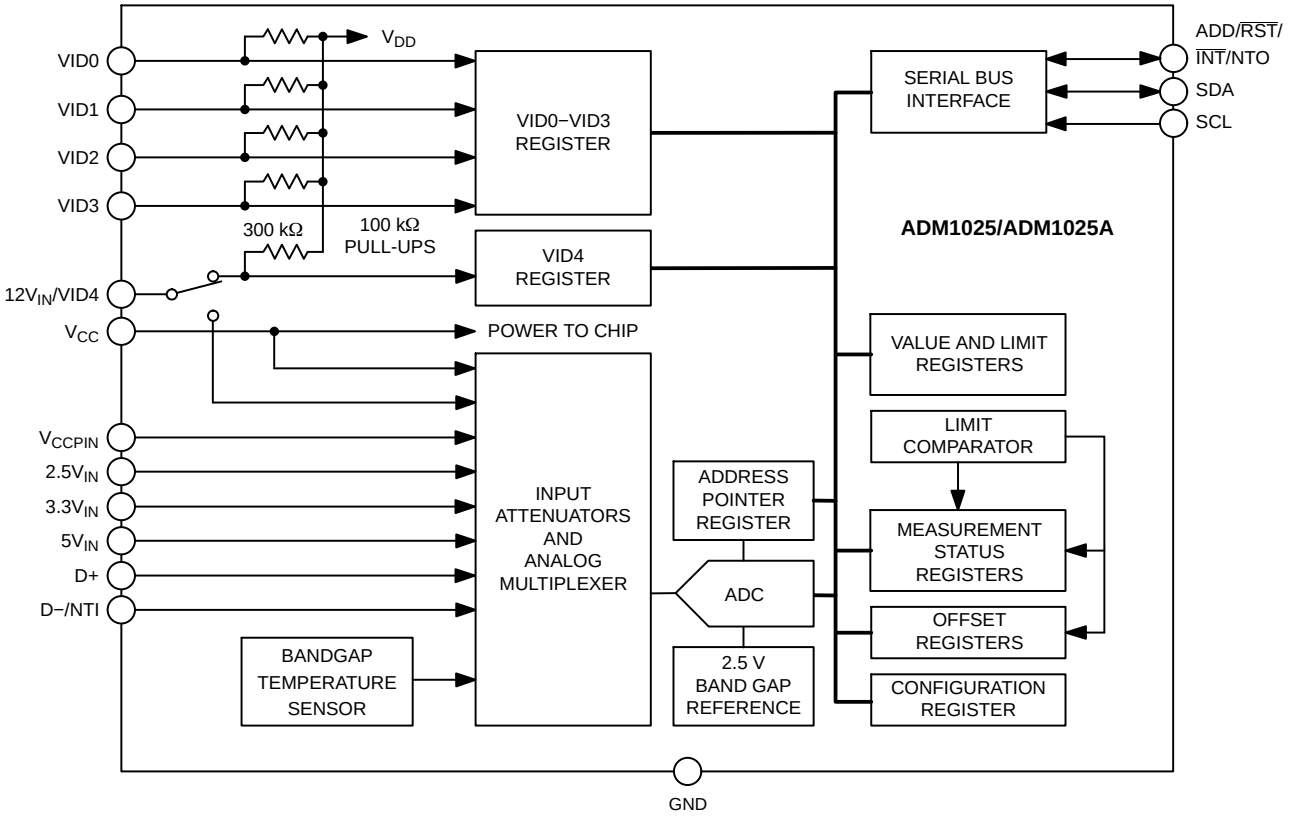

Figure 1. Functional Block Diagram

Table 1. ABSOLUTE MAXIMUM RATINGS

Rating	Value	Unit
Positive Supply Voltage (V_{CC})	6.5	V
Voltage on 12 V V_{IN} Pin	20	V
Voltage on Any Input or Output Pin	−0.3 to +6.5	V
Input Current at Any Pin	±5	mA
Package Input Current	±20	mA

Table 3. PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	SDA	Digital I/O. Serial bus bidirectional data. Open-drain output.
2	SCL	Digital Input. Serial bus clock.
3	GND	System Ground
4	V_{CC}	Power. Can be powered by 3.3 V standby power if monitoring in low power states is required. This pin also serves as the analog input to monitor V_{CC}.
5	VID0	Digital Input. Core voltage ID readouts from the processor. This value is read into the VID0−VID3 Status Register. It has an on-chip 100 kΩ pull-up resistor (ADM1025 only).
6	VID1	Digital Input. Core voltage ID readouts from the processor. This value is read into the VID0−VID3 Status Register. It has an on-chip 100 kΩ pull-up resistor (ADM1025 only).
7	VID2	Digital Input. Core voltage ID readouts from the processor. This value is read into the VID0−VID3 Status Register. It has an on-chip 100 kΩ pull-up resistor (ADM1025 only).
8	VID3	Digital Input. Core voltage ID readouts from the processor. This value is read into the VID0−VID3 Status Register. It has an on-chip 100 kΩ pull-up resistor (ADM1025 only).
9	D−/NTI	Analog/Digital Input. Connected to cathode of external temperature sensing diode. If held high at power-up, it initiates NAND tree test mode.
10	D+	Analog Input. Connected to anode of external temperature sensing diode.
11	$12V_{IN}$/VID4	Programmable Analog/Digital Input. Defaults to 12 V_{IN} analog input at power-up but may be programmed as VID4 Core Voltage ID readout from the processor. This value is read into the VID4 Status Register. In analog 12 V_{IN} mode, it has an on-chip voltage attenuator. In VID4 mode, it has an on-chip 300 kΩ pull-up resistor.
12	$5V_{IN}$	Analog Input. Monitors 5 V supply.
13	$3.3V_{IN}$	Analog Input. Monitors 3.3 V supply.
14	$2.5V_{IN}$	Analog Input. Monitors 2.5 V supply.
15	V_{CCPIN}	

Table 4. ELECTRICAL CHARACTERISTICS (continued)
($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OPEN-DRAIN DIGITAL OUTPUTS (ADD, $\overline{RST}$, $\overline{INT}$, NTO)					
Output Low Voltage, V_{OL}	I_{OUT} = −6.0 mA, V_{CC}				

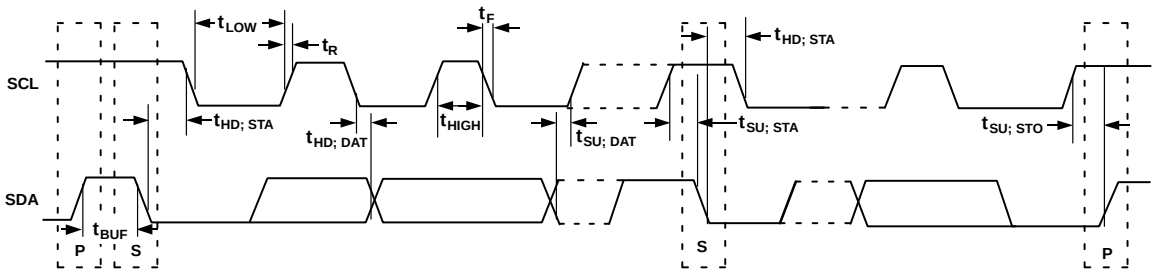

Figure 2. Serial Bus Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

General Description

Measurement Inputs

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Sequential Measurement

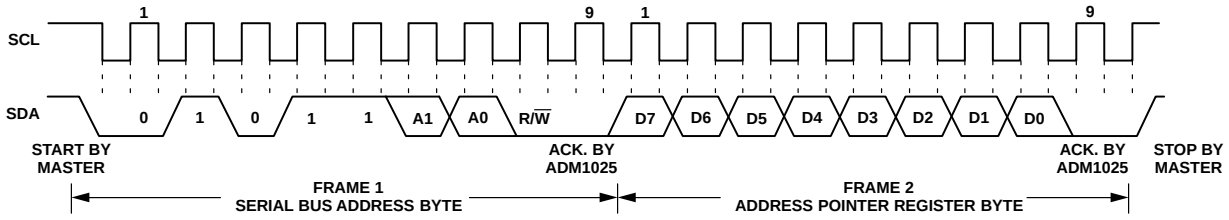

Figure 11. Writing to the Address Pointer Register Only

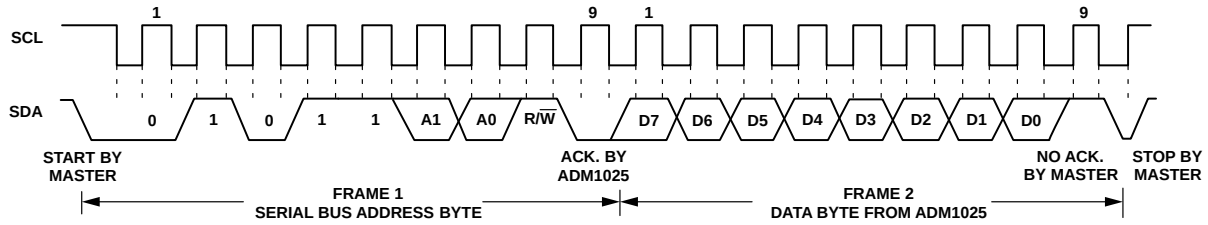

Figure 12. Reading Data from a Previously Selected Register

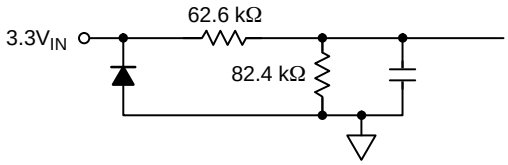

Figure 13. Structure of Analog Inputs

NOTES:

1. Although it is possible to read a data byte from a data register without first writing to the Address Pointer Register, if the Address Pointer Register is already at the correct value, it is not possible to write data to a register without writing to the Address Pointer Register because the first data byte of a write is always written to the Address Pointer Register.
2. In Figure 10 to Figure 12, the serial bus address is shown as the default value 01011(A1)(A0), where A1 and A0 are set by the three-state ADD pin.
3. In addition to supporting the Send Byte and Receive Byte protocols, the ADM1025/ADM1025A also supports the Read Byte protocol (see System Management Bus specifications Rev. 1.1 for more information).
4. If Reset or interrupt functionality is required, the address pin cannot be strapped to GND, since this would keep the ADD/$\overline{\text{RST}}$/$\overline{\text{INT}}$/NTO pin permanently low.

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Table 7. TEMPERATURE DATA FORMAT

Temperature	Digital Output
−128°C	1000 0000
−125°C	1000 0011
−100°C	1001 1100
−75°C	

$$\Delta V_{BE} = KT/q \times \ln(N) \quad \text{(eq. 1)}$$

K
q
T
N

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Layout Considerations

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Figure 15. Arrangement of Signal Tracks

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Generating an SMBALERT

NAND Tree Tests

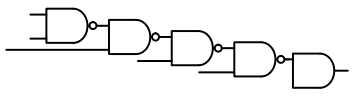


Figure 17. NAND Tree

Starting Conversion

Table 12. REGISTER 41h −

IMIT REGISTERS (Note 1)

Description
Manufacturers Test Register
Offset Register
2.5 V Reading
V_{CCP} Reading
3.3 V Reading
5 V Reading
12 V Reading
V_{CC} Reading
Remote Diode Temperature Reading
Local Temperature Reading
2.5 V High Limit
2.5 V Low Limit
V_{CCP} High Limit
V_{CCP} Low Limit
3.3 V High Limit
3.3 V Low Limit
5 V High Limit
5 V Low Limit
12 V High Limit

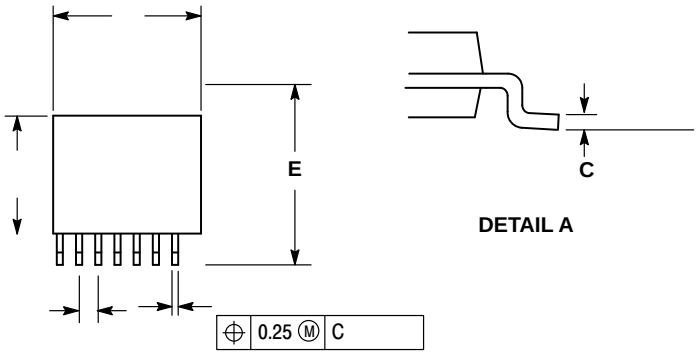
Table 20. NAND TREE TEST VECTORS

Vector No.	SDA	SCL	VID0	VID1	VID2	VID3	ADD/$\overline{\text{RST}}$/INT

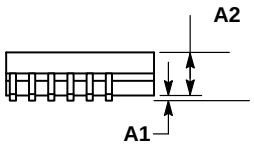
QSOP16
CASE 492−01
ISSUE A

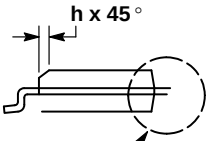
DATE 23 MAR 2011

SCALE 2:1



DETAIL A





DETAIL A

NOTES:

DIM	INCHES MIN	MA
A	0.053	0.069
A1	0.004	0.010
	0.008	0.012
	0.007	0.010
	0.025 BSC	
	0.009	0.020
L	0.016	0.050
M	0	8