Figure 1. Functional Block Diagram

Table 4. ELECTRICAL CHARACTERISTICS

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
		– – –		–	µ
TEMPERATURE-TO-DIGITAL CONVERTER					
		–			
		–		–	
		–			
		–		–	
		– –		– –	µ
ANALOG-TO-DIGITAL CONVERTER					
		–	–		
		–	–		
		–		–	
		– –		– –	
FAN RPM-TO-DIGITAL CONVERTER					
		–	–		
		–	–		
		– – – –		– – – –	
OPEN-DRAIN DIGITAL OUTPUTS ($\overline{\text{INT}}$, $\overline{\text{CFAULT}}$)					
	–	–	–		
		–			µ
OPEN-DRAIN SERIAL DATA BUS OUTPUT (SDA)					
		–	–		
		–			µ
SERIAL BUS DIGITAL INPUTS (SCL, SDA)					
			–	–	
		–	–		
		–		–	
DIGITAL INPUT LOGIC LEVELS ($\overline{\text{RESET}}$, GPIO1−6, $\overline{\text{FAULT1/2}}$, TACH1/2, $\overline{\text{PRESENT1/2}}$)					
			–	–	
		–	–		
DIGITAL INPUT CURRENT					
			–	–	µ

Table 4. ELECTRICAL CHARACTERISTICS

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SERIAL BUS TIMING					
			–	–	μ
			–	–	μ
			–	–	μ
			–	–	μ
			–	–	μ
			–		μ
		–	–		
		–	–		
			–	–	
			–	–	

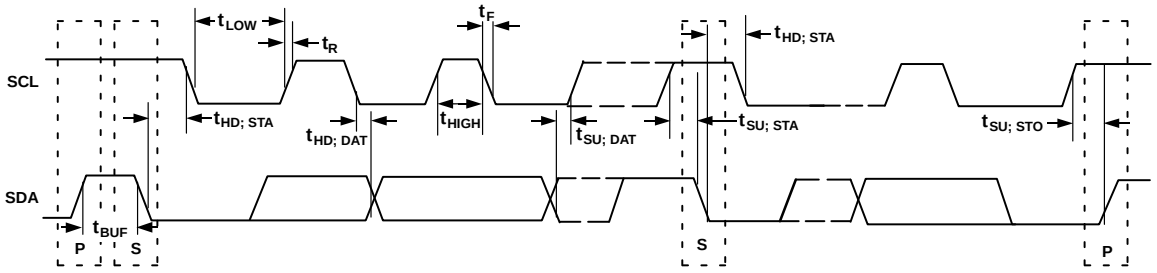
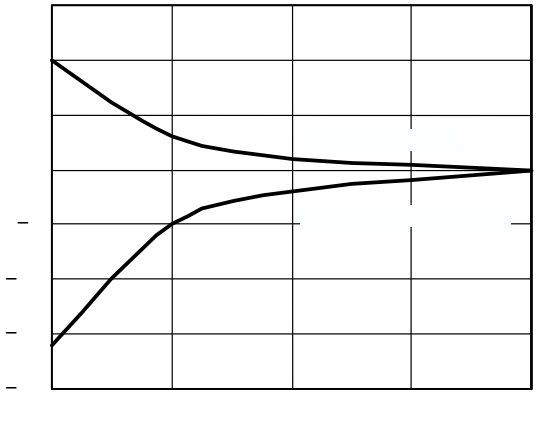


Figure 2. Serial Bus Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS



Ω

Figure 3. Remote Temperature Error vs. PC Board Track Resistance

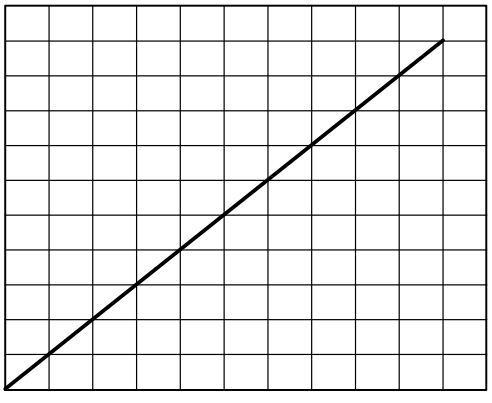


Figure 4. Pentium® III Temperature Measurement vs. ADM1029 Reading

TYPICAL PERFORMANCE CHARACTERISTICS

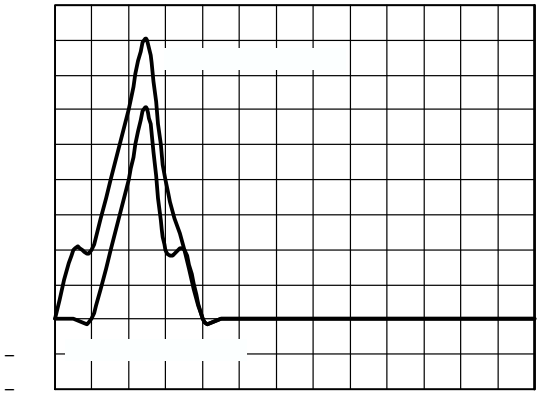


Figure 5. Remote Temperature Error vs. Power Supply Noise Frequency

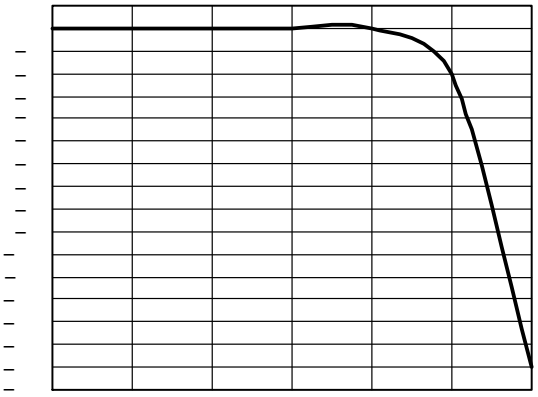


Figure 6. Remote Temperature Error vs. Capacitance between D+ and D−

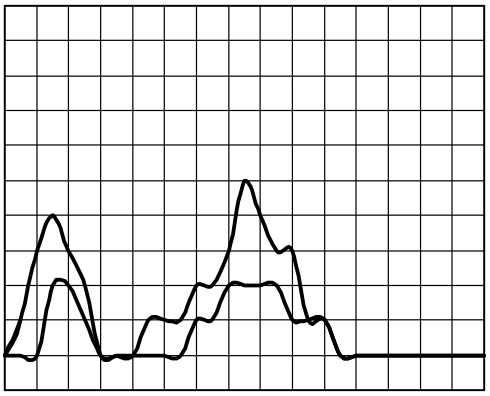


Figure 7. Remote Temperature Error vs. Common-mode Noise Frequency

Figure 8. Standby Current vs. Clock Frequency

Functional Description

Serial Bus Interface

Control of the ADM1029 is carried out via the serial bus. The ADM1029 is connected to this bus as a slave device, under the control of a master device.

The ADM1029 has a 7-bit serial bus address. The four MSBs of the address are set to 0101. The three LSBs can be set by the user to give a total of eight different addresses, allowing up to eight ADM1029s to be connected to a single serial bus segment.

To minimize device pin count and size, the three LSBs are set using a single pin (ADD, Pin 15). This is an 8-level input whose input voltage is set by a potential divider. The voltage on ADD is sampled immediately after power-up and digitized by the on-chip ADC to determine the value of the 3 LSBs. Since ADD is sampled only at power-up, any changes made while power is on will have no effect.

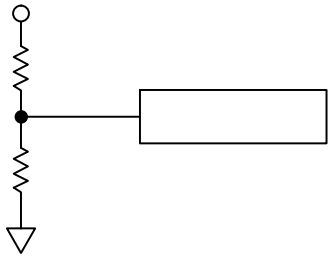


Figure 16. Setting the Serial Address

Table 5 shows resistor values for setting the 3 LSBs of the serial bus address. The same principle is used to set the voltage on Pin 18 (TMIN/INSTALL), which controls the automatic fan speed control function, and also tells the ADM1029 how many fans should be installed, as described later.

If several ADM1029s are used in a system, their ADD inputs can tap off a single potential divider, as shown in Figure 17.

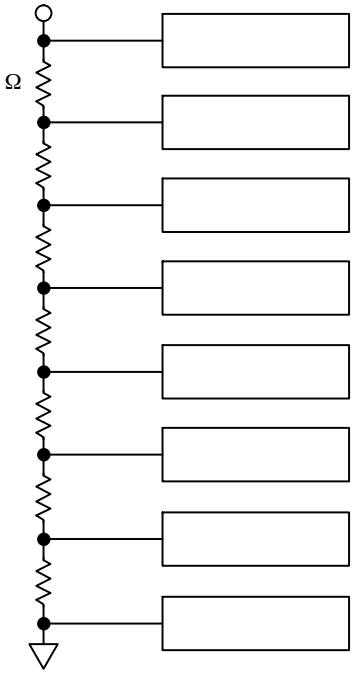


Figure 17. Setting Address of up to Eight ADM1029s

write to the slave device. If the R/$\overline{W}$ bit is a 1 the master will read from the slave device.

2. Data is sent over the serial bus in sequences of nine clock pulses, eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low-to-high transition when the clock is high may be interpreted as a STOP signal. The number of data bytes that can be transmitted over the serial bus in a single READ or WRITE operation is limited only by what the master and slave devices can handle.
3. When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master will pull the data line high during the tenth clock pulse to assert a STOP condition. In READ mode, the master device will override the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse. This is known as No Acknowledge. The master will then take the data line low during the low period before the tenth clock pulse, high during the tenth clock pulse to assert a STOP condition.

Any number of bytes of data may be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation, because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

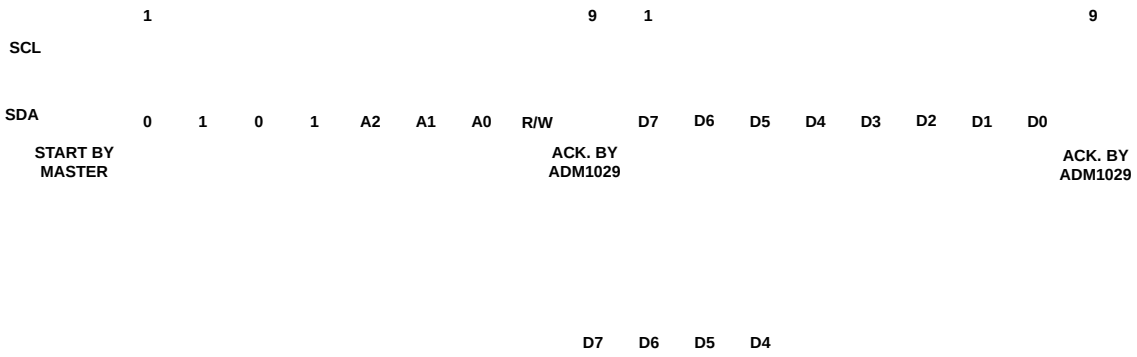


Figure 18. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

In the case of the ADM1029, write operations contain either one or two bytes, and read operations contain one byte, and perform the following functions:

To write data to one of the device data registers or read data from it, the Address Pointer Register must be set so that

provided for temperature monitoring on some microprocessors, but it could equally well be a discrete transistor.

If a discrete transistor is used, the collector will not be grounded, and should be linked to the base. If a PNP transistor is used, the base is connected to the D– input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D– input and the base to the D+ input.

Figure 21. Signal Conditioning for Remote Diode Temperature Sensors

1. Place the ADM1029 as close as possible to the remote sensing diode. Provided that the worst noise sources such as clock generators, data/address buses, and CRTs are avoided, this distance can be 4 to 8 inches.
2. Route the D+ and D– tracks close together, in parallel, with grounded guard tracks on each side. Provide a ground plane under the tracks if possible.
3. Use wide tracks to minimize inductance and reduce noise pickup. Ten mil track minimum width and spacing is recommended.

Figure 22. Arrangement of Signal Tracks

4. Try to minimize the number of copper/solder joints, which can cause thermocouple effects. Where copper/solder joints are used, make sure that they are in both the D+ and D– path and at the same temperature.
   Thermocouple effects should not be a major problem as 1 C corresponds to about 240 μV, and thermocouple voltages are about 3 μV/ C of temperature difference. Unless there are two thermocouples with a big temperature differential between them, thermocouple voltages should be much less than 200 μV.
5. Place 0.1 μF bypass and 1000 pF input filter capacitors close to the ADM1029.
6. If the distance to the remote sensor is more than 8 inches, the use of twisted pair cable is recommended. This will work up to about 6 to 12 feet.
7. For really long distances (up to 100 feet), use shielded twisted pair such as Belden #8451 microphone cable. Connect the twisted pair to D+ and D– and the shield to GND close to the ADM1029. Leave the remote end of the shield unconnected to avoid ground loops.

Because the measurement technique uses switched current sources, excessive cable and/or filter capacitance can affect the measurement. When using long cables, the filter capacitor may be reduced or removed.

Cable resistance can also introduce errors. 1 Ω series resistance introduces about 0.5 C error.

Temperature-related Registers

Table 7 is a list of registers on the ADM1029 that are specific to temperature measurement and control.

Table 7. TEMPERATURE-SPECIFIC REGISTERS

Address	Description

expects to see a fan interfaced to it. It does not necessarily mean that the fan is actually, physically, connected.

If two fans are installed, Bit 0 would be 1 by default and Pin 18 would be tied high* to set Bit 1. If only one fan is installed, it would normally be Fan 1 and Pin 18 would be tied low* to clear Bit 1. However, both of these bits can be modified by writing to the register, so it is possible to have Fan 2 installed and not Fan 1, or even have no fans installed.

$\overline{\text{FAULT}}$ Inputs/Outputs

The ADM1029 can be used with fans that have a fault output which indicates if the fan has stalled or failed. If one or both of the $\overline{\text{FAULT}}$ inputs (Pin 2 or Pin 23) goes low, both $\overline{\text{INT}}$ and $\overline{\text{CFAULT}}$ will be asserted.

Events on the fault inputs are also reflected in Bits 2 and 3 of the corresponding Fan Status Registers at addresses 10h and 11h. Bit 2 reflects the inverse state of the $\overline{\text{FAULT}}$ pin (0 if $\overline{\text{FAULT}}$ is high, 1 if $\overline{\text{FAULT}}$ is low), while Bit 3 is latched high if a $\overline{\text{FAULT}}$ input goes low. It must be cleared by writing a zero to it.

If the fan(s) being used do not have a $\overline{\text{FAULT}}$ output, the $\overline{\text{FAULT}}$ input(s) on the ADM1029 should be pulled high to V_{CC}.

The $\overline{\text{FAULT}}$ pins can also be configured as open-drain outputs by setting Bit 5 of the corresponding Fan Fault Action Register (18h or 19h). If a $\overline{\text{FAULT}}$ pin is configured as an output, it will still function as an input. This means that when a fault input occurs it will be latched low by the fault output, even if the fault input is removed. The fault output can be used to drive a fan failure indicator such as an LED.

If the $\overline{\text{FAULT}}$ pin is used as an output, any input to the $\overline{\text{FAULT}}$ pin should also be open-drain. This will avoid the fault input trying to source a high current into the $\overline{\text{FAULT}}$ pin if the fault input goes high while the fault output is low.

Fan Present Inputs

The fan $\overline{\text{PRESENT}}$ signal is implemented by a shorting link to ground in the fan connector. When the fan is plugged in, the corresponding $\overline{\text{PRESENT}}$ input (Pin 4 or Pin 21) on the ADM1029 is pulled low. If the fan is unplugged, the $\overline{\text{PRESENT}}$ input will be pulled high. $\overline{\text{INT}}$ and $\overline{\text{CFAULT}}$ will be asserted (unless masked) and the event will be reflected in Bits 0 and Bit 1 of the corresponding Fan Status Register.

Appearance or disappearance of a $\overline{\text{PRESENT}}$ input signal during normal operation signals to the ADM1029 that a fan has been hot-plugged or unplugged. $\overline{\text{INT}}$

Fan Speed Limits

Fans generally do not overspeed if run from the correct voltage, so the failure condition of interest is under-speed due to electrical or mechanical failure. For this reason only low-speed limits are programmed into the Tach Limit Registers for the fans. These registers are at address 78h for Fan 1 and 79h for Fan 2. It should be noted that, since fan period rather than speed is being measured, the fan speed count will be larger the slower the fan speed. Therefore a fan failure fault will occur when the measurement *exceeds* the limit value.

For the most accurate fan failure indication, the oscillator

an analog input crosses the corresponding AIN low limit, the direction depending on the setting of Bit 3 of the AIN control register. (0 = alarm when input goes below low limit, 1 = alarm when input goes above low limit).

If a thermal override occurs while the ADM1029 is in sleep mode, all fans controlled by the ADM1029 will run at alarm speed.

Hot-plug Speed

Hot-plug speed is set by the four LSBs of the Fan 1 and Fan 2 Configuration Registers (addresses 68h and 69h). The PWM frequency is set by Bits 4 and 5 of these registers, while Bits 6 and 7 set the number of pulses per revolution for fan speed measurement.

Fan(s) will run at hot-plug speed if any of the following conditions occur, assuming the condition has not been masked using the Fan Event Mask Registers:

If a fan is unplugged, the other fan (if any) controlled by the ADM1029 will run at hot-plug speed.

Setting Bit 0 of register 08h forces Fan 1 to run at hot-plug speed (Set Fan x Hot-plug Speed).

Setting Bit 1 of register 08h forces Fan 2 to run at hot-plug speed (Set Fan x Hot-plug Speed).

When a GPIO pin is configured as an input by setting Bit 0 of the corresponding GPIO Behavior Register, and Bit 5 of the GPIO Behavior Register is also set, all fans controlled by the ADM1029 will go to hot-plug speed when the logic input is asserted (high or low, depending on the polarity bit, Bit 1 of the corresponding GPIO Behavior Register).

If Bit 6 of a Fan Fault Action Register is set (18h for Fan 1, 19h for Fan 2) the corresponding fan will go to hot-plug speed when $\overline{\text{CFAULT}}$ is pulled low by an external source.

Full Speed

Fans will run at full speed if the corresponding bits in the Set Fan x Full Speed Register (address 09h) are set: Bit 0 for Fan 1 and Bit 1 for Fan 2.

Fan Mask Registers

The effect of various conditions on fan speed can be enabled or disabled by mask registers. In all these registers, setting Bit 0 of the register enables Fan 1 to go to alarm speed or hot-plug speed if the corresponding event occurs, while setting Bit 1 enables Fan 2. Clearing these bits masks the effect of the corresponding event on fan speed.

Registers 20h and 21h are Fan Event Mask Registers. Bits 0 and 1 of register 20h enable (bit set) or mask (bit clear) the effect of a Fan 1 fault (underspeed or fault input) on Fan 1 and Fan 2 speed. Similarly, Bits 0 and 1 of register 21h enable (bit set) or mask (bit clear) the effect of a Fan 2 Fault on Fan 1 and Fan 2 speed.

Registers 38h to 3Eh are GPIO X Event Mask Registers. Bits 0 and 1 of these registers enable or mask the effect of a GPIO assertion on Fan 1 and Fan 2 speed.

Registers 58h and 59h are AIN Event Mask Registers. Bits 0 and 1 of these registers enable or mask the effect of an AIN out-of-limit event on Fan 1 and Fan 2 speed.

Modes of Operation

The ADM1029 has three different modes of operation. These modes determine the behavior of the system.

1. PWM Duty Cycle Select Mode (directly sets fan speed under software control)
2. Thermal Trip Mode
3. Automatic Fan Speed Control Mode

PWM Duty Cycle Select Mode

The ADM1029 may be operated under software control by clearing bits <1:0> of the three Temp Cooling Action Registers (Reg 0x48, 0x49, 0x4A). Once under Software Control, each fan speed may be controlled by programming values of PWM Duty Cycle in to the devn3 Tw. V.0199 Tc0 8 0 TD0 TD-.ea

It is recommended that the minimum PWM duty cycle be set to 33% (0x05). This has been determined to be the lowest PWM duty cycle that most fans will run reliably at. Note that the PWM duty cycle values programmed in to these registers also define the PWM duty cycle that the fans will turn on at, in Automatic Fan Speed Control Mode. It is recommended that after power-up, the PWM duty cycle is set to 33% before enabling Automatic Fan Speed Control.

Thermal Trip Mode

The ADM1029 can thermally trip the fan(s) for simple on/off fan control, or 2-speed fan control. For example, a fan can be programmed to run at 33% duty cycle. If the temperature exceeds the high temperature limit set for that temperature channel, the fan can automatically trip and run at Alarm Speed. The fan will continue to run at Alarm Speed even if the temperature error condition subsides, until the Latch Temp Fault bit (Bit 7 of the Temp x Fault Action Reg) is cleared in software by writing a 0 to it. To configure Fan 1 normally, run at 33% but to thermally trip to Alarm Speed for a Remote 2 measured temperature of 70 C, set up the following registers:

1. Configure the normal PWM duty cycle for Fan 1 to 33%.

The T_{RANGE} parameter actually defines the fan speed versus temperature slope of the control loop.

3. **T_{MAX}**. This is defined as the temperature at which a fan will be at its maximum speed. At this temperature, the PWM duty cycle driving the fan will be 100%. T_{MAX} is given by T_{MIN} + T_{RANGE}. Since this parameter is the sum of the T_{MIN} and T_{RANGE} parameters, it does *not* need to be programmed into a register on-chip.
4. Programmable hysteresis is included in the control loop to prevent the fans continuously switching on and off if the temperature is close to T_{MIN}. The fans will continue to run until such time as the temperature drops below T_{MIN}–T_{HYST}. The four MSBs of the T_{RANGE}/T_{HYST} registers (Registers 0x88, 0x89, 0x8A) contain a temperature hysteresis value that can be programmed from 0001 to 1111. This allows a temperature hysteresis range from 1 C to 15 C for each temperature measurement channel.

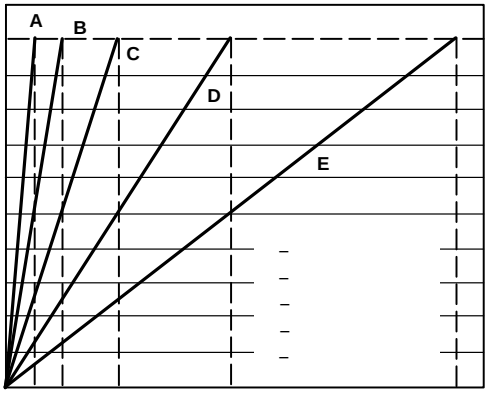


Figure 30. PWM Duty Cycle vs. Temperature Slopes (T_{RANGE})

Figure 30 shows the different control slopes determined by the T_{RANGE} value chosen, and programmed in to the ADM1029. T_{MIN} was set to 0 C to start all slopes from the same point. It can be seen how changing the T_{RANGE} value affects the PWM Duty Cycle vs. Temperature Slope.

Figure 31 shows how for a given T_{RANGE}, changing the T_{MIN} value affects the loop. Increasing the T_{MIN} value will increase the T_{MAX} (temperature at which the fan runs full speed) value, since T_{MAX} = T_{MIN} + T_{RANGE}. Note, however, that the PWM Duty Cycle versus Temperature slope remains exactly the same. Changing the T_{MIN} value merely shifts the control slope.

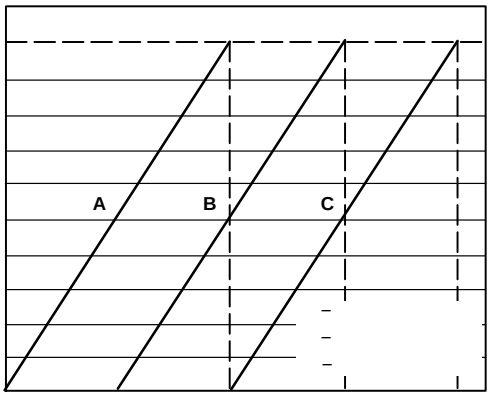


Figure 31. Effect of Increasing T_{MIN} Value on Control Loop

Fan Spin-up

As previously mentioned, once the temperature being measured exceeds the T_{MIN} value programmed, the fan will turn on at minimum speed (default = 33% duty cycle). However, the problem with fans being driven by PWM is

Speed Control Mode by writing to the three Temperature Cooling Action Registers (Registers 0x48, 0x49, 0x4A).

T_{MIN} was defined as being the temperature at which a fan switched on and ran at minimum speed. This minimum speed should be set to 33%. If the minimum PWM duty cycle is programmed to 33%, the fan control loops will operate as previously described.

It should be noted, however, that changing the minimum PWM duty cycle affects the control loop behavior.

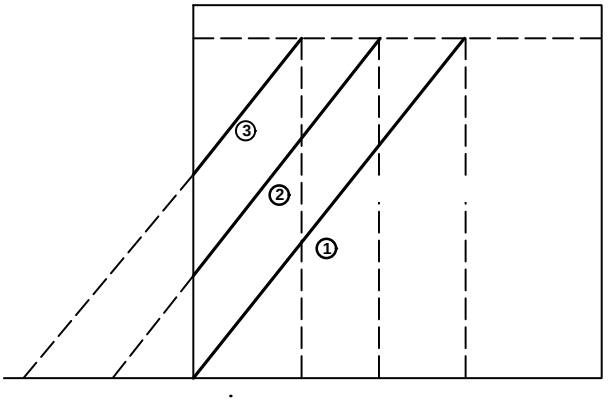


Figure 34. Effect of Changing Minimum Duty Cycle on Control Loop with T_{MIN} and T_{RANGE} Values

Table 12. PWM DUTY CYCLE SELECT MODE

Decimal Value	PWM Duty Cycle

Slope 1 of Figure 34 shows T_{MIN} set to 0 C and the T_{RANGE} chosen is 40 C. In this case, the fan's PWM duty cycle will vary over the range 33% to 100%. The fan will run full speed at 40 C. If the minimum PWM duty cycle at which the fan runs at T_{MIN} is changed, its effect can be seen on Slopes 2 and 3. Take Case 2, where the minimum PWM duty cycle is reprogrammed from 33% (default) to 53%. The fan will actually reacT5=aɲimum PWM7nMIN

ADM1029

Table 13. RESISTOR RATIOS FOR SETTING T_{MIN} AND NUMBER OF FANS INSTALLED USING TMIN/INSTALL PIN (PIN 18)

3 MSBs of ADC	Ideal Ratio R2/(R1 + R2)	R1 (kΩ)	R2 (kΩ)	Actual R2/(R1 + R2)	Error (%)	T_{MIN}	Fans Installed
					–		
					–		
			q				

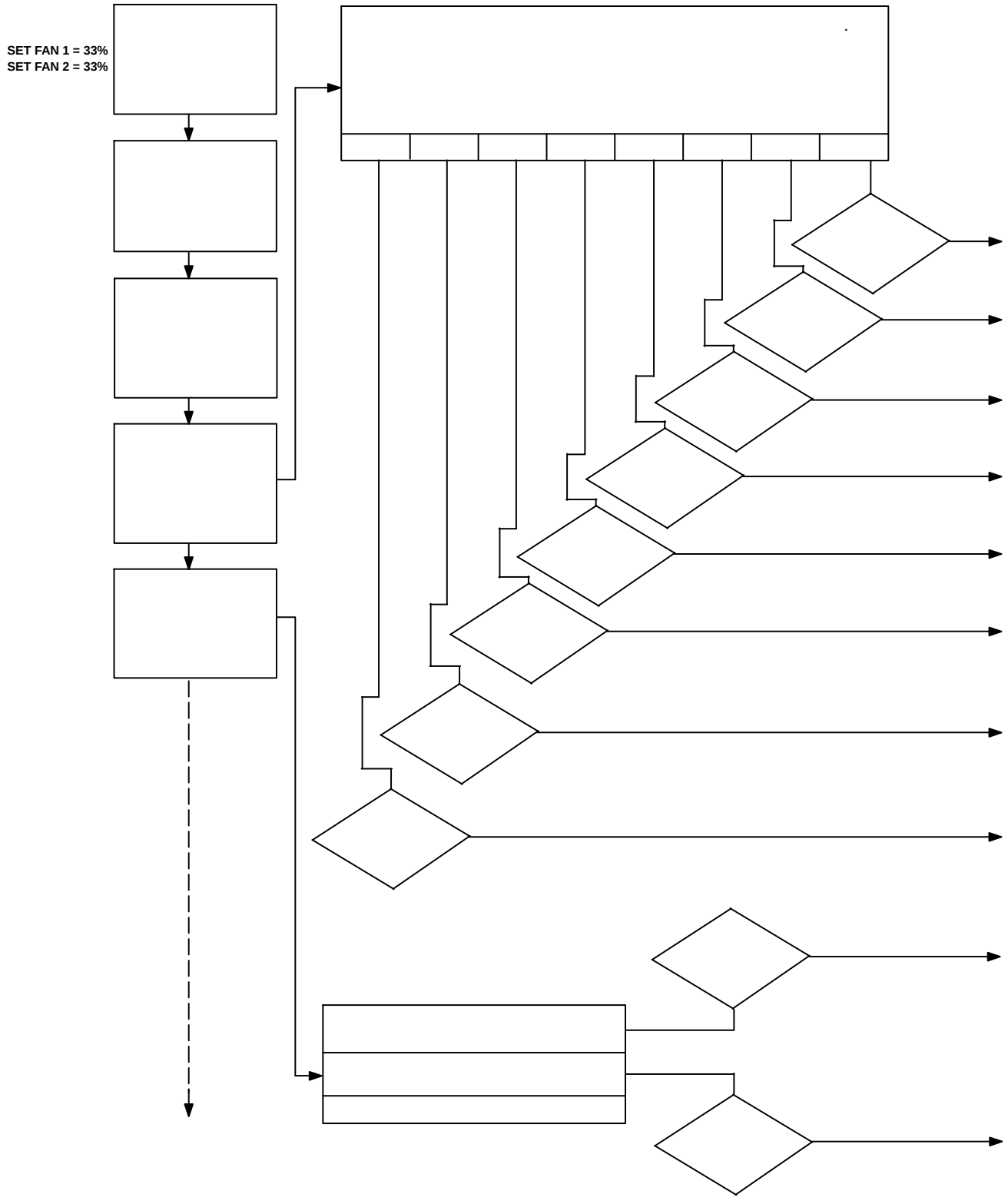


Figure 36. Fan Configuration Flowchart

Fan 2 is turned off. Fan 2 is then run at 100% with Fan 1 turned off. Both fans are then spun-up for the Fan Spin-up time. Note that the Hotplug Latch bit and Missing Latch bit remains set (Bits 7 and 1). These need to be cleared to 0

General Purpose Logic Input/Outputs

The ADM1029 has six dual-function pins (see Pin Function Descriptions section) that may be configured as general-purpose Logic I/O pins by setting the appropriate bit(s) of the GPIO Present/AIN Register (address 05h) or as their alternate functions by clearing these bits.

When configured as GPIO pins, each GPIO pin has a Behavior Register associated with it (Registers 28h to 2Eh) that may be used to configure the operation of the pin.

The GPIO pins may be configured as inputs or outputs. When used as inputs, they may be configured to:

Be Active High or Active Low

Set/Clear a Bit in the Behavior Register when GP Input Is Asserted/Deasserted

Latch a Bit In the Behavior Register when GP Input Is Asserted (Must Be Cleared by Software)

Assert $\overline{\text{CFAULT}}$ when GP Input Asserted

Assert $\overline{\text{INT}}$ when GP Input Asserted

Set Fan(s) to Alarm Speed when GP Input Asserted

Set Fan(s) to Hot-plug Speed when GP Input Asserted

When Used as Outputs, They May Be Configured to:

Be Active High or Low

Be Asserted If a High Temperature Limit Is Exceeded

Be Asserted If a Temperature Measurement Falls Below a Low Limit

Be Asserted If a Fan Fault Is Detected

Be Asserted If a Fan Tach Limit Is Exceeded

Be Asserted If an AIN High Limit Is Exceeded

Be Asserted If an Analog Input Falls Below a Low Limit

Figure 39 shows how to configure the GPIO pins to handle different out-of-limit and fault events.

$\overline{\text{CFAULT}}$ Output

The Cascade Fault output ($\overline{\text{CFAULT}}$), is an open-drain, active low output, intended to communicate fault conditions to other ADM1029s in a system, without the intervention of the host processor. The other ADM1029's may then adjust their fans' speed to compensate, depending on the settings of various registers.

$\overline{\text{CFAULT}}$ is asserted if any of the following conditions occurs:

A Hot-plug Event

Setting Bit 5 of the Configuration Register (Address 01h) forces $\overline{\text{CFAULT}}$ to be asserted

When a GPIO pin is configured as an input by setting Bit 0 of the corresponding GPIO Behavior Register and Bit 2 of the GPIO Behavior Register is also set, $\overline{\text{CFAULT}}$ will be asserted when the logic input is asserted (high or low depending on the polarity bit, Bit 1 of the corresponding GPIO Behavior Register)

If Bit 0 of a Temp. Fault Action Register is set (40h Local Sensor, 41h Remote 1, 42h Remote 2), $\overline{\text{CFAULT}}$ will be asserted if the corresponding temperature high limit is exceeded

If Bit 4 of a Temp. Fault Action Register is set, $\overline{\text{CFAULT}}$ will be asserted if a temperature input crosses the corresponding temperature low limit, the direction depending on the setting of Bit 3 of the Temp. Fault Action Register. (0 = $\overline{\text{CFAULT}}$ when input goes below low limit, 1 = $\overline{\text{CFAULT}}$ when input goes above low limit)

If Bit 0 of a Fan Fault Action Register (18h or 19h) is set, $\overline{\text{CFAULT}}$ will be asserted when a tach measurement for the corresponding fan exceeds the set limit

If Bit 0 of a Fan Fault Action Register (18h or 19h) is set, $\overline{\text{CFAULT}}$ will be asserted, when the fan fault input pin for the corresponding fan is asserted (low)

If Bit 0 of an AIN Behavior Register is set (50h AIN0, 51h AIN1), $\overline{\text{CFAULT}}$ will be asserted if the corresponding AIN high limit is exceeded

If Bit 4 of an AIN Behavior Register is set, $\overline{\text{CFAULT}}$ will be asserted if an analog input crosses the corresponding AIN low limit, the direction depending on the setting of Bit 3 of the AIN Behavior Register. (0 = $\overline{\text{CFAULT}}$ when input goes below low limit, 1 = $\overline{\text{CFAULT}}$ when input goes above low limit).

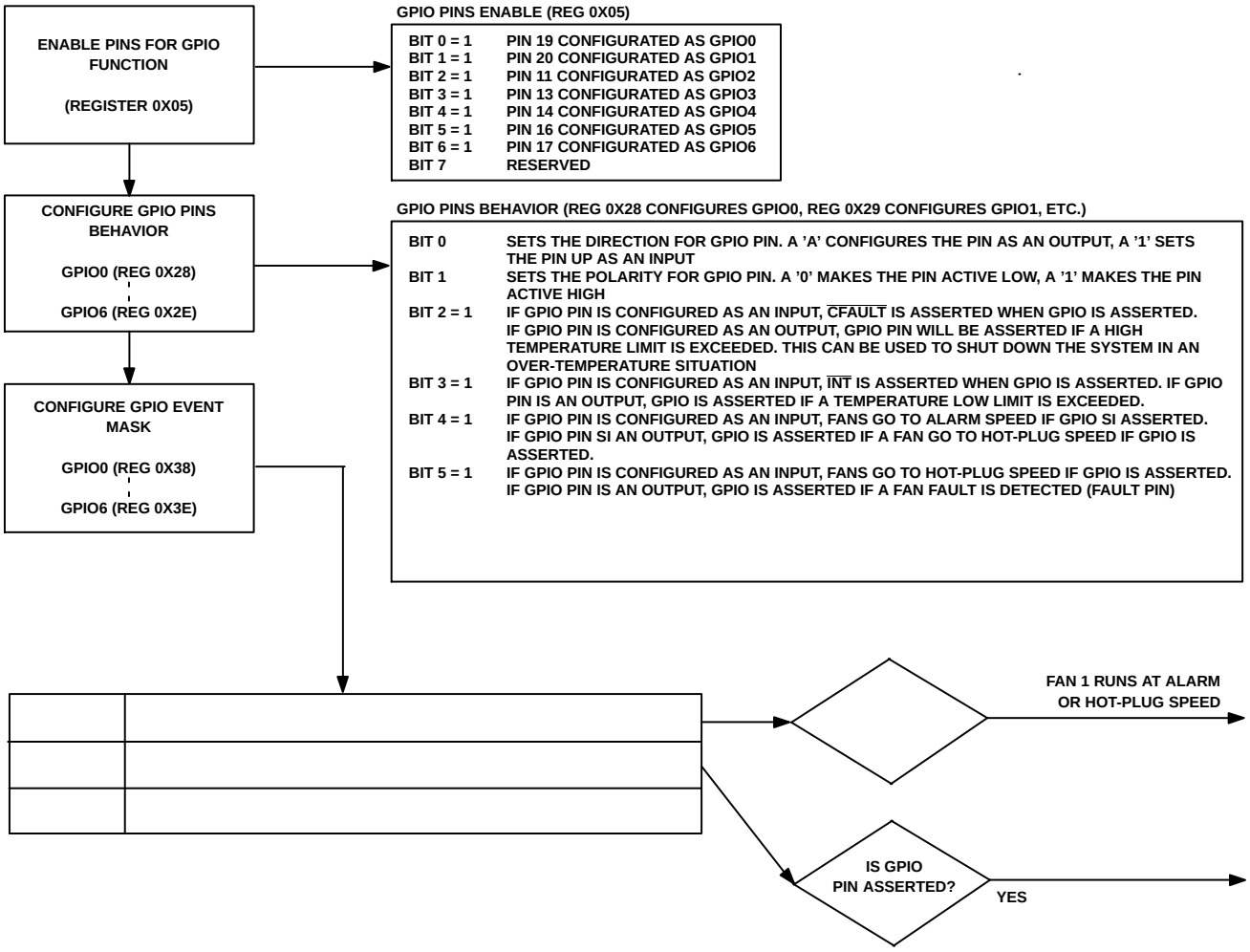


Figure 39. Configuring GPIO Pins

Table 15. REGISTER MAP

Address	Name	Default Value	Description

Table 15. REGISTER MAP

Address	Name	Default Value	Description

Table 15. REGISTER MAP

Address	Name	Default Value	Description

ADM1029

Table 18. REGISTER 07H – SET FAN X* ALARM SPEED (POWER-ON DEFAULT 00H)

Bit	Name	R/W	Description

STATUS REGISTERS

Table 21. REGISTER 00H – STATUS REGISTER (POWER-ON DEFAULT 00H)

Bit	Name	R/W	Description

Table 24. REGISTER 04H – GPIOS SUPPORTED BY CONTROLLER (POWER-ON DEFAULT 7FH)

Bit	Name	R/W	Description

TEMPERATURE REGISTERS

Table 27. REGISTER 06H – TEMP DEVICES INSTALLED (POWER-ON DEFAULT 0000 0??1)

Bit	Name	R/W	Description

Table 28. REGISTER 30H, 31H, 32H – TEMP X OFFSET REGISTERS (POWER-ON DEFAULT 00H)

Bit	Name	R/W	Description

Table 29. REGISTER 40H, 41H, 42H – TEMP X* FAULT ACTION (POWER-ON DEFAULT 08H)

Bit	Name	R/W	Description

Table 30. REGISTER 48H, 49H, 4AH – TEMP X* COOLING ACTION (POWER-ON DEFAULT 00H)

Bit	Name	R/W	Description
			*
			*
			*
			*

Table 32. REGISTER 88H, 89H, 8AH TEMP X* T_{RANGE}/T_{HYST} (POWER-ON DEFAULT 51H)

Bit	Name	R/W	Description
	*		* Bits <3:0> T_{RANGE}
	*		* * * *

Table 33. REGISTER 90H, 91H, 92H – TEMP X* HIGH LIMIT (POWER-ON DEFAULT 80 C FOR LOCAL SENSOR, 100 C FOR REMOTE SENSORS)

Bit	Name	R/W	Description
	*		*

Table 34. REGISTER 98H, 99H, 9AH – TEMP X* LOW LIMIT (POWER-ON DEFAULT 60 C FOR LOCAL SENSOR, 70 C FOR REMOTE SENSORS)

Bit	Name	R/W	Description
	*		*

Table 35. REGISTER A0H, A1H, A2H – TEMP X* MEASURED VALUE (POWER−ON DEFAULT 00H)

Bit	Name	R/W	Description
	*		*

FAN REGISTERS

Table 36. REGISTER 02H – FAN SUPPORTED BY CONTROLLER (POWER-ON DEFAULT 03H)

Bit	Name	R/W	Description

Table 37. REGISTER 03H – FANS SUPPORTED IN SYSTEM (POWER-ON DEFAULT 0000 00?1)

Bit	Name	R/W	Description

Table 38. REGISTER 07H – SET FAN X ALARM SPEED (POWER-ON DEFAULT 00H)

Bit	Name	R/W	Description

Table 40. REGISTER 09H – SET FAN X FULL SPEED (POWER-ON DEFAULT 00H)

Bit	Name	R/W	Description

Table 41. REGISTER 0CH – FAN SPIN-UP REGISTER (POWER-ON DEFAULT 03H)

Bit	Name	R/W	Description

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Table 46. REGISTER 68H, 69H – FAN X* CONFIGURATION (POWER-ON DEFAULT 2FH)

Bit	Name	R/W	Description
	*		* *
			* **Bits 5–4 PWM Freq**
			* * **Bit 7 Bit 6 Oscillator Frequency (Hz)**

Table 47. REGISTER 70H, 71H – FAN X* TACH VALUE (POWER-ON DEFAULT 00H)

Bit	Name	R/W	Description
	*		*

Table 48. REGISTER 78H, 79H – FAN X* TACH HIGH LIMIT (POWER-ON DEFAULT FFH)

Bit	Name	R/W	Description
	*		*

GPIO REGISTERS

Table 49. REGISTER 04H – GPIOS SUPPORTED BY CONTROLLER (POWER-ON DEFAULT 7FH)

Bit	Name	R/W	Description

Table 51. REGISTER 28H, 29H, 2AH, 2BH, 2CH, 2DH, 2EH – GPIOX* BEHAVIOR (POWER-ON DEFAULT 00H)

Bit	Name	R/W	Description
			* * *
			* * *
			* *
			* * * *
			* * * * *
			* * * * *
			* * *
			* *

Table 52. REGISTER 38H, 39H, 3AH, 3BH, 3CH, 3DH, 3EH – GPIOX* EVENT MASK (POWER-ON DEFAULT 00H)

Bit	Name	R/W	Description
			*
			*

AIN REGISTERS

Table 53. REGISTER 05H – GPIO PRESENT/AIN (POWER-ON DEFAULT 0????111)

Bit	Name	R/W	Description

Table 55. REGISTER 58H, 59H – AINX* EVENT MASK (POWER-ON DEFAULT 00H)

Bit	Name	R/W	Description
			*
			*

Table 56. REGISTER A8H, A9H – AINX* HIGH LIMIT (POWER-ON DEFAULT FFH)

Bit	Name	R/W	Description
	*		*

Table 57. REGISTER B0H, B1H – AINX* LOW LIMIT (POWER-ON DEFAULT 00H)

Bit	Name	R/W	Description
	*		*

Table 58. REGISTER B8H, B9H – AINX* MEASURED VALUE (POWER-ON DEFAULT 00H)

Bit	Name	R/W	Description
	*		*

MISCELLANEOUS REGISTERS

Table 59. REGISTER 0BH – S/W RESET (POWER-ON DEFAULT 00H)

Bit	Name	R/W	Description

Table 60. REGISTER 0DH – MANUFACTURER'S ID (POWER-ON DEFAULT 41H)

Bit	Name	R/W	Description

Table 61. REGISTER 0EH – REVISION (POWER-ON DEFAULT 00H)

Bit	Name	R/W	Description

Table 62. REGISTER 0FH – MANUFACTURER'S TEST REGISTER (POWER-ON DEFAULT 00H)

Bit	Name	R/W	Description

Table 63. ORDERING INFORMATION TABLE

Model*	Temperature Range	Package Type	Package Option	Shipping
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QSOP24 NB
CASE 492B−01
ISSUE A

DATE 06 MAY 2008

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