# ADM1033

# Thermal Monitor and Fan Speed (RPM) Controller

The ADM1033 is a one channel remote- and local-temperature sensor and fan controller. The remote channel monitors the temperature of the remote thermal diode, which may be discrete 2N3904/6s or may be located on a microprocessor die. The device also monitors its own ambient temperature.

The ADM1033 can monitor and control the speed of cooling fan. The user can program a target fan speed, or else use the look-up table to input a temperature-to-fan speed profile. The look-up table can be configured to run the fans at discrete speeds (discrete mode) or to ramp the fan speed with temperature (linear mode).

The ADM1033 communicates over a 2-wire SMBus 2.0 interface. An 8-level LOCATION input allows the user to choose between SMBus 1.1 and SMBus 2.0. An $\overline{\text{ALERT}}$ output indicates error conditions. The $\overline{\text{THERM}}$ I/O signals overtemperature as an output and times $\overline{\text{THERM}}$ assertions as an input. Pin 8 can be configured as a reference for the $\overline{\text{THERM}}$ ($\overline{\text{PROCHOT}}$) input.

**Features**

- 1 Local and Remote Temperature Channels
- 1 C Accuracy on Local and Remote Channels
- Automatic Remote Temperature Channel, Up to 1 kΩ
- Fast (Up to 64 Measurements per Second)
- SMBus 2.0, 1.1, and 1.0 Compliant
- SMBus Address Input/LOCATION Input to UDID
- Programmable Over/Undertemperature Limits
- Programmable Fault Queue
- $\overline{\text{SMBusALERT}}$ Output
- Fail-Safe Overtemperature Comparator Output
- Fan Speed (RPM) Controller
- Look-up Table for Temperature-to-Fan Speed Control
- Linear and Discrete Options for Look-up Table
- $\overline{\text{FAN\_FAULT}}$ Output
- $\overline{\text{THERM}}$ Input, Used to Time $\overline{\text{PROCHOT}}$ Assertions
- REF Input, Used as Reference for $\overline{\text{THERM}}$ ($\overline{\text{PROCHOT}}$)
- 3.0 V to 5.5 V Supply
- Small 16-lead QSOP Package
- This is a Pb-Free Device*

**Applications**

- Desktop and Notebook PCs
- Embedded Systems
- Telecommunications Equipment
- LCD Projectors

* For additional information on our Pb-Free strategy and soldering details, please

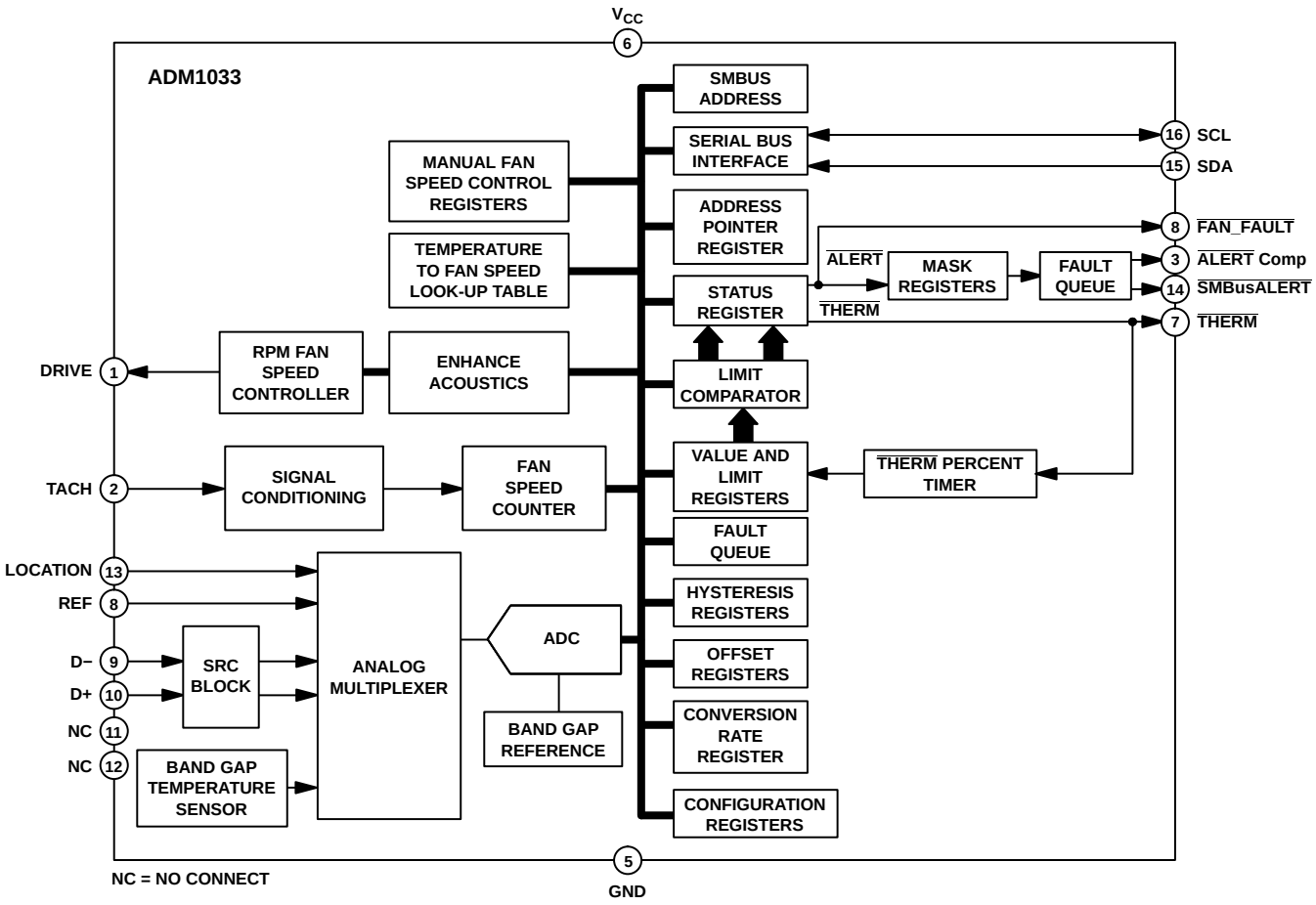



**Figure 1. Functional Block Diagram**

**Table 1. ABSOLUTE MAXIMUM RATINGS**

| Parameter | Rating | Unit |
|---|---|---|
| Positive Supply Voltage ($V_{CC}$) | −0.3, +6.5 | V |
| Voltage on Any Input or Output Pin except $\overline{\text{FAN\_FAULT}}$ and LOCATION | −0.3 to $V_{DD}$ + 6.5 | V |
| Voltage on $\overline{\text{FAN\_FAULT}}$ (Note 1) | $V_{CC}$ | |
| Voltage on LOCATION | $V_{CC}$ + 0.3 | V |
| Input Current at Any Pin | 20 | mA |
| Maximum Junction Temperature ($T_{J\ MAX}$) | 150 | C |
| Storage Temperature Range | −65 to +150 | C |
| Lead Temperature, Soldering (10 s) | 300 | C |
| IR Reflow Peak Temperature | 220 | C |
| ESD Rating − All Pins | 1500 | V |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the

**Table 2. THERMAL CHARACTERISTICS**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 16-lead QSOP Package | 150 | 39 | C/W |

**Table 3. PIN ASSIGNMENT**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | DRIVE1 | DRIVE1 Pin Drives Fan 1. Open-drain output. Requires a pullup resistor. |
| 2 | TACH1 | Fan 1 Fan Speed Measurement Input. Connects to the fan's TACH output to measure the fan speed. |
| 3 | $\overline{\text{ALERT}}$ Comp | Open-Drain Active Low Output. Assets low whenever a measurement goes outside its programmed limits if not masked. Automatically goes high again when the measured parameter falls back within its limits. |
| 4 | NC | No Connect. |
| 5 | GND | |

**Table 4. ELECTRICAL CHARACTERISTICS** ($T_A = T_{MIN}$ to $T_{MAX}$, $V_{CC} = V_{MIN}$ to $V_{MAX}$, unless otherwise noted.) (Note 1)

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Power Supply** | | | | | |
| Supply Voltage, $V_{CC}$ (Note 2) | | 3.0 | 3.30 | 3.6 | V |
| Supply Current, $I_{CC}$ | Interface inactive, ADC Active | − | − | 3.0 | mA |
| | Standby Mode | − | − | 900 | μA |
| Undervoltage Lockout Threshold | | − | 2.5 | − | V |
| Power-On Reset Threshold | | 1.0 | − | 2.4 | V |
| **Temperature-to Digital Converter** | | | | | |
| Internal Sensor Accuracy | 20 C $T_A$ 60 C<br>−40 C $T_A$ +100 C | −<br>−4.0 | 1.0<br>− | 2.0<br>+2.0 | C |
| Resolution | | − | 0.03125 | − | C |
| External Diode Sensor Accuracy | −40 C $T_D$ +100 C; $T_A$ = +40 C<br>−40 C $T_D$ +100 C; +20 C $T_A$ +60 C<br>−40 C $T_D$ +100 C; −40 C $T_A$ +100 C | −<br>−<br>−3.0 | 0.5<br>1.0<br>− | 1.0<br>1.25<br>+2.0 | C |
| Resolution | | − | 0.03125 | − | C |
| Remote Sensor Source Current | High Level<br>Mid Level<br>Low Level | −<br>−<br>− | 85<br>34<br>5.0 | −<br>−<br>− | μA |
| Series Resistance Cancellation | | − | − | 1000 | Ω |
| Power Supply Sensitivity | | − | 1.0 | − | %/V |
| Conversion Time (Local Temperature) | Averaging Enabled | − | 11 | − | ms |
| Conversion Time (Remote Temperature) | Averaging Enabled | − | 32 | − | ms |
| Total Conversion Time | Averaging Enabled | − | 43 | − | ms |
| **Open-Drain Digital Outputs ($\overline{\text{ALERT}}$, $\overline{\text{THERM}}$** | | | | | |

## TYPICAL PERFORMANCE CHARACTERISTICS

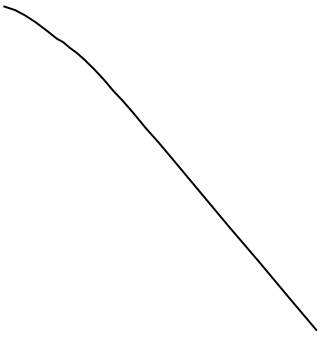


**Figure 3. Temperature Error vs. PCB Track Resistance DXP to GND and $V_{CC}$**

**Figure 4. Remote Temperature Error vs. D+, D− Capacitance**

**Figure 5. Remote Temperature Error vs. Series Resistance on D+ and D−**

# ADM1033

### Functional Description

The ADM1033 is a local- and remote-temperature monitor and fan controller for use in a variety of applications, including microprocessor-based systems. The device accurately monitors remote and ambient temperature and uses that information to quietly control the speed of a cooling fan. Whenever a fan stalls, the device asserts a $\overline{\text{FAN\_FAULT}}$ output.

The ADM1033 features a $\overline{\text{THERM}}$ I/O. As an input, this measures assertions on the $\overline{\text{THERM}}$ pin. As an output, it asserts a low signal to indicate when the measured temperature exceeds the programmed $\overline{\text{THERM}}$ temperature. The ADM1033 communicates over an SMBus 2.0 interface. Its LOCATION input determines which version of SMBus to use, as well as the SMBus address (in fixed and discoverable mode) and the LOCATION bits in the UDID (in ARP-capable mode).

### Internal Registers

Table 5 gives a brief description of the ADM1033's principal internal registers. For more detailed information on the function of each register, refer to Table 35.

### Serial Bus Interface

The ADM1033 communicates with the master via the 2-wire SMBus 2.0 interface. It supports two versions of SMBus 2.0, determined by the value of the LOCATION input's resistors.

The first version is fully ARP-capable. This means that it supports address resolution protocol (ARP), allowing the master to dynamically address the device on powerup. It responds to ARP commands such as "Prepare to ARP."

The second SMBus version, fixed and discoverable, is backwards compatible with SMBus 1.0 and 1.1. In this mode, the ADM1033 powers up with a fixed address, which is determined by the state of the LOCATION pin on powerup.

NOTE: When using the ADM1033, Addresses 0xC2 and 0xCA should not be used by any other device on the bus.

### Location Input

The LOCATION input is a resistor divider input. It has multiple functions and can specify the SMBus version (in fixed and discoverable or ARP-capable modes); the SMBus address (in fixed and discoverable mode); and the LLL bits (in UDID in ARP-capable mode).

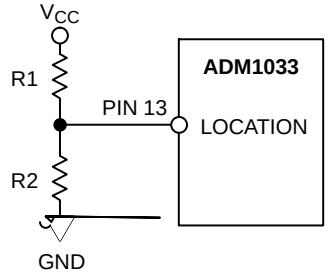



**Figure 15. Bootstrapping the LOCATION Input**

The voltage of this 8-level input is set by a potential divider. The voltage on LOCATION is sampled on powerup and digitized by the on-chip ADC to determine the LOCATION input value. Because the LOCATION input is sampled only at powerup, changes made while power is applied have no effect.

### SMBus 2.0 ARP-Capable Mode

In ARP-capable mode, the ADM1033 supports features such as address resolution protocol (ARP) and unique device identifier (UDID). The UDID is a 128-bit message that describes the ADM1033's capabilities to the master. The UDID also includes a vendor specific ID for functionally equivalent devices.

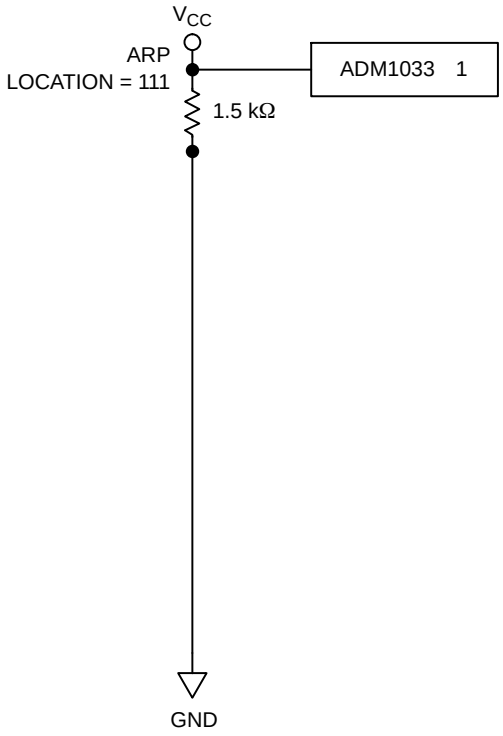



**Figure 16. Setting Up Multiple ADM1033 Addresses in SMBus 2.0 ARP-capable Mode**

### SMBus 2.0 Fixed and Discoverable Mode

The ADM1033 also supports fixed and discoverable mode, which is backwards compatible with SMBus 1.0 and 1.1. Fixed and discoverable mode supports all the same functionality as ARP-capable mode, except for assign address in which case it powers up with a fixed address and is not changed by the assign address call. The fixed address is determined by the state of the LOCATION pin on powerup.

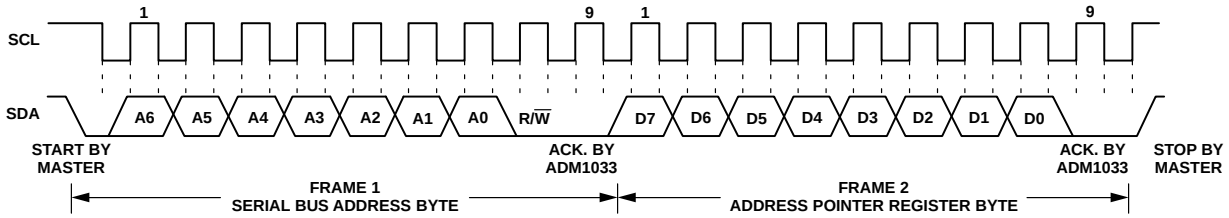



**Figure 18. Writing to the Address Pointer Register Only (Send Byte)**

### Block Write

In this operation, the master device writes a block of data to a slave address as follows. A maximum of 32 bytes can be written.

1. The master asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by a write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends the register address. The register address sets up the address pointer register and determines whether a block write (MSB = 1) or a byte write (MSB = 0) takes place.
5. The slave asserts ACK on SDA.
6. The master sends the byte count.
7. The slave asserts ACK on SDA.
8. The master sends N data bytes.
9. The slave asserts ACK on SDA after each byte.
10. The master asserts a stop condition on SDA to end the transaction.

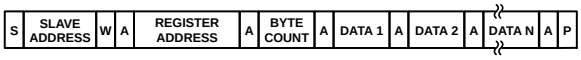



**Figure 22. Block Write to RAM**

## Read Operations

### Receive Byte

This is useful when repeatedly reading a single register. The register address must be set up prior to this, with the MSB at 0 to read a single byte. In this operation, the master device receives a single byte from a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts ACK on SDA.
4. The master receives a data byte.
5. The master sends NO ACK on SDA.
6. The master asserts a stop condition on SDA, and the transaction ends.

In the ADM1033, the receive byte protocol is used to read a single byte from a register whose address has previously been set by a send byte or write byte operation.


**Figure 23. Receive Byte**

### Block Read

In this operation, the master reads a block of data from a slave device. The number of bytes to be read must be set in advance. To do this, use a write byte operation to the #Bytes/Block Read Register at Address 0x00. The register address determines whether a block-read or a read-byte operation is to be completed (set MSB to 1 to specify a block-read operation). A maximum of 32 bytes can be read.

1. The master asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends the register address (MSB = 1).
5. The slave asserts ACK on SDA.
6. The master asserts a repeated start on SDA.
7. The master sends the 7-bit slave address followed by the read bit (high).
8. The slave asserts ACK on SDA.
9. The slave sends the byte count.
10. The master asserts ACK on SDA.
11. The slave sends N data bytes.
12. The master asserts ACK on SDA after each data byte.
13. The master does not acknowledge after the Nth data byte.
14. The master asserts a stop condition on SDA to end the transaction.


**Figure 24. Block Read from RAM**

# ADM1033

If the sensor is used in a very noisy environment, a capacitor value up to 1000 pF may be placed between the D+ and Dǐ inputs to filter the noise. However, additional parasitic capacitance on the lines between D+, Dǐ, and the thermal diode should also be considered. The total capacitance should never be greater than 1000 pF.

To measure each $\Delta V_{BE}$, the sensor is switched between operating currents of I, (N1 I), and (N2 I). The resulting waveform is passed through a 65 kHz low-pass filter to remove noise, then to a chopper-stabilized amplifier that amplifies and rectifies the waveform. This produces a dc voltage proportional to $\Delta V_{BE}$. These voltage measurements determine the temperature of the thermal diode, while automatically compensating for any series resistance on the D+ and/or Dǐ lines. The temperature is stored in two registers as a 13-bit word.

To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles at conversion rates of less than or equal to 8 Hz. An external temperature measurement takes nominally 32 ms when averaging is enabled and 6 ms when averaging is disabled.

One LSB of the ADC corresponds to 0.03125 C. The ADM1033 can theoretically measure temperatures from ǐ64 C to +191.96875 C, although these are outside its operating range. The extended temperature resolution data format is shown in Table 9. The data for the local and remote channels is stored in the extended temperature resolution registers (Reg. 0x40 = Local, Reg. 0x42 = Remote 1).

**Table 10. TEMPERATURE MEASUREMENT REGISTERS**

| Register | Description | Default |
|---|---|---|
| 0x40 | Local Temperature, LSBs | 0x00 |
| 0x41 | Local Temperature, MSBs | 0x00 |
| 0x42 | Remote 1 Temperature, LSBs | 0x00 |
| 0x43 | Remote 1 Temperature, MSBs | 0x00 |

High and low temperature limit registers are associated with each temperature measurement channel. Exceeding the programmed high and low limits sets the appropriate status bit. Exceeding either limit can cause an $\overline{\text{SMBusALERT}}$ interrupt.

**Table 11. TEMPERATURE MEASUREMENT LIMIT REGISTERS**

| Register | Description | Default |
|---|---|---|
| 0x0B | Local High Limit | 0x8B (75 C) |
| 0x0C | Local Low Limit | 0x54 (20 C) |
| 0x0D | Local $\overline{\text{THERM}}$ Limit | 0x95 (85 C) |
| 0x0E | Remote 1 High Limit | 0x8B (75 C) |
| 0x0F | Remote 1 Low Limit | 0x54 (20 C) |
| 0x10 | Remote 1 $\overline{\text{THERM}}$ Limit | 0x95 (85 C) |

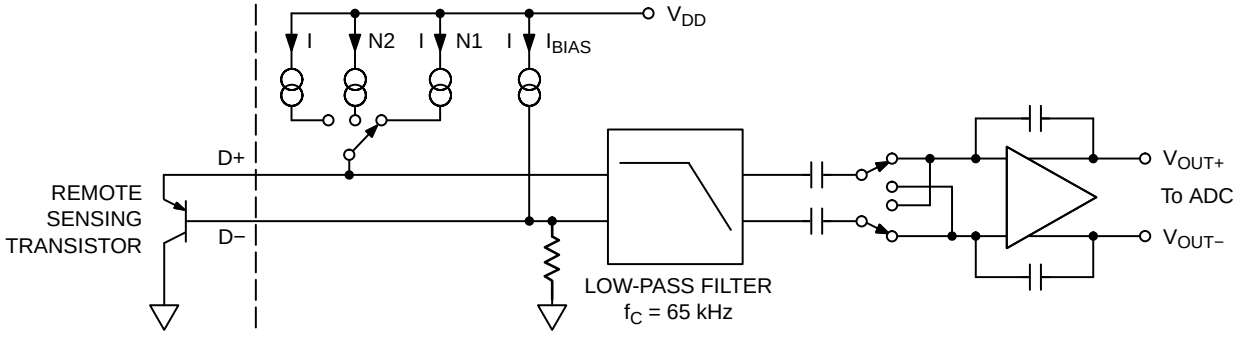



**Figure 27. ADM1033 Signal Conditioning**

**Table 12. CHANNEL SELECTOR**

| Bits 5:4 | Channel Selector (Configuration 2) |
|---|---|
| 00 | Local Channel = Default |
| 01 | Remote 1 Channel |
| 10 | Reserved |
| 11 | Reserved |

### Removing Temperature Errors

As CPUs run faster and faster, it gets more difficult to avoid high frequency clocks when routing the D+ and Dĭ traces around a system board. Even when the recommended layout guidelines are followed, temperature errors attributed to noise coupled onto the D+ and Dĭ lines remain. High frequency noise generally gives temperature measurements that are consistently too high. The ADM1033 has Local and Remote temperature offset registers at 0x16 and 0x17; one for each channel. By completing a one-time calibration, the

The construction of a filter allows the ADM1033 and the remote temperature sensor to operate in noisy environments. Figure 29 shows a low-pass R-C-R filter with the following values: R = 100 Ω and C = 1 nF. This filtering reduces both common-mode noise and differential noise.

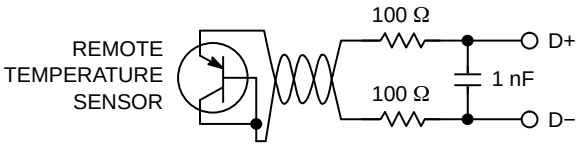



**Figure 29. Filter between Remote Sensor and ADM1033**

## Limits, Status Registers, and Interrupts

High and low limits are associated with each measurement channel on the ADM1033. These can form the basis of system status monitoring. A status bit can be set for any out-of-limit condition and detected by polling the device. Alternatively, $\overline{\text{SMBusALERT}}$s can be generated to flag a processor or microcontroller of an out-of-limit condition.

### 8-bit Limits

The following is a list of all the 8-bit limits on the ADM1033:

**Table 15. TEMPERATURE LIMIT REGISTERS**

| Register | Description | Default |
|---|---|---|
| 0x0B | Local High Limit | 0x8B (75 |

**Table 17. INTERRUPT STATUS REGISTER 1 (REG. 0X4F)**

| Bit # | Name | Description |
|---|---|---|
| 7 | LH | 1 = Local high temperature limit has been exceeded. |
| 6 | LL | 1 = Local low temperature limit has been exceeded. |
| 5 | R1H | 1 = Remote 1 high temperature limit has been exceeded |
| 4 | R1L | 1 = Remote 1 low temperature limit has been exceeded. |
| 3 | R1D | 1 = Remote 1 diode error; indicates an open or short on the D1+/D1− pins. |
| 2 | Unused | Reserved |
| 1 | Unused | Reserved |
| 0 | Unused | Reserved |

**Table 18. STATUS REGISTER 2 (REG. 0X50)**

| Bit # | Name | Description |
|---|---|---|
| 7 | LT | 1 = Local $\overline{\text{THERM}}$ temperature limit has been exceeded. |
| 6 | R1T | 1 = Remote 1 $\overline{\text{THERM}}$ temperature limit has been exceeded. |
| 5 | Unused | Reserved |
| 4 | T% | 1 = $\overline{\text{THERM}}$ % on-time limit has been exceeded. |
| 3 | TA | 1 = One of the $\overline{\text{THERM}}$ limits has been exceeded; and the $\overline{\text{THERM}}$ output signal has been asserted. |
| 2 | TS | 1 = $\overline{\text{THERM}}$ state. Indicates the $\overline{\text{THERM}}$ pin is active; clears on a read if $\overline{\text{THERM}}$ is not active. Does not generate an $\overline{\text{ALERT}}$ in $\overline{\text{ALERT}}$ comp mode. |
| 1 | Res | Reserved |
| 0 | Res | Reserved |

**Table 19. STATUS REGISTER 3 (REG. 0X51)**

| Bit # | Name | Description |
|---|---|---|
| 7 | F1S | 1 = Fan 1 has stalled. |
| 6 | FA | 1 = Fan alarm speed. Fan 1 and Fan 2 are running at alarm speed. |
| 5 | Res | Reserved |
| 4 | Res | Reserved |
| 3 | Res | Reserved |
| 2 | Res | Reserved |
| 1 | Res | Reserved |
| 0 | $\overline{\text{ALERT}}$ | 1 = $\overline{\text{ALERT}}$ low; indicates the $\overline{\text{ALERT}}$ line has been pulled low. |

### $\overline{\text{ALERT}}$ Interrupt Behavior

The ADM1033 generates an $\overline{\text{ALERT}}$ whenever an out-of-limit measurement is made (if it is not masked out). The user can also detect out-of-limit conditions by polling the ADM1033 status registers. It is important to note how the SMBus $\overline{\text{ALERT}}$ output behaves when writing interrupt handler software.

The $\overline{\text{ALERT}}$ output on the ADM1033 can be programmed to operate in either $\overline{\text{SMBusALERT}}$ mode or in comp mode.

In $\overline{\text{SMBusALERT}}$ mode, the $\overline{\text{ALERT}}$ output remains low until the measurement falls back within its programmed limits and either the status register is read or an ARA is completed. In comp mode, the $\overline{\text{ALERT}}$ output automatically resets once the temperature measurement falls back within the programmed limits.

### Configuring the $\overline{\text{ALERT}}$ Output

For $\overline{\text{SMBusALERT}}$ mode, set the $\overline{\text{ALERT}}$ configuration bit (Bit 3) of the Configuration Register 1 (Address 0x01) to 0.

In $\overline{\text{SMBusALERT}}$ mode, a status bit is set when a measurement goes outside of its programmed limit. If the corresponding mask bit is not set, the $\overline{\text{ALERT}}$ output is pulled low. If the measured value falls back within the limits, the $\overline{\text{ALERT}}$ output remains low until the corresponding status register is read or until an ARA is completed (as long as no other measurement is outside its limits).

For comp mode, set the $\overline{\text{ALERT}}$ configuration bit (Bit 3) of Configuration Register 1 (Address 0x01) to1.

In comp mode, the $\overline{\text{ALERT}}$ output is automatically pulled low when a measurement goes outside its programmed limits. Once the measurement falls back within its limits (and assuming no other measurement channel is outside its limits), the $\overline{\text{ALERT}}$ output is automatically pulled high again.

The main difference between the two modes is that the $\overline{\text{SMBusALERT}}$ does not reset without software intervention, whereas the comp mode $\overline{\text{ALERT}}$ output automatically resets.

**Figure 30. $\overline{\text{ALERT}}$ Comparator and $\overline{\text{SMBusALERT}}$**

4. Mask the interrupt source by setting the appropriate mask bit in the interrupt mask registers (from Reg. 0x08 to Reg. 0x0A).
5. Take the appropriate action for a given interrupt source.
6. Exit the interrupt handler.
7. Periodically poll the status register. If the interrupt status bit clears, reset the corresponding interrupt mask bit to 0. The $\overline{\text{SMBusALERT}}$ output and status bits then behave as shown in Figure 31.

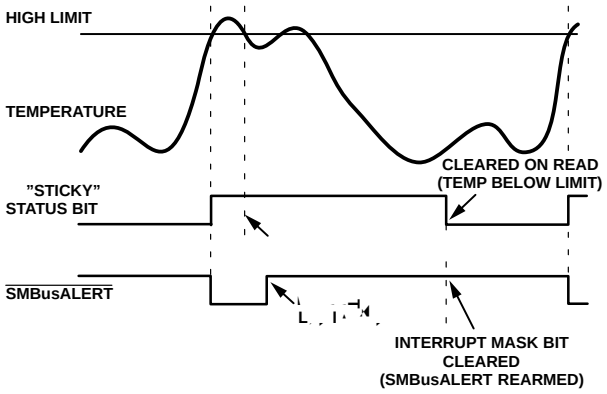



**Figure 31. Handling $\overline{\text{SMBusALERT}}$**

$\overline{\text{THERM}}$ % Exceeded Bit (Bit 4) in Status Register 2 (Address 0x50) is asserted and an $\overline{\text{ALERT}}$ is generated, that is, if the mask bit is not set. If the limit is set to 0x00, an $\overline{\text{ALERT}}$ is generated on the first assertion. If the limit is set to 0xFF, an $\overline{\text{ALERT}}$ is never generated. This is because 0xFF corresponds to the $\overline{\text{THERM}}$ input, which is asserted continuously.

**Table 25. CONVERSION RATES**

| Code | $\overline{\text{THERM}}$ % On-Time Window |
|---|---|
| 000 | 0.25 s |
| 001 | 0.5 s |
| 010 | 1 s |
| 011 | 2 s |
| 100 | 4 s |
| 101 | 8 s |
| 110 | 8 s |
| 111 | 8 s |

When $\overline{\text{THERM}}$ is configured as an input only, setting the Enable $\overline{\text{THERM}}$ Events bits in Configuration Register 4 allows Pin 7 to operate as an I/O.

The user can configure the $\overline{\text{THERM}}$ pin to be pulled low as an output whenever the local temperature exceeds the local $\overline{\text{THERM}}$ limit. To do this, set the Enable Local $\overline{\text{THERM}}$ events bit (Bit 0) of Configuration Register 4 (Address 0x04).

The user can also configure the $\overline{\text{THERM}}$ pin to be pulled low as an output whenever the Remote 1 temperature exceeds the Remote 1 $\overline{\text{THERM}}$ limit. Set the Enable Remote 1 $\overline{\text{THERM}}$ events bit (Bit 1) of Configuration Register 4 (Address 0x04).

### $\overline{\text{THERM}}$ % Limit Register

The $\overline{\text{THERM}}$ % limit is programmed to Register 0x19. An $\overline{\text{ALERT}}$ is generated, if $\overline{\text{THERM}}$ is asserted for longer than the programmed percentage limit. The limit is programmed as a percentage of the chosen time window.

$\overline{\text{THERM}}$ % limit register is an 8-bit register.

0x00 = 0%

0xFF = 100%

Therefore, 1 LSB = 0.39%.

Example:

If a time window of 8 seconds is chosen, and an $\overline{\text{ALERT}}$ is to be generated if $\overline{\text{THERM}}$ is asserted for more than

signal and waits for a transition on the TACH signal. When a transition takes place on the TACH signal, the PWM drive is switched off for a period of time called $t_{off}$. The drive signal is then switched on again. The toff time is varied in order to vary the fan speed. If the fan is running too fast, the toff time is increased. If the fan is running too slow, the toff time is decreased.

Since the drive signal is synchronized with the TACH

R1 and R2 should be chosen such that

$$2\ V < V_{PULLUP} \times R2/(R_{PULLUP} + R1 + R2) < 5\ V \quad \text{(eq. 3)}$$

RPM = (81920  60) / 6143
Fan Speed = 800 RPM

### Alarm Speed

The fan ALARM speed (Bit 6) in Status Register 3 (Address 0x51) is set whenever the fan runs at alarm speed. This occurs if the device is programmed to run the fan at full speed whenever the $\overline{\text{THERM}}$ temperature limits are exceeded. The device runs at alarm speed, for example, if the Boost Disable bit (Bit 1) of the Configuration 2 Register (Address 0x02) is not set to 1.

### Fan Response Register

The ADM1033 fan speed controller operates by reading the current fan speed, comparing it with the programmed fan speed, and then updating the drive signal applied to the fan. The rate at which the ADM1033 looks at and updates the drive signal is determined by the fan response register. Different fans have different inertias and respond to a changing drive signal more or less quickly than others. The fan response register allows the user to tailor the ADM1033 to a particular fan to prevent situations like overshoot.

The user programs the number of updates the ADM1033 can make to the drive signal per second. Table 27 lists the available options.

**Table 27. FAN RESPONSE CODES**

| Code | Update Rate |
|---|---|
| 000 | 1.25 Updates/Second |
| 001 | 2.5 Updates/Second = Default |
| 010 | 5 Updates/Second |
| 011 | 10 Updates/Second |
| 100 | 20 Updates/Second |
| 101 | 40 Updates/Second |
| 110 | 80 Updates/Second |
| 111 | 160 Updates/Second |

**Table 28. CONVERSION RATES**

| Bit # | Function |
|---|---|
| 7 | Reserved |
| <6:4> | Reserved |
| 3 | Reserved |
| <2:0> | Fan 1 Response |

### Look-up Table: Modes of Operation

Figure 40 and Figure 41 show what the look-up table looks like if all eight points are used on the one curve.

Figure 40 shows the transfer curve when the fan is programmed to run at discrete speeds. The ADM1033 spins the fan at its new speed once a threshold is crossed.

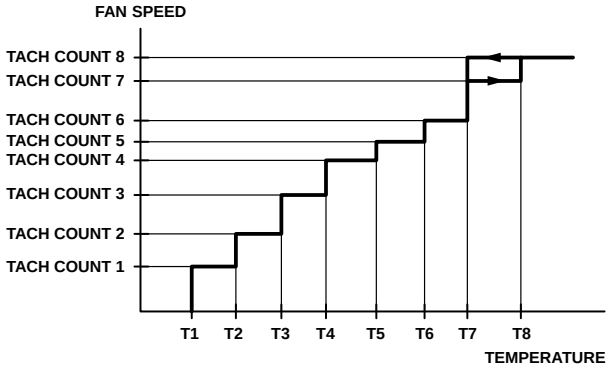



**Figure 40. Programming the Look-up Table in Discreet Fan Speeds Mode**

Figure 41 shows the transfer curve if the Linear Fan Speeds option is chosen. At temperature T1, the fan runs at Fan Speed 1. As the temperature increases, the fan speed increases until it reaches Fan Speed 2 at T2.

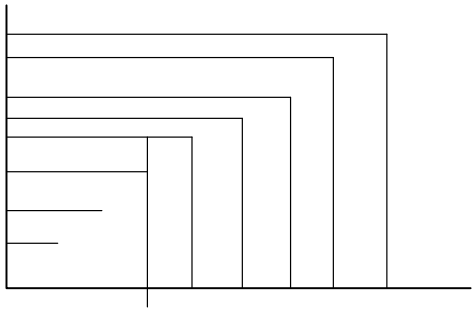


**Figure 41. Programming the Look-up Table in Linear Fan Speeds Mode**

The ADM1033 can be configured so that Fan 1 can be controlled by either the local temperature, or by the Remote 1 temperatures.

**Table 31. DRIVE BHVR BITS**

| Bits | DRIVE x BHVR |
|---|---|
| 00 | Local Temperature Controls Fan |
| 01 | Remote 1 Temperature Controls Fan |
| 10 | Reserved |
| 11 | Fan Runs at Full Speed |

### Look-up Table Hysteresis

The user can program a hysteresis to be applied to the look-up table. The advantage of this is apparent if the temperature is cycling around one of the threshold temperatures and causing the fan speed to switch between the two speeds, particularly when the look-up table is configured in discrete mode. It would not be as important in the linear mode.

**Table 32. PROGRAMMING THE HYSTERESIS**

| Code | Hysteresis Value |
|---|---|
| 0000 0000 | 0 C |
| 0000 0001 | 1 C |
| 0000 0010 | 2 C |
| 0000 0101 | 5 C |
| 0000 1000 | 8 C |
| 0000 1111 | 15 C |

The look-up table's hysteresis register is at Address 0x3A. A hysteresis value of between 0 C and 15 C can be programmed with a resolution of 1 C and applied to all the temperature thresholds. Table 32 gives examples of values for programming.

### Programming the $\overline{\text{THERM}}$ Limit for Temperature Channels

$\overline{\text{THERM}}$ is the absolute maximum temperature allowed on a temperature channel. Above this temperature, a component such as the CPU or VRM may be operating beyond its safe operating limit. When the temperature measured exceeds $\overline{\text{THERM}}$, all fans are driven at full speed to provide critical system cooling. The fans remain running at full speed until the temperature drops below $\overline{\text{THERM}}$ – Hysteresis. The hysteresis value is programmable; its default is 5 C. If the Boost Disable bit (Bit 1) is set in Configuration Register 2, the fan do not run to full speed.

The $\overline{\text{THERM}}$ limit is considered the maximum worst-case operating temperature of the system. Exceeding any $\overline{\text{THERM}}$ limit runs the fan at full speed, a condition with very negative acoustic effects. This limit should be set up as a fail-safe and not exceeded under normal system operating conditions. The $\overline{\text{THERM}}$ temperature limit registers are listed in Table 33.

**Table 33. $\overline{\text{THERM}}$ HYSTERESIS REGISTERS**

| Address | Description | Default |
|---|---|---|
| 0x0D | Local $\overline{\text{THERM}}$ Limit | 0x95 (85 C) |
| 0x10 | Remote 1 $\overline{\text{THERM}}$ Limit | 0x95 (85 C) |

The $\overline{\text{THERM}}$ hysteresis register is at Address 0x1A. A hysteresis value is programmed and applied to all two temperature channels; Local and Remote 1. A $\overline{\text{THERM}}$ hysteresis value of between 0 C and 15 C can be programmed with a resolution of 1 C. Table 33 gives some examples.

**Table 34. PROGRAMMING $\overline{\text{THERM}}$ HYSTERESIS**

| Code | Hysteresis Value |
|---|---|
| 0000 0000 | 0 C |
| 0000 0001 | 1 C |
| 0000 0010 | 2 C |
| 0000 0101 | 5 C = Default |
| 0000 1000 | 8 C |
| 0000 1111 | 15 C |

### XOR Tree Test Mode

The ADM1033 includes an XOR tree test mode. This is useful for in circuit test equipment at board level testing. By applying stimulus to the pins included in the XOR test, it is possible to detect opens or shorts on the system board. Figure 43 shows the signals that are exercised in the XOR tree test mode. The XOR tree test is enabled by setting the XOR bit (Bit 3) in Configuration 4 Register (0x04).

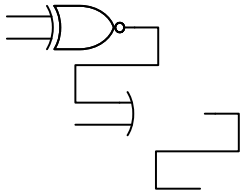


**Figure 43. XOR Tree Test**

**Table 35. ADM1033 REGISTERS**

| Address | R/W | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default | Lock |
|---|---|---|---|---|---|---|---|---|---|---|---|---|

**Table 35. ADM1033 REGISTERS**

| Address | R/W | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x3C/BC | R/W | Fan Response | RES | RES | RES | RES | RES | F1 | F1 | F1 | 0x01 | |
| 0x3D/BD | R | Device ID | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x34 | N |
| 0x3E/BE | R | Company ID | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x41 | N |
| 0x3F/BF | R | Revision Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x02 | N |
| 0x40/C0 | R | Local Temperature | 4 | 3 | 2 | 1 | 0 | RES | RES | RES | 0x00 | N |
| 0x41/C1 | R | Local Temperature | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 0x00 | N |
| 0x42/C2 | R | Remote 1 Temp | 4 | 3 | 2 | 1 | 0 | RES | RES | RES | 0x00 | N |
| 0x43/C3 | R | Remote 1 Temp | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 0x00 | N |
| 0x4A/CA | R | TACH1 Period | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0xFF | N |
| 0x4B/CB | R | TACH1 Period | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 0xFF | N |
| 0x4E/CE | R | $\overline{\text{THERM}}$ % Ontime | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x00 | N |
| | | | | | | | | RES | RES | RES | 0x00 | |

**Table 38. REGISTER 0X02, CONFIGURATION REGISTER 2, POWER-ON DEFAULT 0X84, LOCK = Y, S/W RESET = Y**

| Bit | Name | R/W | Description |
|---|---|---|---|
| 7 | Round Robin | R/W | |

**Table 41. REGISTER 0X05, CONFIGURATION RATE REGISTER, POWER-ON DEFAULT 0X07, LOCK = Y, S/W RESET = Y**

| Bit | Name | R/W | Description |
|---|---|---|---|
| 7 | Reserved | R | This bit is reserved for future use. Do not write to this bit. |
| <6:4> | Reserved | R | Reserved. |
| <3:0> | Conversion Rate | R/W | |

**Table 45. REGISTER 0X09, MASK REGISTER 2, POWER-ON DEFAULT 0X18, LOCK = N, S/W RESET = Y**

| Bit | Name | R/W | Description |
|---|---|---|---|
| <7:5> | Unused | R | Unused |
| 4 | $\overline{\text{THERM}}$ % | R/W | A 1 disables the corresponding interrupt status bit, preventing it from causing the interrupt output. The status bit is not affected. Default = 1. |
| 3 | $\overline{\text{THERM}}$ Assert | R/W | A 1 disables the corresponding interrupt status bit, preventing it from causing the interrupt output. The status bit is not affected. Default = 0. |
| 2 | $\overline{\text{THERM}}$_State | R/W | A 1 disables the corresponding interrupt status bit, preventing it from causing the interrupt output. The status bit is not affected. Default = 0. This bit has no effect in $\overline{\text{ALERT}}$ comparator mode, because the corresponding status bit does not generate an $\overline{\text{ALERT}}$ in that mode. |
| <1:0> | Unused | R | Unused |

**Table 46. REGISTER 0X0A, MASK REGISTER 3, POWER-ON DEFAULT 0X00, LOCK = N, S/W RESET = Y**

| Bit | Name | R/W | Description |
|---|---|---|---|
| 7 | | | |

**Table 52. REGISTER 0X10, REMOTE 1 $\overline{\text{THERM}}$ LIMIT, POWER-ON DEFAULT 0X95, LOCK = Y, S/W RESET = N**

| Bit | Name | R/W | Description |
|---|---|---|---|
| <7:0> | Remote 1 $\overline{\text{THERM}}$ Limit | R/W | When the Remote 1 temperature exceeds this temperature, the corresponding status bit is set and the $\overline{\text{THERM}}$ output is activated. |

**Table 53. REGISTER 0X16, LOCAL OFFSET REGISTER, POWER-ON DEFAULT 0X00, LOCK = Y, S/W RESET = N**

| Bit | Name | R/W | Description |
|---|---|---|---|
| <7:0> | Local Offset | | |

**Table 57. LOOK-UP TABLE REGISTERS, LOCK = Y, S/W RESET = Y**

| Register Address | R/W | Description | Power-On Default |
|---|---|---|---|
| 0x22 | R/W | Look-up Table, T1 | 0xFF |
| 0x23 | R/W | Look-up Table, T2 | 0xFF |
| 0x24 | R/W | Look-up Table, T3 | 0xFF |
| 0x25 | R/W | Look-up Table, T4 | 0xFF |
| 0x26 | R/W | Look-up Table, T5 | 0xFF |
| 0x27 | R/W | Look-up Table, T6 | 0xFF |
| 0x28 | R/W | Look-up Table, T7 | 0xFF |
| 0x29 | R/W | Look-up Table, T8 | 0xFF |
| 0x2A | R/W | Look-up Table, FS1, LSB | 0xFF |
| 0x2B | R/W | Look-up Table, FS1, MSB | 0xFF |
| 0x2C | R/W | Look-up Table, FS2, LSB | 0xFF |
| 0x2D | R/W | Look-up Table, FS2, MSB | 0xFF |
| 0x2E | R/W | Look-up Table, FS3, LSB | 0xFF |
| 0x2F | R/W | Look-up Table, FS3, MSB | 0xFF |
| 0x30 | R/W | Look-up Table, FS4, LSB | 0xFF |
| 0x31 | R/W | Look-up Table, FS4, MSB | 0xFF |
| 0x32 | R/W | Look-up Table, FS5, LSB | 0xFF |
| 0x33 | R/W | Look-up Table, FS5, MSB | 0xFF |
| 0x34 | R/W | Look-up Table, FS6, LSB | 0xFF |
| 0x35 | R/W | Look-up Table, FS6, MSB | 0xFF |
| 0x36 | R/W | Look-up Table, FS7, LSB | 0xFF |
| 0x37 | R/W | Look-up Table, FS7, MSB | 0xFF |
| 0x38 | R/W | Look-up Table, FS8, LSB | 0xFF |
| 0x39 | R/W | Look-up Table, FS8, MSB | 0xFF |

**Table 58. REGISTER 0X3A, LOOK-UP TABLE HYSTERESIS, POWER-ON DEFAULT 0X05, LOCK = Y, S/W RESET = Y**

| Bit | Name | R/W | Description |
|---|---|---|---|
| <7:4> | Reserved | R | Reserved |
| <3:0> | Look-up Table Hysteresis | R/W | These bits determine the hysteresis applied to the temperature thresholds in the Look-up table. LSB size = 1 |

**Table 61. REGISTER 0X3E, COMPANY ID, POWER-ON DEFAULT 0X41, LOCK = N, S/W RESET = N**

| Bit | Name | R/W | Description |
|---|---|---|---|
| <7:0> | Company ID | R | This read-only value contains the company ID, which is 0x41. |

**Table 62. REGISTER 0X3F, REVISION REGISTER, POWER-ON DEFAULT 0X02, LOCK = N, S/W RESET = N**

| Bit | Name | R/W | Description |
|---|---|---|---|
| <7:0> | Revision ID | R | This read-only value contains the revision ID. |

**Table 63. REGISTER 0X40/41, LOCAL TEMP REGISTERS, POWER-ON DEFAULT 0X00, LOCK = N, S/W RESET = Y**

| Bit | Name | R/W | Description |
|---|---|---|---|
| <4:0> | Local Temperature LSB | R | This register contains the LSBs of the last measured local temperature value. Resolution = 0.03125 C. |
| <12:5> | Local Temperature MSB | R | This register contains the MSBs of the last measured local temperature value. Resolution = 1 C. |

**Table 64. REGISTER 0X42/43, REMOTE 1 TEMP REGISTERS, POWER-ON DEFAULT 0X00, LOCK = N, S/W RESET = Y**

| Bit | Name | R/W | Description |
|---|---|---|---|
| <4:0> | Remote 1 Temperature LSB | R | This register contains the LSBs of the last measured Remote 1 temperature value. Resolution = 0.03125 C. |
| <12:5> | Remote 1 Temperature MSB | R | This register contains the LSBs of the last measured Remote 1 temperature value. Resolution = 1 C. |

**Table 65. REGISTER 0X4A/4B, TACH1 PERIOD, POWER-ON DEFAULT 0XFF, LOCK = N, S/W RESET = Y**

| Bit | Name | R/W | Description |
|---|---|---|---|
| <7:0> | Fan 1 Period Count, LSB | R | This register contains the LSBs of the last measured Fan 1 revolution count. |
| <15:8> | Fan 1 Period Count, MSB | R | This register contains the MSBs of the last measured Fan 1 revolution count. |

**Table 66. REGISTER 0X4E, $\overline{\text{THERM}}$ % ON-TIME, POWER-ON DEFAULT 0X00, LOCK = N, S/W RESET = Y**

| Bit | Name | R/W | Description |
|---|---|---|---|
| <7:0> | $\overline{\text{THERM}}$ % On-Time | R | Represents the % time of $\overline{\text{THERM}}$ activity within the time window set by the configuration bits. |

**Table 67. REGISTER 0X4F, STATUS 1, POWER-ON DEFAULT 0X00, LOCK = N, S/W RESET = Y**

| Bit | Name | R/W | Description |
|---|---|---|---|

7

**Table 68. REGISTER 0X50, STATUS 2, POWER-ON DEFAULT 0X00, LOCK = N, S/W RESET = Y**

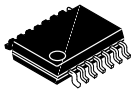
| Bit | Name | R/W | Description |
|---|---|---|---|
| 7 | Local $\overline{\text{THERM}}$ | R | A 1 indicates that the local $\overline{\text{THERM}}$ limit has been tripped. |
| 6 | Remote 1 $\overline{\text{THERM}}$ | R | A 1 indicates that the Remote 1 $\overline{\text{THERM}}$ limit has been tripped. |
| 4 | $\overline{\text{THERM}}$ % Exceeded | R | A 1 indicates that the $\overline{\text{THERM}}$ signal has been asserted for longer than the programmed limit. Clear on Read. If $\overline{\text{THERM}}$ % Limit = 0x00 and $\overline{\text{THERM}}$ is asserted, it is reasserted immediately. |
| 3 | $\overline{\text{THERM}}$ Asserted | R | A 1 indicates that the $\overline{\text{THERM}}$ signal has been asserted low as an input only. |
| 2 | $\overline{\text{THERM}}$_State | R | A 1 indicates that the $\overline{\text{THERM}}$ pin has been asserted low as an output. |
| 1 | Reserved | R | Reserved |
| 0 | Reserved | R | Reserved |

**Table 69. REGISTER 0X51, STATUS REGISTER 3, POWER-ON DEFAULT 0X00, LOCK = N, S/W RESET = Y**

| Bit | Name | R/W | Description |
|---|---|---|---|
| 7 | Fan 1 Stalled | R | A 1 indicates that Fan 1 has stalled. |
| 6 | Fan Alarm Speed | R | A 1 indicates that the fans are running at full speed due to an alarm condition, for instance, when a $\overline{\text{THERM}}$ temperature limit is exceeded. |
| 4 | Reserved | R | Reserved |
| 3 | Reserved | R | Reserved |
| 2 | Reserved | R | Reserved |
| 1 | Reserved | R | Reserved |
| 0 | $\overline{\text{ALERT}}$ Low | R | A 1 indicates that the ADM1033 has pulled the $\overline{\text{ALERT}}$ output pin low. This allows polling of a single status register to determine if an $\overline{\text{ALERT}}$ condition in any of the status registers has occurred. |

**Table 70. ORDERING INFORMATION**

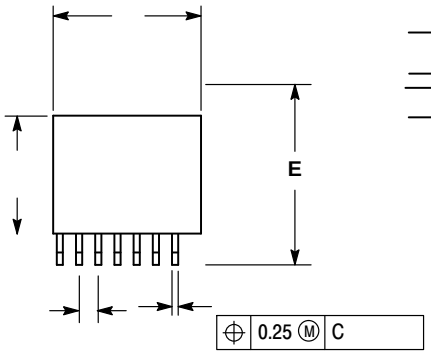
| Device Number* | Temperature Range | Package Type | Package Option | Shipping |
|---|---|---|---|---|

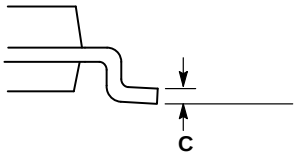


**SCALE 2:1**

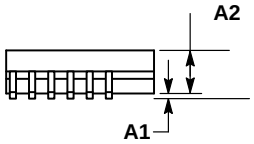
**QSOP16**
CASE 492−01
ISSUE A

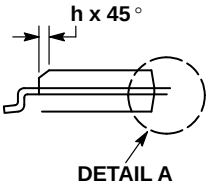
DATE 23 MAR 2011




**DETAIL A**




**DETAIL A**

NOTES:

| DIM | INCHES MIN | MA |
|---|---|---|
| A | 0.053 | 0.069 |
| A1 | 0.004 | 0.010 |
| | 0.008 | 0.012 |
| \ | 0.007 | 0.010 |
| | 0.025 BSC | |
| | 0.009 | 0.020 |
| L | 0.016 | 0.050 |
| M | 0 | 8 |