

Figure 1. Functional Block Diagram

ADM1034

Table 2. THERMAL CHARACTERISTICS

	Package Type	θ_{JA}	θ_{JC}	Unit
	16-lead QSOP Package	150	39	C/W

Table 3. PIN ASSIGNMENT

Pin No.

ADM1034

Table 4. ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX} , $V_{CC} = V_{MIN}$ to V_{MAX} , unless otherwise noted). (Note 1)

Parameter

ADM1034

Table 4. ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX} , $V_{CC} = V_{MIN}$ to V_{MAX} , unless otherwise noted). (Note 1)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
-----------	--------------------------	-----	-----	-----	------

TYPICAL PERFORMANCE CHARACTERISTICS

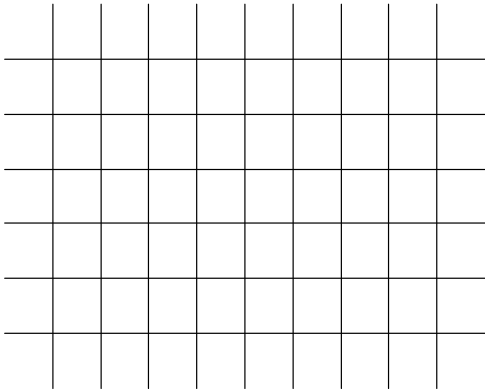


Figure 3. Temperature Error vs. PCB Track Resistance DXP to GND and V_{CC}

Figure 4. Remote Temperature Error vs. D+, D- Capacitance

Figure 5. Remote Temperature Error vs. Series Resistance on D+ and D-

Figure 6. Remote Temperature Error vs. Power Supply Noise Frequency

Figure 7. Remote Temperature Error vs. Common-Mode Noise Frequency Coupled on D+ and D-

Figure 8. Remote Temperature Error vs. Differential-Mode Noise Frequency Coupled on D+ and D-

ADM1034

ADM1034

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

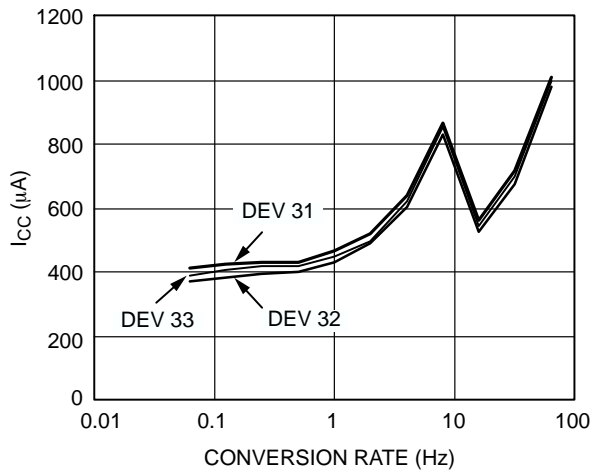


Figure 13. Supply Current vs. Conversion Rate

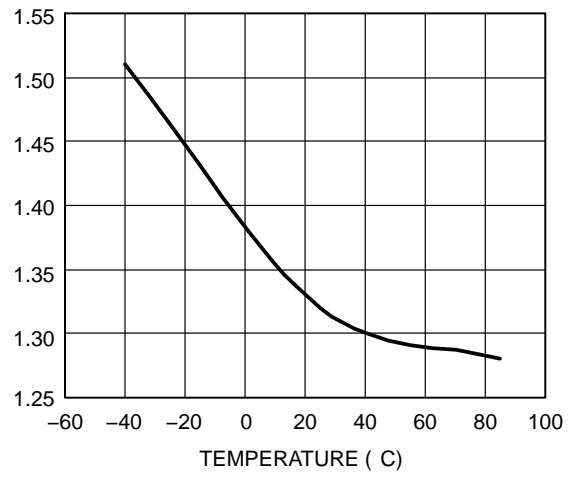


Figure 14. Supply Current vs. ADM1034 Temperature

ADM1034

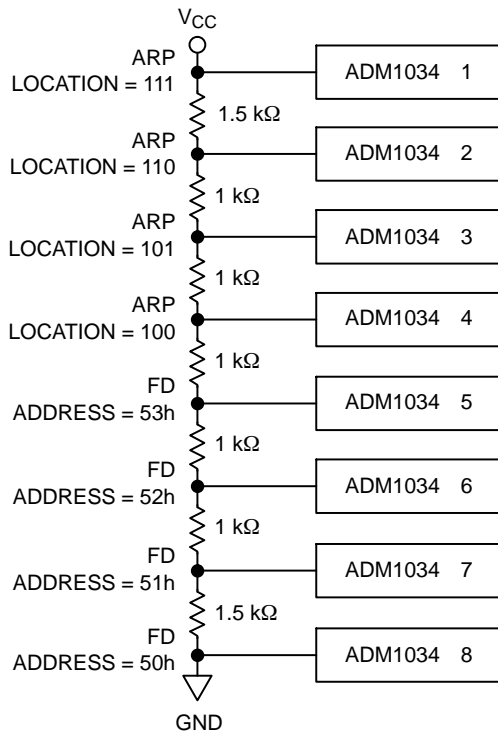


Figure 16. Setting Up Multiple ADM1034 Addresses in SMBus 2.0 ARP-capable Mode

In SMBus 2.0 mode, this vendor specific ID is generated by an on-chip random number generator. This should enable two adjacent ADM1034s in the same system to powerup with a different vendor specific ID, allowing the master to identify the two separate ADM1034's and assign a different address to each.

The state of the LOCATION input on powerup is also reflected in the UDID. This is useful when there is more than one ADM1034 in the system, so the master knows which one it is communicating with. The complete UDID is listed in Table 7.

The SMBus 2.0 master issues both general and directed ARP commands. A general command is directed at all ARP devices. A directed command is targeted at a single device once an address has been established. The PEC byte must be used for ARP commands. (Refer to the Packet Error Checking (PEC) section.)

The ADM1034 responds to the following commands:

- Prepare to ARP (General)
- Reset Device (General and Directed)
- Get UDID (General and Directed)
- Assign Address (General)

Table 5. INTERNAL REGISTER DESCRIPTIONS

Register	Description
Configuration	Provides control and configuration of various functions on the device.
Conversion Rate	Determines the number of measurements per second completed by the ADM1034.
Address Pointer	Contains the address that selects one of the other internal registers. When writing to the ADM1034, the first byte of data is always a register address, written to the address pointer register.
Status	Provides the status of each limit comparison.
Interrupt Mask	

ADM1034

Table 6. RESISTOR RATIOS FOR SETTING LOCATION BITS

Ideal Ratio $R2/(R1 + R2)$	R1 k Ω	R2 Ω	Actual $R2/(R1 + R2)$	Error %	SMBus Ver (Note 1)	SMBus Address	UDID LLL
N/A	0	O/C	1	0	ARP	N/A	111

ADM1034

clock pulse to assert a stop condition. In read mode, the master device overrides the acknowledge bit by pulling the data line high



Figure 22. Block Write to RAM

Temperature Measurement System

Internal Temperature Measurement

The ADM1034 contains an on-chip band gap temperature sensor. The on-chip ADC performs conversions on the sensor’s output, outputting the data in 13-bit format. The resolution of the local temperature sensor is 0.03125 C.

Table 8 shows the format of the temperature data MSBs. Table 9 shows the same for the LSBs. To ensure accurate readings, read the LSBs first. This locks the current LSBs and MSBs until the MSBs are read. They then start to update again. (Reading only the MSBs does not lock the registers.) Temperature updates to the look-up table take place in parallel; so fan speeds may be updated even if the MSBs are locked.

**Table 8. TEMPERATURE DATA FORMAT
(LOCAL TEMPERATURE AND REMOTE
TEMPERATURE HIGH BYTES)**

Temperature (°C)	Digital Output
-64 C	

ADM1034

To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles at conversion rates of less than or equal to 8 Hz. An external temperature measurement takes nominally 32 ms when averaging is enabled and 6 ms when averaging is disabled.

One LSB of the ADC corresponds to 0.03125 C. The ADM1034 can theoretically measure temperatures from 64 C to +191.96875 C, although these are outside its operating range. The extended temperature resolution data format is shown in Table 9. The data for the local and remote channels is stored in the extended temperature resolution registers (Reg. 0x40 = Local, Reg. 0x42 = Remote 1, and Reg. 0x44 = Remote 2).

Table 10. TEMPERATURE MEASUREMENT REGISTERS

Register	Description	Default
0x40	Local Temperature, LSBs	0x00
0x41	Local Temperature, MSBs	0x00
0x42	Remote 1 Temperature, LSBs	0x00
0x43	Remote 1 Temperature, MSBs	0x00
0x44	Remote 2 Temperature, LSBs	0x00
0x45	Remote 2 Temperature, MSBs	0x00

High and low temperature limit registers are associated with each temperature measurement channel. Exceeding the programmed high and low limits sets the appropriate status bit. Exceeding either limit can cause an SMBusALERT interrupt.

Table 11. TEMPERATURE MEASUREMENT LIMIT REGISTERS

Register	Description	Default
0x0B	Local High Limit	0x8B (75 C)
0x0C	Local Low Limit	0x54 (20 C)
0x0D	Local THERM Limit	0x95 (85 C)
0x0E	Remote 1 High Limit	0x8B (75 C)
0x0F	Remote 1 Low Limit	0x54 (20 C)
0x10	Remote 1 THERM Limit	0x95 (85 C)
0x11	Remote 2 High Limit	0x8B (75 C)
0x12	Remote 2 Low Limit	0x54 (20 C)
0x13	Remote 2 THERM Limit	0x95 (85 C)

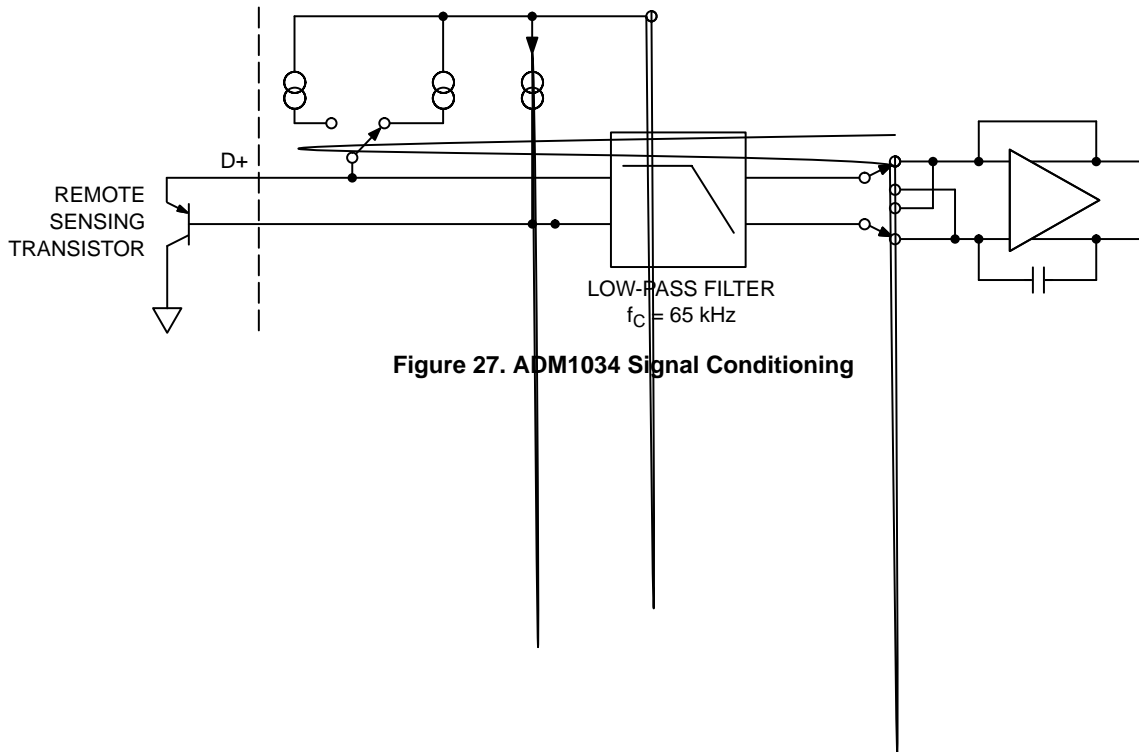


Figure 27. ADM1034 Signal Conditioning

Removing Temperature Errors

As CPUs run faster and faster, it gets more difficult to avoid high frequency clocks when routing the D+ and D- traces around a system board. Even when the recommended layout

temperature sensor and the part. The effect of any filter resistance seen in series with the remote sensor is automatically cancelled from the temperature.

The construction of a filter allows the ADM1034 and the remote temperature sensor to operate in noisy environments. Figure 29 shows a low-pass R C R filter with the following values: $R = 100 \Omega$ and $C = 1 \text{ nF}$. This filtering reduces both common-mode noise and differential noise.



Figure 29. Filter between Remote Sensor and ADM1034

temperature channel; L or more consecutive out-of-limits on the external 1 temperature channel; or L or more consecutive out-of-limits on the external 2 temperature channel. The fault queue is independent of the state of the bits in the ALERT status registers.

Table 23. FAULT QUEUE ADDRESS 0X06

Bits <3:0>	Fault Queue
000X	1
001X	2
01XX	3
1XXX	4

To reset the fault queue, do one of the following:

- SMBus ARA Command
- Read Status Register 1
- Power-On Reset

The SMBusALERT clears, even if the condition that caused the SMBusALERT remains. The SMBusALERT is reasserted if the fault queue fills up.

Conversion Rate Register

The ADM1034 makes up to 64 measurements per second. However, for the sake of reduced power consumption and better noise immunity, users may run the ADM1034 at a slower conversion rate. Better noise immunity results from the averaging that occurs at the slower conversion rates. Averaging does not occur at rates of 16, 32, or 64 conversions per second. Table 24 lists the available conversion rates. Note that the current round-robin loop must be finished for conversion rates changes to take effect.

Table 24. CONVERSION RATES

Code	Conversion Rate
0x00	0.0625
0x01	0.125
0x02	

$\overline{\text{ALERT}}$ is never generated. This is because 0xFF corresponds to the $\overline{\text{THERM}}$ input, which is asserted continuously.

Table 25. CONVERSION RATES

Code	$\overline{\text{THERM}}$ % On-Time Window
000	0.25 s
001	0.5 s
010	1 s
011	2 s
100	4 s
101	8 s
110	8 s
111	8 s

When $\overline{\text{THERM}}$ is configured as an input only, setting the Enable $\overline{\text{THERM}}$ Events bits in Configuration Register 4 allows Pin 7 to operate as an I/O.

The user can configure the $\overline{\text{THERM}}$ pin to be pulled low as an output whenever the local temperature exceeds the local $\overline{\text{THERM}}$ limit. To do this, set the Enable Local $\overline{\text{THERM}}$ events bit (Bit 0) of Configuration Register 4 (Address 0x04).

The user can also configure the $\overline{\text{THERM}}$ pin to be pulled low as an output whenever the Remote 1 temperature exceeds the Remote 1 $\overline{\text{THERM}}$ limit. Set the Enable Remote 1 $\overline{\text{THERM}}$ events bit (Bit 1) of Configuration Register 4 (Address 0x04).

The last option is to configure the $\overline{\text{THERM}}$ pin to be pulled low as an output whenever the Remote 2 temperature exceeds the Remote 2 $\overline{\text{THERM}}$ limit. Set the Enable Remote 2 $\overline{\text{THERM}}$ events bit (Bit 2) of Configuration Register 4 (Address 0x04).

$\overline{\text{THERM}}$ % Limit Register

The $\overline{\text{THERM}}$ % limit is programmed to Register 0x19. An $\overline{\text{ALERT}}$ is generated, if $\overline{\text{THERM}}$ is asserted for longer than the programmed percentage limit. The limit is programmed as a percentage of the chosen time window.

$\overline{\text{THERM}}$ % limit register is an 8-bit register.

0x00 = 0%

0xFF = 100%

Therefore, 1 LSB = 0.39%.

Example:

If a time window of 8 seconds is chosen, and an $\overline{\text{ALERT}}$ is to be generated if $\overline{\text{THERM}}$ is asserted for more than 1 second, program the following value to the limit register:

$$\% \text{ Limit} = 1/8 \cdot 100 = 12.5\%$$

$$12.5\% / 0.39\% = 32d = 0x20 = 0010\ 0000$$

An $\overline{\text{ALERT}}$ is generated if the $\overline{\text{THERM}}$ limit is exceeded after the time window has elapsed, assuming it is not masked.

Fan Drive Signal

The ADM1034 controls the speed of up to two cooling fans. Varying the duty cycle (on/off time) of a square wave applied to the fan varies the speed of the fan. The ADM1034 uses a control method called synchronous speed control, in which the PWM drive signal applied to the fan is synchronized with the fan's TACH signal. See the Synchronous Speed Control section for more information.

The external circuitry required to drive the fan is very simple. A single N-channel MOSFET is the only drive device required. The specifications of the MOSFET depend on the maximum current required by the fan and the gate voltage drive ($V_{GS} < 3.0\text{ V}$ for direct interfacing to the drive pin). V_{GS} can be greater than 3.0 V, as long as the pullup on the gate is tied to 5.0 V. The MOSFET should also have a low on-resistance to ensure that there is no significant voltage drop across the FET. A high on-resistance reduces the voltage applied across the fan and therefore the maximum operating speed of the fan. Figure 33 shows a scheme for driving a 3-wire fan.

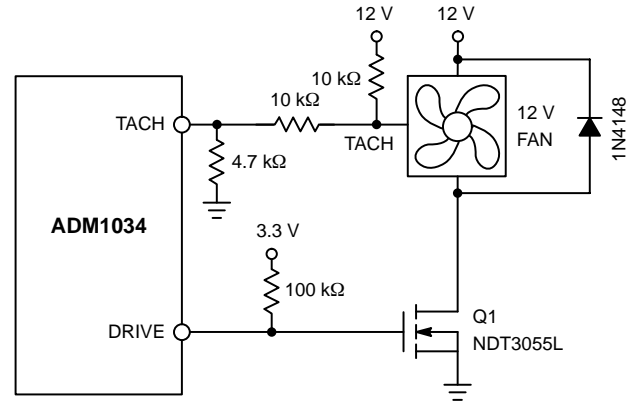


Figure 33. Interfacing a 3-wire Fan to the ADM1034 by Using an N-channel MOSFET

Figure 33 uses a 10 kΩ pullup resistor for the TACH signal. This assumes that the TACH signal is an open collector from the fan. In all cases, the fan's TACH signal must be kept below 5.0 V maximum to prevent damaging the ADM1034.

If in doubt as to whether a fan has an open-collector or totem pole TACH output, use one of the input signal conditioning circuits shown in the Fan Inputs section.

When designing drive circuits with transistors and FETs, make sure that the drive pins are not required to source current and that they sink less than the maximum current

GS

measurements are the main benefits. The fan is allowed to run reliably at speeds as low as 30 percent of the full capability.

The drive signal applied to the fan is synchronized with the TACH signal. The ADM1034 switches on the drive signal and waits for a transition on the TACH signal. When a transition takes place on the TACH signal, the PWM drive is switched off for a period of time called t_{OFF} . The drive signal is then switched on again. The toff time is varied in order to vary the fan speed. If the fan is running too fast, the toff time is increased. If the fan is running too slow, the toff time is decreased.

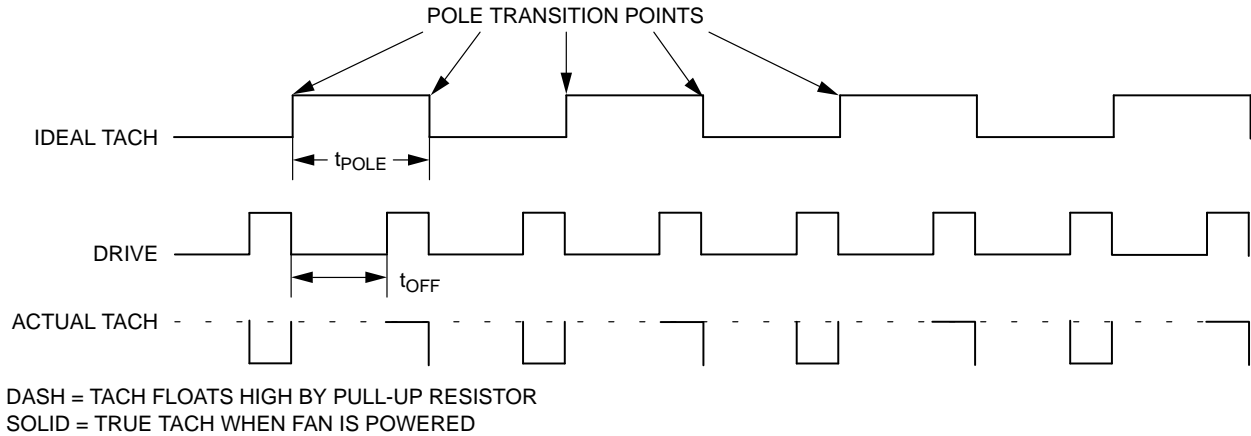


Figure 34. Drive Signal by Using Synchronous Control

Fan Inputs

Pin 2 and Pin 4 are TACH inputs intended for fan speed measurement. These inputs are open-drain.

Signal conditioning on the ADM1034 accommodates the slow rise and fall time of typical tachometer outputs. The maximum input signal range is from 0 V to 5.0 V, even when V_{CC} is less than 5.0 V. In the event that these inputs are supplied from fan outputs exceeding 0 V to 5.0 V, either resistive attenuation of the fan signal or diode clamping must be used to keep the fan inputs within an acceptable range.

Figure 35 to Figure 38 show examples of possible fan input circuits. If the fan TACH has a resistive pullup to V_{CC} , it can be connected directly to the fan output.

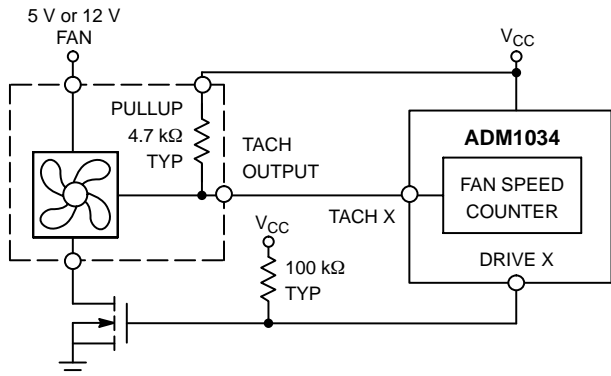


Figure 35. Fan with TACH Pullup to $+V_{CC}$

Since the drive signal is synchronized with the TACH signal, the frequency with which the fan is driven depends on the current speed of the fan and the number of poles in it.

Figure 34 shows how the synchronous speed drive signal works. The ideal TACH signal is the TACH signal that would be output from the fan if power were applied 100 percent of the time. It is representative of the actual speed of the fan. The actual TACH signal is the signal the user would see on the TACH output from the fan if the user were to put a scope on it. In effect, the actual TACH signal is the ideal TACH signal chopped with the drive signal.

If the fan output has a resistive pullup to 12 V (or another voltage greater than 5.0 V), the fan output can be clamped with a Zener diode, as shown in Figure 36. The Zener voltage should be chosen so that it is greater than V_{IH} but less than 5.0 V. Allowing for the voltage tolerance of the Zener, a value of between 3.0 V and 5.0 V is suitable.

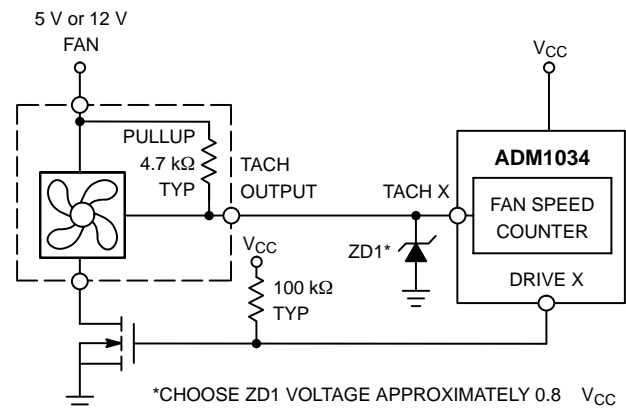


Figure 36. Fan with TACH Pullup to Voltage > 5.0 V, Clamped with Zener Diode

If the fan has a strong pullup (less than 1 kΩ to +12 V) or a totem-pole output, a series resistor can be added to limit the Zener current, as shown in Figure 37. Alternatively, a resistive attenuator may be used, as shown in Figure 38.

ADM1034

R1 and R2 should be chosen such that

$$2\text{ V} < V_{\text{PULLUP}} \times R2 / (R_{\text{PULLUP}} + R1 + R2) < 5\text{ V} \quad (\text{eq. 3})$$

The fan inputs have an input resistance of nominally 160 k Ω

$$\text{RPM} = (81920 - 60) / 6143$$

$$\text{Fan Speed} = 800 \text{ RPM}$$

Alarm Speed

The fan ALARM speed (Bit 6) in Status Register 3 (Address 0x51) is set whenever the fan runs at alarm speed. This occurs if the device is programmed to run the fan at full speed whenever the THERM

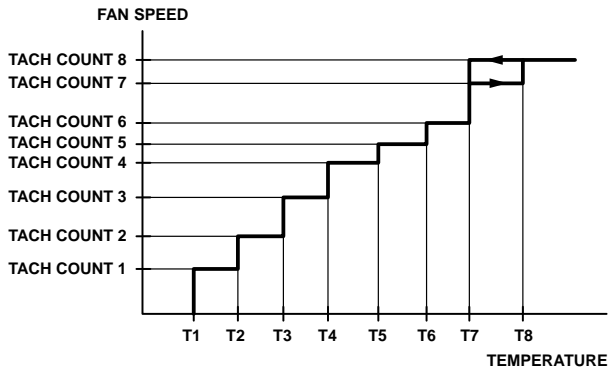


Figure 40. Programming the Look-up Table in Discret Fan Speeds Mode

Figure 41 shows the transfer curve if the Linear Fan Speeds option is chosen. At temperature T1, the fan runs at Fan Speed 1. As the temperature increases, the fan speed increases until it reaches Fan Speed 2 at T2.

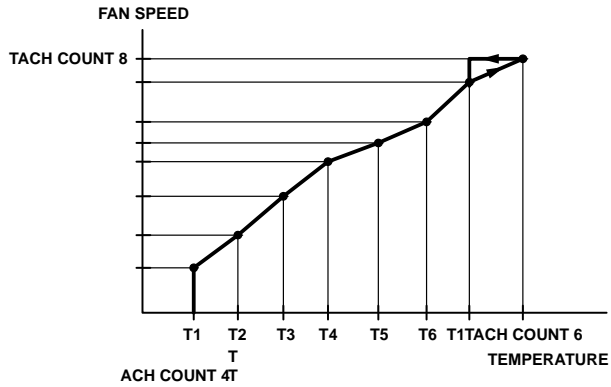


Figure 41. Programming the Look-up Table in Linear Fan Speeds Mode

The ADM1034 can be configured so that Fan 1 or Fan 2 can be controlled by either the local temperature, or by the Remote 1 or Remote 2 temperatures.

Table 31. DRIVE X BHVR BITS

Bits	DRIVE x BHVR
00	Local Temperature Controls Fan x
01	Remote 1 Temperature Controls Fan x
10	Remote 2 Temperature Controls Fan x
11	Fan x Runs at Full Speed

By default, Remote 1 controls Fan 1, and Remote 2 controls Fan 2. If the ADM1034 is in single-channel mode and one of the fans is set up to run from a temperature channel that is not being measured, the drive X BHVR bits are set to 11 and the fan is run at full speed.

Look-up Table Hysteresis

The user can program a hysteresis to be applied to the look-up table. The advantage of this is apparent if the temperature is cycling around one of the threshold temperatures and causing the fan speed to switch between the two speeds, particularly when the look-up table is configured in discrete mode. It would not be as important in the linear mode.

Programming the Look-up Table Hysteresis

The look-up table’s hysteresis register is at Address 0x3A. A hysteresis value of between 0 C and 15 C can be programmed with a resolution of 1 C and applied to all the temperature thresholds. Table 32 gives examples of values for programming.

Table 32. PROGRAMMING THE HYSTERESIS

Code	Hysteresis Value
0000 0000	0 C
0000 0001	1 C
0000 0010	2 C
0000 0101	5 C = Default
0000 1000	8 C
0000 1111	15 C

Programming the THERM Limit for Each Temperature Channel

THERM is the absolute maximum temperature allowed on a temperature channel. Above this temperature, a component such as the CPU or VRM may be operating beyond its safe operating limit. When the temperature measured exceeds THERM, all fans are driven at full speed to provide critical system cooling. The fans remain running at full speed until the temperature drops below THERM – Hysteresis. The hysteresis value is programmable; its default is 5 C. If the Boost Disable bit (Bit 1) is set in Configuration Register 2, the fans do not run to full speed.

The THERM limit is considered the maximum worst-case operating temperature of the system. Exceeding any THERM limit runs all fans at full speed, a condition with very negative acoustic effects. This limit should be set up as a fail-safe and not exceeded under normal system operating conditions.

The THERM temperature limit registers are listed in Table 33.

Table 33. THERM HYSTERESIS REGISTERS

Address	Register Name	Value
0x10	Remote 1 THERM Limit	0x95 (85 C)
0x13	Remote 2 THERM Limit	0x95 (85 C)

The THERM

Lock Bit

ADM1034

Table 36. REGISTER 0X00, # BYTES/BLOCK READ, POR = 0X20, LOCK = Y, S/W RESET = Y

Bit	Name	R/W	Description
<7:0>	# Bytes Block Read	R/W	Block reads are # bytes/block read long. The maximum is 32 bytes, the SMBus transaction limit.

Table 37. REGISTER 0X01, CONFIGURATION REGISTER 1, POWER-ON DEFAULT 0X01, LOCK = Y, S/W RESET = Y

Bit	Name	R/W	Description
7	Table/SW Con	R/W	Set this bit to 1 to place the fan speed under the control of the look-up table. When this bit is 0, the ADM1034 is in software/manual control mode. Default = 0.
6	Lock Bit	R/W	Set this bit to 1 to prevent the user from writing to the ADM1034 registers. 1 = ADM1034 registers locked. 0 = ADM1034 registers unlocked. Default = 0.
5	SDA Timeout	R/W	1 = SDA timeout enabled. 0 = SDA timeout disabled. Default = 0.
4	SCL Timeout	R/W	1 = SCL timeout enabled. 0 = SCL timeout disabled. Default = 0.
3	ALERT Configuration	R/W	0 = $\overline{\text{SMBusALERT}}$. Default = 0. 1 = $\overline{\text{ALERT_COMP}}$ mode.
2	Enable THERM Timer	R/W	1 = timer enabled, 0 = timer disabled. This bit enables THERM as an input. Default = 0.
1	Averaging Off	R/W	This bit is used to disable averaging at the slower conversion rates (8 Hz and slower). Averaging is automatically disabled at the higher (16[1]-28,slowe64.8JT*-.1055 Tw[Dc(R/W[ult)-277.361)-2

ADM1034

Table 40. REGISTER 0X04, CONFIGURATION REGISTER 4, POWER-ON DEFAULT 0X00, LOCK = Y, S/W RESET = Y

Bit	Name	R/W	Description
7	FAN_FAULT/REF	R/W	This bit sets the function for Pin 8. 0 = Default = FAN_FAULT output (THERM input is CMOS). 1 = Reference input for THERM.
<6:4>	THERM % Time Window	R/W	These bits set the time window over which THERM % is calculated. 000 = 0.25 second 001 = 0.5 second 010 = 1 second 011 = 2 seconds 100 = 4 seconds 101 = 8 seconds 110 = 8 seconds 111 = 8 seconds
3	XOR Test	R/W	Set this bit to 1 to enable the XOR connectivity test.
2	Enable Remote 2 THERM Events	R/W	This bit enables THERM

ADM1034

Table 43. REGISTER 0X07, FAN BEHAVIOR REGISTER, POWER-ON DEFAULT 0X09, LOCK = Y, S/W RESET = Y

Bit	Name	R/W	Description
7	Fan 2 Off	R/W	Set this bit to 1 to switch off Fan 2
6	Fan 1 Off	R/W	Set this bit to 1 to switch off Fan 1
5	Res	R	Reserved
4	Res	R	Reserved
<3:2>	DRIVE2 BHVR	R/W	These bits determine which temperature source controls the DRIVE2 output 00 = Local temperature controls DRIVE2 01 = Remote 1 temperature controls DRIVE2 10 = Remote 2 temperature controls DRIVE2 11 = DRIVE2 full speed
<1:0>	DRIVE1 BHVR	R/W	These bits determine which temperature source controls the DRIVE1 output 00 = Local temperature controls DRIVE1 01 = Remote 1 temperature controls DRIVE1 10 = Remote 2 temperature controls DRIVE1 11 = DRIVE1 full speed

Table 44. REGISTER 0X08, MASK REGISTER 1, POWER-ON DEFAULT 0X52, LOCK = N, S/W RESET = Y

Bit	Name	R/W	Description
7	Local High	R/W	A 1 disables the corresponding interrupt status bit from causing the interrupt output to be set. The status bit is not affected. Default = 0.
6	Local Low	R/W	A 1 disables the corresponding interrupt status bit from causing the interrupt output to be set. The status bit is not affected. Default = 1.
5	Remote 1 High	R/W	A 1 disables the corresponding interrupt status bit from causing the interrupt output to be set. The status bit is not affected. Default = 0.
4	Remote 1 Low	R/W	A 1 disables the corresponding interrupt status bit from causing the interrupt output to be set. The status bit is not affected. Default = 1.
3	Remote 1 Diode Error	R/W	A 1 disables the corresponding interrupt status bit from causing the interrupt output to be set. The status bit is not affected. Default = 0.
2	Remote 2 High	R/W	A 1 disables the corresponding interrupt status bit from causing the interrupt output to be set. The status bit is not affected. Default = 0.
1	Remote 2 Low	R/W	A 1 disables the corresponding interrupt status bit from causing the interrupt output to be set. The status bit is not affected. Default = 1.
0	Remote 2 Diode Error	R/W	A 1 disables the corresponding interrupt status bit from causing the interrupt output to be set. The status bit is not affected. Default = 0.

Table 45. REGISTER 0X09, MASK REGISTER 2, POWER-ON DEFAULT 0X18, LOCK = N, S/W RESET = Y

Bit	Name	R/W	Description
<7:5>	Unused	R	Unused
4	THERM %	R/W	A 1 disables the corresponding interrupt status bit, preventing it from causing the interrupt output. The status bit is not affected. Default = 1.
3	THERM Assert	R/W	A 1 disables the corresponding interrupt status bit, preventing it from causing the interrupt output. The status bit is not affected. Default = 0.
2	THERM_State	R/W	A 1 disables the corresponding interrupt status bit, preventing it from causing the interrupt output. The status bit is not affected. Default = 0. This bit has no effect in ALERT comparator mode, because the corresponding status bit does not generate an ALERT in that mode.
<1:0>	Unused	R	Unused

Table 46. REGISTER 0X0A, MASK REGISTER 3, POWER-ON DEFAULT 0X00, LOCK = N, S/W RESET = Y

Bit	Name	R/W	Description
7	Fan 1 Stalled	R/W	A 1 disables the corresponding interrupt status bit, preventing it from causing the interrupt output. The status bit is not affected. Default = 0.
6	Fan Alarm Speed	R/W	A 1 disables the corresponding interrupt status bit, preventing it from causing the interrupt output. The status bit is not affected. Default = 0.
5	Fan 2 Stalled	R/W	A 1 disables the corresponding interrupt status bit, preventing it from causing the interrupt output. The status bit is not affected. Default = 0.
4	Reserved	R	Reserved. Default = 0.
3	Reserved	R	Reserved. Default = 0.
2	Reserved	R	Reserved. Default = 0.
1	Reserved	R	Reserved. Default = 0.
0	Reserved	R	Reserved. Default = 0.

Table 47. REGISTER 0X0B, LOCAL HIGH LIMIT, POWER-ON DEFAULT 0X8B, LOCK = N, S/W RESET = N

Bit	Name	R/W	Description
<7:0>	Local High Limit	R/W	When the local temperature exceeds this temperature, the corresponding interrupt status bit is set.

Table 48. REGISTER 0X0C, LOCAL LOW LIMIT, POWER-ON DEFAULT 0X54, LOCK = N, S/W RESET = N

Bit	Name	R/W	Description
<7:0>	Local Low Limit	R/W	When the local temperature falls below this temperature, the corresponding interrupt status bit is set.

Table 49. REGISTER 0X0D, LOCAL THERM LIMIT, POWER-ON DEFAULT 0X95, LOCK = Y, S/W RESET = Y

Bit	Name	R/W	Description
<7:0>	Local THERM Limit	R/W	When the local temperature exceeds this temperature, the corresponding status bit is set and the THERM output is activated.

Table 50. REGISTER 0X0E, REMOTE 1 HIGH LIMIT, POWER-ON DEFAULT 0X8B, LOCK = N, S/W RESET = N

Bit	Name	R/W	Description
<7:0>	Remote 1 High Limit	R/W	When the Remote 1 temperature exceeds this temperature, the corresponding interrupt status bit is set.

Table 51. REGISTER 0X0F, REMOTE 1 LOW LIMIT, POWER-ON DEFAULT 0X54, LOCK = N, S/W RESET = N

Bit	Name	R/W	Description
<7:0>	Remote 1 Low Limit	R/W	When the Remote 1 temperature falls below this temperature, the corresponding interrupt status bit is set.

Table 52. REGISTER 0X10, REMOTE 1 THERM LIMIT, POWER-ON DEFAULT 0X95, LOCK = Y, S/W RESET = N

Bit	Name	R/W	Description
<7:0>	Remote 1 THERM Limit	R/W	When the Remote 1 temperature exceeds this temperature, the corresponding status bit is set and the THERM output is activated.

Table 53. REGISTER 0X11, REMOTE 2 HIGH LIMIT, POWER-ON DEFAULT 0X8B, LOCK = N, S/W RESET = N

Bit	Name	R/W	Description
<7:0>	Remote 2 High Limit	R/W	When the Remote 2 temperature exceeds this temperature, the corresponding interrupt status bit is set.

ADM1034

Table 54. REGISTER 0X12, REMOTE 2 LOW LIMIT, POWER-ON DEFAULT 0X54, LOCK = N, S/W RESET = N

Bit	Name	R/W	Description
<7:0>	Remote 2 Low Limit	R/W	When the Remote 2 temperature falls below this temperature, the corresponding interrupt status bit is set.

Table 55. REGISTER 0X13, REMOTE 2 THERM LIMIT, POWER-ON DEFAULT 0X95, LOCK = Y, S/W RESET = N

Bit	Name	R/W	Description
<7:0>	Remote 2 THERM Limit	R/W	When the Remote 2 temperature exceeds this temperature, the corresponding status bit is set and the THERM output is activated.

Table 56. REGISTER 0X16, LOCAL OFFSET REGISTER, POWER-ON DEFAULT 0X00, LOCK = Y, S/W RESET = N

Bit	Name	R/W	Description
<7:0>	Local Offset	R/W	Allows a twos compliment offset to be automatically added to or subtracted from the local temperature measurement. Resolution = 0.125 C. Maximum offset from -16 C to +15.875 C. Default = 0.

Table 57. REGISTER 0X17, REMOTE 1 OFFSET REGISTER, POWER-ON DEFAULT 0X00, LOCK = Y, S/W RESET = N

Bit	Name	R/W	Description
<7:0>	Remote 1 Offset	R/W	Allows a twos compliment offset to be automatically added to or subtracted from the Remote 1 temperature measurement. Resolution = 0.125 C. Maximum offset from -16 C to +15.875 C. Default = 0.

Table 58. REGISTER 0X18, REMOTE 2 OFFSET REGISTER, POWER-ON DEFAULT 0X00, LOCK = Y, S/W RESET = N

Bit	Name	R/W	Description
<7:0>	Remote 2 Offset	R/W	Allows a twos compliment offset to be automatically added to or subtracted from the Remote 2 temperature measurement. Resolution = 0.125 C. Maximum offset from -16 C to +15.875 C. Default = 0.

Table 59. REGISTER 0X19, THERM TIMER % LIMIT, POWER-ON DEFAULT 0XFF, LOCK = Y, S/W RESET = N

Bit	Name	R/W	Description
<7:0>	THERM Timer on% Limit	R/W	If the THERM is asserted for greater than this limit on the time window, the corresponding status bit is set.

Table 60. REGISTER 0X1A, THERM HYSTERESIS, POWER-ON DEFAULT 0X05, LOCK = Y, S/W RESET = N

Bit	Name	R/W	Description
<7:4>	Reserved	R	Reserved
<3:0>	THERM Hysteresis	R/W	An unsigned THERM hysteresis value, LSB = 1 C. Once THERM has been activated on a temperature channel, the THERM limit – hysteresis is deactivated if the temperature drops below THERM.

ADM1034

Table 61. LOOK-UP TABLE REGISTERS, LOCK = Y, S/W RESET = Y

Register Address	R/W	Description	Power-On Default
0x22	R/W	Look-up Table, T1	0xFF
0x23	R/W	Look-up Table, T2	0xFF
0x24	R/W	Look-up Table, T3	0xFF
0x25	R/W	Look-up Table, T4	0xFF
0x26	R/W	Look-up Table, T5	0xFF
0x27	R/W	Look-up Table, T6	0xFF
0x28	R/W	Look-up Table, T7	0xFF
0x29	R/W	Look-up Table, T8	0xFF
0x2A	R/W	Look-up Table, FS1, LSB	0xFF
0x2B	R/W	Look-up Table, FS1, MSB	0xFF
0x2C	R/W	Look-up Table, FS2, LSB	0xFF
0x2D	R/W	Look-up Table, FS2, MSB	0xFF
0x2E	R/W	Look-up Table, FS3, LSB	0xFF
0x2F	R/W	Look-up Table, FS3, MSB	0xFF
0x30	R/W	Look-up Table, FS4, LSB	0xFF
0x31	R/W	Look-up Table, FS4, MSB	0xFF
0x32	R/W	Look-up Table, FS5, LSB	0xFF
0x33	R/W	Look-up Table, FS5, MSB	0xFF
0x34	R/W	Look-up Table, FS6, LSB	0xFF
0x35	R/W	Look-up Table, FS6, MSB	0xFF
0x36	R/W	Look-up Table, FS7, LSB	0xFF
0x37	R/W	Look-up Table, FS7, MSB	0xFF
0x38	R/W	Look-up Table, FS8, LSB	0xFF
0x39	R/W	Look-up Table, FS8, MSB	0xFF

Table 62. REGISTER 0X3A, LOOK-UP TABLE HYSTERESIS, POWER-ON DEFAULT 0X05, LOCK = Y, S/W RESET = Y

Bit	Name	R/W	Description
<7:4>	Reserved	R	Reserved
<3:0>	Look-up Table Hysteresis	R/W	These bits determine the hysteresis applied to the temperature thresholds in the

ADM1034

Table 63. REGISTER 0X3C, FAN RESPONSE REGISTER, POWER-ON DEFAULT 0X11, LOCK = Y, S/W RESET = Y

Bit	Name	R/W	Description
7	Res	R	Reserved
<6:4>	Fan 2 Response	R/W	These bits set the fan's response in the fan speed control mode. 000 = 1.25 updates/second 001 = 2.5 updates/second = Default 010 = 5 updates/second 011 = 10 updates/second 100 = 20 updates/second 101 = 40 updates/second 110 = 80 updates/second 111 = 160 updates/second
3	Res	R	Reserved
<2:0>	Fan 1 Response	R/W	These bits set the fan's response in the fan speed control mode. 000 = 1.25 updates/second 001 = 2.5 updates/second = Default 010 = 5 updates/second 011 = 10 updates/second 100 = 20 updates/second 101 = 40 updates/second 110 = 80 updates/second 111 = 160 updates/second

Table 64. REGISTER 0X3D, DEVICE ID, POWER-ON DEFAULT 0X34, LOCK = N, S/W RESET = N

Bit	Name	R/W	Description
<7:0>	Device ID	R	This read-only value contains the device ID, which is 0x34.

Table 65. REGISTER 0X3E, COMPANY ID, POWER-ON DEFAULT 0X41, LOCK = N, S/W RESET = N

Bit	Name	R/W	Description
<7:0>	Company ID	R	This read-only value contains the company ID, which is 0x41.

Table 66. REGISTER 0X3F, REVISION REGISTER, POWER-ON DEFAULT 0X02, LOCK = N, S/W RESET = N

Bit	Name	R/W	Description
<7:0>	Revision ID	R	This read-only value contains the revision ID.

Table 67. REGISTER 0X40/41, LOCAL TEMP REGISTERS, POWER-ON DEFAULT 0X00, LOCK = N, S/W RESET = Y

Bit	Name	R/W	Description
<4:0>	Local Temperature LSB	R	This register contains the LSBs of the last measured local temperature value. Resolution = 0.03125 C.
<12:5>	Local Temperature MSB	R	This register contains the MSBs of the last measured local temperature value. Resolution = 1 C.

Table 68. REGISTER 0X42/43, REMOTE 1 TEMP REGISTERS, POWER-ON DEFAULT 0X00, LOCK = N, S/W RESET = Y

Bit	Name	R/W	Description
<4:0>	Remote 1 Temperature LSB	R	This register contains the LSBs of the last measured Remote 1 temperature value. Resolution = 0.03125 C.
<12:5>	Remote 1 Temperature MSB	R	This register contains the MSBs of the last measured Remote 1 temperature value. Resolution = 1 C.

Table 69. REGISTER 0X44/45, REMOTE 2 TEMP REGISTERS, POWER-ON DEFAULT 0X00, LOCK = N, S/W RESET = Y

Bit	Name	R/W	Description
<4:0>	Remote 2 Temperature LSB	R	This register contains the LSBs of the last measured Remote 2 temperature value. Resolution = 0.03125 C.
<12:5>	Remote 2 Temperature MSB	R	This register contains the MSBs of the last measured Remote 2 temperature value. Resolution = 1 C.

ADM1034

Table 70. REGISTER 0X4A/4B, TACH1 PERIOD, POWER-ON DEFAULT 0XFF, LOCK = N, S/W RESET = Y

Bit	Name	R/W	Description
<7:0>	Fan 1 Period Count, LSB	R	This register contains the LSBs of the last measured Fan 1 revolution count.
<15:8>	Fan 1 Period Count, MSB		

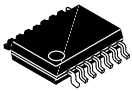
ADM1034

Table 75. REGISTER 0X51, STATUS REGISTER 3, POWER-ON DEFAULT 0X00, LOCK = N, S/W RESET = Y

Bit	Name	R/W	Description
7	Fan 1 Stalled	R	A 1 indicates that Fan 1 has stalled.
6	Fan Alarm Speed	R	A 1 indicates that the fans are running at full speed due to an alarm condition, for instance, when a THERM temperature limit is exceeded.
5	Fan 2 Stalled	R	A 1 indicates that Fan 2 has stalled.
4	Reserved	R	Reserved
3	Reserved	R	Reserved
2	Reserved	R	Reserved
1	Reserved	R	Reserved
0	ALERT Low	R	A 1 indicates that the ADM1034 has pulled the $\overline{\text{ALERT}}$ output pin low. This allows polling of a single status register to determine if an $\overline{\text{ALERT}}$ condition in any of the status registers has occurred.

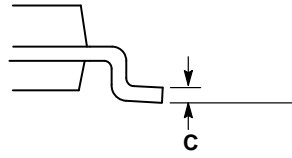
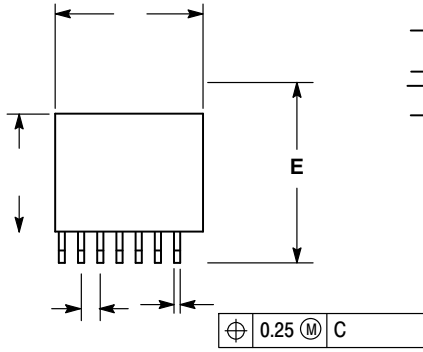
Table 76. ORDERING INFORMATION

Device Number*	Temperature Range	Package Type	Package Option	Shipping†
ADM1034ARQZ REEL	-40 C to +125 C	16-lead QSOP	RQ-16	2,500 Tape & Reel

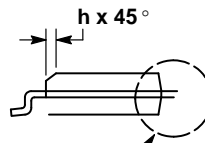
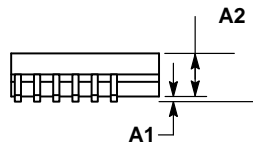


SCALE 2:1

QSOP16



DETAIL A



DETAIL A

NOTES:

INCHES		
DIM	MIN	MA
A	0.053	0.069
A1	0.004	0.010
	0.008	0.012
	0.007	0.010

0.025 BSC		
DIM	MIN	MA
L	0.009	0.020
M	0	8

onsemi, **onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi**
