

### ADP



						_
۱	•	en ιen	. n			n۱
PWM INPUT						
Input Voltage High <sup>2</sup>			2.0			V
Input Voltage Low <sup>2</sup>					0.8	V
Input Current <sup>2</sup>			-1		+1	μA
Hysteresis <sup>2</sup>			90	250		mV
DD INPUT						
Input Voltage High <sup>2</sup>			2.0			V
Input Voltage Low <sup>2</sup>					0.8	V
Input Current <sup>2</sup>			-1		+1	μA
Hysteresis <sup>2</sup>			<b>90</b>	250		mV
Propagation Delay Times <sup>3</sup>	tpdl <sub>op</sub>	See Figure 3		20	35	ns
helder a the second second	tpdh <sub>op</sub>	See Figure 3	85 ×	40	55	ns
HGH-SIDE DRIVER						
Output Resistance, Sourcing Current		BST to SW = 12 V	1 Contraction	3.8	4.4	
Output			1		1.8	
Output						k
Transit					55	ns
					45	ns
Propag					65	ns
					35	ns
SW Pul						k
.OW-SIDI						
Output					4.0	
Output					1.8	
Output						k
Transit					50	ns
					30	ns
Propag					35	ns
					40	ns
Time-o						ns
						ns
UPPLY						1
Supply					13.2	V
Supply					5	mA
UVLO					3.0	V

# ADP

## AB OL E MAXIM M RA ING

ab e

ab e		rsss‱ando os ∜s n rA⊠dso≀ Maria, Marings
٢	١n	yaayıcaals pryaanın Maryaayoo ic Trisis Marsıs s
VCC	–0.3 V to +15 V	n 🖬 ing on ly nc ion 🖬 op n 🖬 ion o ic 🖬 s or 🖬 hy
BST	–0.3 V to VCC + 15 V	o r con i i i ons 🖾 o os in i c🖬 in op maion 🕅
BST to SW	–0.3 V to +15 V	sciono isspeiieMaionisno i pi Epposr o Mandsot
SW		
DC	–5 V to +15 V	ic rikowsii y nisso rwis spoii Mano rokogs
<200 ns	–10 V to +25 V	Marrrnc o D
DRVH		
DC	SW – 0.3 V to BST + 0.3 V	
<200 ns	SW – 2 V to BST + 0.3 V	
DRVL		
DC	-0.3 V to VCC + 0.3 V	
<200 ns	-2 V to VCC + 0.3 V	A Start
IN, OD		
JA, SOIC N		
2-Layer Board	123°C/W	
4-Layer Board	90°C/W	
Operating Ambient Temperature		
Range	0°C to 0E°C	
Junction T		
Storage Te		
Lead Temp		
Solderin		
Vapor P		
Infrared		
А		
ESD (elect		
the humar		WARNING!
proprietar		
electrostat		ESD SENSITIVE DEVIC
degradatio		

# PIN CONFIG RA ION AND F NC ION DE CRIP ION



#### ab e P n Funct on Descr pt ons

n ●_	. n ●n	ι en
1	BST -	Upper MOSFET Floating Bootstrap Supply. A capacitor connected between the BST and SW pins holds this
		bootstrapped voltage for the high-side MOSFET as it is switched.
2	IN MARCEN	Logic Level PWM Input. This pin has primary control of the driver outputs. In normal operation, pulling this pin
		low turns on the low-side driver; pulling it high turns on the high-side driver:
3	OD	

## IMING CHARAC ERI IC



### **APPLICA ION INFORMA ION**

ΑΑ

or spplyinp BCC o AD Marcali Bayp Mass c Map Macion is r co nois Man ospply so o p Macrin s Mawn s Marcali bow E c Map Macion i May r c r Marcali c c i p MacC c Map Macions pro i Marcali c c Map Macion o bow E Man s Marsi p c r Marcali c c Map Macion Kascos Masposi Marcali o AD

### **B**, **A**

**Q**<sub>GATE</sub>

 $\mathbf{C}_{\mathbf{BST}} + \mathbf{C}_{\mathbf{BST}} = \mathbf{X}$ 

\_⊠alisi, sppty o≀&ag T ⊠a n&ag orw&ar crrn c&an&a si ga &bay

 $\mathbf{I}_{\mathbf{F} \mathbf{AVG}} = \mathbf{Q}_{\mathbf{GATE}} \times \mathbf{f}_{\mathbf{MAX}}$ 

w r **f**<sub>MAX</sub>







# **O** LINE DIMEN ION

