MAXIMUM RATINGS

Rating	Value	Unit
		°
		°
− − − θ − − θ − − − θ − − θ		° ° ° °
	−	°
−		°

ELECTRICAL CHARACTERISTICS

° ° ° °

Characteristic	Symbol	Condition	Min

APPLICATIONS INFORMATION

Theory of Operation

The ADP3110A are single phase MOSFET drivers designed for driving two N−channel MOSFETs in a synchronous buck converter topology. The ADP3110A will operate from 5.0 V or 12 V, but have been optimized for high current multi−phase buck regulators that convert 12 V rail directly to the core voltage required by complex logic chips. A single PWM input signal is all that is required to properly drive the high−side and the low−side MOSFETs. Each driver is capable of driving a 3 nF load at frequencies up to 1 MHz.

Low−Side Driver

The low−side driver is designed to drive a ground−referenced low $R_{DS(on)}$ N−Channel MOSFET. The voltage rail for the low−side driver is internally connected to the V_{CC} supply and PGND.

High−Side Driver

The high−side driver is designed to drive a floating low $R_{DS(on)}$ N−channel MOSFET. The gate voltage for the high side driver is developed by a bootstrap circuit referenced to Switch Node (SW) pin.

The bootstrap circuit is comprised of an external diode, and an external bootstrap capacitor. When the ADP3110A are starting up, the SW pin is at ground, so the bootstrap capacitor will charge up to V_{CC} through the bootstrap diode See Figure 4. When the PWM input goes high, the high−side driver will begin to turn on the high−side MOSFET using the stored charge of the bootstrap capacitor. As the high−side MOSFET turns on, the SW pin will rise. When the high−side MOSFET is fully on, the switch node will be at 12 V, and the BST pin will be at 12 V plus the charge of the bootstrap capacitor (approaching 24 V).

The bootstrap capacitor is recharged when the switch node goes low during the next cycle.

Safety Timer and Overlap Protection Circuit

It is very important that MOSFETs in a synchronous buck regulator do not both conduct at the same time. Excessive shoot−through or cross conduction can damage the MOSFETs, and even a small amount of cross conduction will cause a decrease in the power conversion efficiency.

The ADP3110A prevent cross conduction by monitoring the status of the external mosfets and applying the appropriate amount of “dead−time” or the time between the turn off of one MOSFET and the turn on of the other MOSFET.

When the PWM input pin goes high, DRVL will go low after a propagation delay (tpdlDRVL). The time it takes for the low−side MOSFET to turn off (tfDRVL) is dependent on the total charge on the low−side MOSFET gate. The ADP3110A monitor the gate voltage of both MOSFETs and the switchnode voltage to determine the conduction status of the MOSFETs. Once the low−side MOSFET is turned off an internal timer will delay (tpdhDRVH) the turn on of the high−side MOSFET

Likewise, when the PWM input pin goes low, DRVH will go low after the propagation delay (tpdDRVH). The time to turn off the high−side MOSFET (tfDRVH) is dependent on the total gate charge of the high−side MOSFET. A timer will be triggered once the high−side mosfet has stopped conducting, to delay (tpdhDRVL) the turn on of the low−side MOSFET

Power Supply Decoupling

The ADP3110A can source and sink relatively large currents to the gate pins of the external MOSFETs. In order to maintain a constant and stable supply voltage (V_{CC}) a low ESR capacitor should be placed near the power and ground pins. A 1 μF to 4.7 μF multi layer ceramic capacitor (MLCC) is usually sufficient.

Input Pins

The PWM input and the Output Disable pins of the ADP3110A have internal protection for Electro Static Discharge (ESD), but in normal operation they present a relatively high input impedance. If the PWM controller does not have internal pulldown resistors, they should be added externally to ensure that the driver outputs do not go high before the controller has reached its under voltage lockout threshold. The NCP5381 controller does include a passive internal pull−down resistor on the drive−on output pin.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BST}) and the internal (or an external) diode. Selection of these components can be done after the high−side MOSFET has been chosen. The bootstrap capacitor must have a voltage rating that is able to withstand twice the maximum supply voltage. A minimum 50 V rating is recommended. The capacitance is determined using the following equation:

$$= \frac{\quad}{\Delta}$$

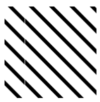
where Q_{GATE} is the total gate charge of the high−side MOSFET, and ΔV_{BST} is the voltage droop allowed on the high−side MOSFET drive. For example, a NTD60N03 has a total gate charge of about 30 nC. For an allowed droop of 300 mV, the required bootstrap capacitance is 100 nF. A good quality ceramic capacitor should be used.

The bootstrap diode must be rated to withstand the maximum supply voltage plus any peak ringing voltages that may be present on SW. The average forward current can be estimated by:

$$= \quad \times$$

where f_{MAX} is the maximum switching frequency of the controller. The peak surge current rating should be checked in−circuit, since this is dependent on the source impedance of the 12 V supply and the ESR of C_{BST}.

DFN8 3x3, 0.5P
CASE 506BJ
ISSUE O



SOIC 8 NB
CASE 751–07
ISSUE AK

DATE 16 FEB 2011