Publication Order Number:
February, 2010 − Rev. 1

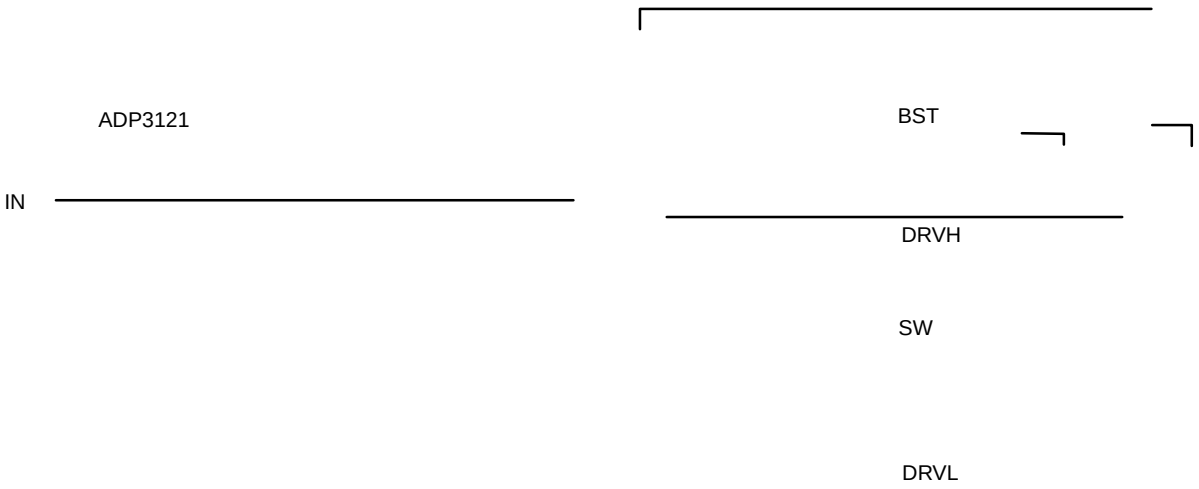

Figure 1. Block Diagram

MAXIMUM RATINGS

Rating	Value	Unit
θ_{JA}, SOIC_N 2−Layer Board 4−Layer Board	 123 90	°C/W
θ_{JA}, LFCSP_VD (Note 1) 4−Layer Board	 64.3	°C/W
Operating Ambient Temperature Range	0 to 85	°C
Junction Temperature Range	0 to 150	°C
Storage Temperature Range	−65 to +150	°C
Lead Temperature Soldering (10 sec) Vapor Phase (60 sec) Infrared (15 sec)	 300 215 260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Internally limited by thermal shutdown, 150°C min. 2−layer board, 1 in^2 Cu, 1 oz thickness. 60−180 seconds minimum above 237°C.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Pin Symbol	Pin Name	V_{max}	V_{min}
V_{CC}	Main supply voltage input	15 V	−0.3 V
GND	Ground	0 V	0 V
BST	Bootstrap Supply Voltage Input DC <200 ns BST to SW	 V_{CC} + 15 +35 +15	−0.3 V
SW	Switching Node (Bootstrap Supply Return) DC <200 ns	 +15 +25 V	 −5 V −10 V
DRVH	High−Side Driver Output DC <20 ns <200 ns	 BST + 0.3 V BST + 2.0 V BST + 0.3 V	 SW − 0.3 V SW − 2.0 V SW − 2.0 V
DRVL	Low−Side Driver Output DC <20 ns <200 ns	 V_{CC} + 0.3 V V_{CC} + 2.0 V V_{CC} + 0.3 V	 −0.3 V −2.0 V −2.0 V
IN	DRVH and DRVL Control Input	6.5 V	−0.3 V
$\overline{OD}$	Outside Disable	6.5 V	−0.3 V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. All voltages are with respect to PGND except where noted.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, BST = 4.0 V to 26 V, T_A = 0°C to 85°C, unless otherwise noted) (Note 1)

Characteristic

Theory of Operation

The ADP3121 is optimized for driving two N−channel MOSFETs in a synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high side and the low−side MOSFETs. Each driver is capable of driving a 3 nF load at speeds up to 500 kHz. A functional block diagram of ADP3121 is shown in Figure 1.

Low−Side Driver

The low−side driver is designed to drive a ground referenced N−channel MOSFET. The bias to the low−side driver is internally connected to the V_{CC} supply and PGND.

When the driver is enabled, the driver output is 180° out of phase with the PWM input. When the ADP3121 is disabled, the low−side gate is held low.

High−Side Driver

The high−side driver is designed to drive a floating N−channel MOSFET. The bias voltage for the high−side driver is developed by an external bootstrap supply circuit that is connected between the BST and SW pins.

The bootstrap circuit comprises Diode D1 and Bootstrap Capacitor C_{BST1}. C_{BST2} and R_{BST} are included to reduce the high−side gate drive voltage and to limit the switch node slew rate (called a Boot−

Re−arranging Equation 1 and Equation 2 to solve for C_{BST1} yields:

$$C_{BST1} = 10 \times \frac{Q_{GATE}}{V_{CC} - V_D}$$

C_{BST2} can then be found by rearranging Equation 1.

$$C_{BST2} = 10 \times \frac{Q_{GATE}}{V_{GATE}} - C_{BST1}$$

For example, an NTD60N02 has a total gate charge of about 12 nC at V_{GATE} = 7.0 V. Using V_{CC} = 12 V and V_D = 0.1 V, then C_{BST1} = 12 nF and C_{BST2} = 6.8 nF. Good quality ceramic capacitors should be used.

R_{BST} is used to limit slew rate and minimize ringing at the switch node. It also provides peak current limiting through D1. An R_{BST} value of 1.5 Ω to 2.2 Ω is a good choice. The resistor needs to handle at least 250 mΩ due to the peak currents that flow through it.

A small signal diode can be used for the bootstrap diode due to the ample gate drive voltage supplied by V_{CC}. The bootstrap diode must have a minimum 15 V rating to withstand the maximum supply voltage. The average forward current can be estimated by:

$$I_{F(AVG)} = Q_{GATE} \times f_{MAX} \quad \text{(eq. 3)}$$

where f_{MAX} is the maximum switching frequency of the controller.

The peak surge current rating should be calculated by:

$$I_{F(PEAK)} = \frac{V_{CC} - V_D}{R_{BST}} \quad \text{(eq. 4)}$$

MOSFET Selection

When interfacing the ADP3121 to external MOSFETs, the designer should consider ways to make a robust design that minimizes stresses on both the driver and the MOSFETs. These stresses include exceeding the short time duration voltage ratings on the driver pins as well as the external MOSFET.

It is also highly recommended to use the Boot−Snap circuit to improve the interaction of the driver with the

Another consideration is the nonoverlap circuitry of the ADP3121 that attempts to minimize the nonoverlap period. During the state of the high−side turning off to low−side turning on, the SW pin is monitored (as well as the conditions of SW prior to switching) to adequately prevent overlap.

However, during the low−side turn−off to high−side turn−on, the SW pin does not contain information for determining the proper switching time, so the state of the DRVL pin is monitored to go below one sixth of V_{CC}; then, a delay is added. Due to the Miller capacitance and internal delays of the low−side MOSFET gate, ensure that the Miller−to−input capacitance ratio is low enough, and that the low−side MOSFET internal delays are not so large as to allow accidental turn−on of the low−side when the high−side turns on. Contact ON Semiconductor for an updated list of recommended low−side MOSFETs.

PC Board Layout Considerations

Use these general guidelines when designing printed circuit boards:

- Trace out the high current paths and use short, wide (>20 mil) traces to make these connections.
- Minimize trace inductance between DRVH and DRVL outputs and MOSFET gates.
- Connect the PGND pin of the ADP3121 as closely as

PACKAGE DIMENSIONS

SOIC−

PACKAGE DIMENSIONS

LFCSP8 3x3, 0.5P
CASE 932AF−01
ISSUE O