8-Bit, Programmable, 2- to 3-Phase, Synchronous Buck Controller

ADP3193A

FEATURES

- **Selectable 2- or 3-phase operation at up to 1 MHz per phase**
- **±7.7 mV worst-case differential sensing error over temperature**
- **Logic-level PWM outputs for interface to external high power drivers**
- **Fast enhanced PWM (FEPWM) flex mode for excellent load transient performance**
- **Active current balancing between all output phases**
- **Built-in power-good/crowbar blanking supports on-the-fly VID code changes**
- **Digitally programmable 0.5 V to 1.6 V output supports both VR10.x and VR11 specifications**
- **Programmable short-circuit protection with programmable latch-off delay**

APPLICATIONS

- **Desktop PC power supplies for**
  - **Next generation Intel® processors**
  - **VRM modules**

GENERAL DESCRIPTION

The ADP3193A[1] is a highly efficient, multiphase, synchronous buck switching regulator controller optimized for converting a 12 V main supply into the core supply voltage required by high performance Intel processors. It uses an internal 8-bit DAC to read a voltage identification (VID) code directly from the processor, which is used to set the output voltage between 0.5 V and 1.6 V.

This device uses a multimode PWM architecture to drive the logic-level outputs at a programmable switching frequency that can be optimized for VR size and efficiency. The phase relationship of the output signals can be programmed to provide 2- or 3-phase operation, allowing for the construction of up to three complementary buck switching stages.

The ADP3193A also includes programmable no load offset and slope functions to adjust the output voltage as a function of the load current, optimally positioning it for a system transient. The ADP3193A also provides accurate and reliable short-circuit protection, adjustable current limiting, and delayed power-good output that accommodates on-the-fly output voltage changes requested by the CPU.

FUNCTIONAL BLOCK DIAGRAM

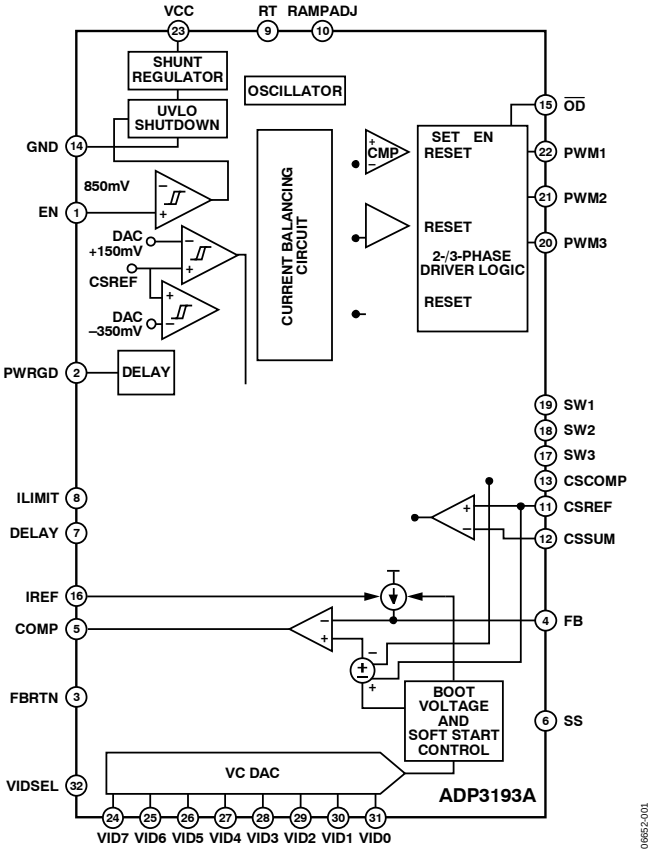

Figure 1.

The ADP3193A has a built-in shunt regulator that allows the part to be connected to the 12 V system supply through a series resistor.

The ADP3193A is specified over the extended commercial temperature range of 0°C to 85°C and is available in a 32-lead LFCSP.

[1] Protected by U.S. Patent Number 6,683,441; other patents pending.

February 2008 – Rev. 1

Publication Order Number:
ADP3193A/D

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REVISION HISTORY

0 /0 **1**

0 /0 **0**

SPECIFICATIONS

VCC = 5 V, FBRTN = GND, T_A = 0°C to 85°C, unless otherwise noted.[1]

. ⁄ **1.**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
REFERENCE CURRENT						
Reference Bias Voltage	V_{IREF}			1.5		V
Reference Bias Current	I_{IREF}	R_{IREF} = 100 kΩ	14.25	15	15.75	µA
ERROR AMPLIFIER						
Output Voltage Range[2]	V_{COMP}		0		4.4	V
Accuracy	V_{FB}	Relative to nominal DAC output, referenced to FBRTN (see Figure 4)	−7.7		+7.7	mV
	$V_{FB(BOOT)}$	In startup	1.092	1.1	1.108	V
Differential Nonlinearity			−1		+1	LSB
Input Bias Current	I_{FB}	$I_{FB} = I_{IREF}$	13.5	15	16.5	µA
FBRTN Current	I_{FBRTN}			65	200	µA
Output Current	I_{COMP}	FB forced to V_{OUT} − 3%		500		µA
Gain Bandwidth Product	$GBW_{(ERR)}$	COMP = FB		20		MHz
Slew Rate		COMP = FB		25		V/µs
Boot Voltage Hold Time	t_{BOOT}	C_{DELAY} = 10 nF		2		ms
VID INPUTS						
Input Low Voltage	$V_{IL(VID)}$	VID(x), VIDSEL			0.4	V
Input High Voltage	$V_{IH(VID)}$	VID(x), VIDSEL	0.8			V
Input Current	$I_{IN(VID)}$			−1		µA
VID Transition Delay Time[2]		VID code change to FB change	400			ns
No CPU Detection Turn-Off Delay Time[2]		VID code change to PWM going low	5			µs
OSCILLATOR						
Frequency Range[2]	f_{OSC}		0.25		4	MHz
Frequency Variation	f_{PHASE}	T_A = 25°C, R_T = 210 kΩ, 3-phase	240	260	293	kHz
		T_A = 25°C, R_T = 100 kΩ, 3-phase		530		kHz
		T_A = 25°C, R_T = 40 kΩ, 3-phase		1000		kHz
Output Voltage	V_{RT}	R_T = 243 kΩ to GND	1.9	2.0	2.1	V
RAMPADJ Output Voltage	$V_{RAMPADJ}$	RAMPADJ − FB	−50		+50	mV
RAMPADJ Input Current Range	$I_{RAMPADJ}$		1		50	µA
CURRENT SENSE AMPLIFIER						
Offset Voltage	$V_{OS(CSA)}$					

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CURRENT LIMIT COMPARATOR						
ILIMIT Bias Current	I_{ILIMIT}	I_{ILIMIT} = 2/3 × I_{IREF}	9	10	11	μA
ILIMIT Voltage	V_{ILIMIT}	R_{ILIMIT} = 121 kΩ (V_{ILIMIT} = (I_{ILIMIT} × R_{ILIMIT}))	1.09	1.21	1.33	V
Maximum Output Voltage			3			V
Current-Limit Threshold Voltage	V_{CL}	V_{CSREF} − V_{CSCOMP}, R_{ILIMIT} = 121 kΩ	80	100	125	mV
Current-Limit Setting Ratio		V_{CL}/V_{ILIMIT}		82.6		mV/V
DELAY TIMER						
Normal Mode Output Current	I_{DELAY}	I_{DELAY} = I_{IREF}	12	15	18	μA
Output Current in Current Limit	$I_{DELAY(CL)}$	$I_{DELAY(CL)}$ = 0.25 × I_{IREF}	3.0	3.75	4.5	μA
Threshold Voltage	$V_{DELAY(TH)}$		1.6	1.7	1.8	V
SOFT START						
Output Current	I_{SS}	During startup, I_{SS} = I_{IREF}	12	15	18	μA
ENABLE INPUT						
Threshold Voltage	$V_{TH(EN)}$		800	850	900	mV

6400633.12 .M f BT 9 0 0 9 45.36 637.5601-4ILtup, I

TEST CIRCUITS

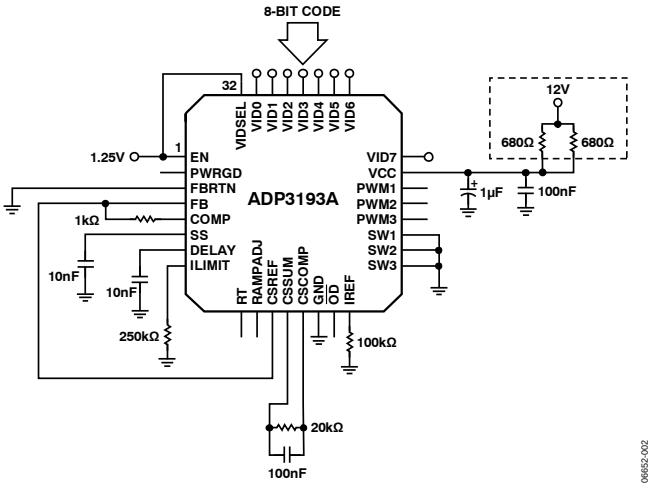
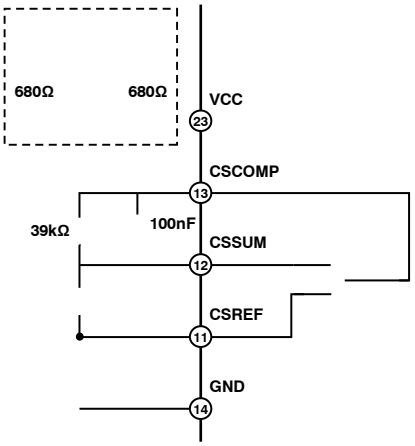


Figure 4. Closed-Loop Output Voltage Accuracy



MASTER CLOCK FREQUENCY

The clock frequency of the ADP3193A is set with an external resistor connected from the RT pin to ground. The frequency follows the graph in Figure 3. To determine the frequency per phase, the clock is divided by the number of phases in use. If all phases are in use, divide by 3. If PWM3 is tied to VCC, divide the master clock by 2 for the frequency of the remaining phases.

OUTPUT VOLTAGE DIFFERENTIAL SENSING

The ADP3193A includes differential sensing, high accuracy VID DAC and reference, and a low offset error amplifier. This maintains a worst-case specification of ±7.7 mV differential sensing error over its full operating output voltage and temperature range. The output voltage is sensed between the FB pin and the FBRTN pin. FB should be connected through a resistor to the regulation point, usually the remote sensing pin of the microprocessor. FBRTN should be connected directly to the remote sensing ground point. The internal VID DAC and precision reference are referenced to FBRTN, which has a minimal current of 65 μA to allow accurate remote sensing. The internal error amplifier compares the output of the DAC to the FB pin to regulate the output voltage.

OUTPUT CURRENT SENSING

The ADP3193A provides a dedicated current sense amplifier (CSA) to monitor the total output current for proper voltage positioning vs. load current and for current-limit detection. Sensing the load current at the output gives the total average current being delivered to the load, which is an inherently more accurate method than peak current detection or sampling the current across a sensing element, such as the low-side MOSFET. Depending on the objectives of the system, this amplifier can be configured in several ways:

Output inductor DCR sensing without a thermistor for lowest cost.
Output inductor DCR sensing with a thermistor for improved accuracy in tracking inductor temperature.
Sensing resistor for highest accuracy measurements.

The positive input of the CSA is connected to the CSREF pin, which is connected to the output voltage. The inputs to the amplifier are summed together through resistors from the sensing element, such as the switch node side of the output inductors,
to the inverting input CSSUM. The feedback resistor between CSCOMP and CSSUM sets the gain of the amplifier, and a filter capacitor is placed in parallel with this resistor. The gain of the amplifier is programmable by adjusting the feedback resistor.

The difference between CSREF and CSCOMP is also used as a differential input for the current-limit comparator.

To provide the best accuracy for sensing current, the CSA has a low offset input voltage and the sensing gain is set by the external resistor.

CURRENT CONTROL MODE AND THERMAL BALANCE

The ADP3193A has individual inputs (SW1 to SW3) for each phase that are used to monitor the current. This information is combined with an internal ramp to create a current-balancing

respect to the VID DAC. The main loop compensation is incorporated into the feedback network between FB and COMP pins.

CURRENT REFERENCE

The IREF pin is used to set an internal current reference. This reference current sets I_{FB}, I_{DELAY}, I_{SS}, and I_{LIMIT}. A resistor to ground programs the current based on the 1.5 V output.

$$IREF = \frac{1.5\,V}{R_{IREF}}$$

Typically, R_{IREF} is set to 100 kΩ to program $IREF$ = 15 μA. Therefore,

$I_{FB} = IREF = 15\ \mu A$

$I_{DELAY} = IREF = 15\ \mu A$

$I_{SS} = IREF = 15\ \mu A$

$I_{LIMIT} = 2/3\ (IREF) = 10\ \mu A$

FAST ENHANCED PWM MODE

Fast enhanced PWM mode is intended to improve the transient response of the ADP3193A to a load step-up. In previous generations of controllers, when a load step-up occurred, the controller could only respond to the load change after the PWM signal was turned on. Enhanced PWM mode allows the controller to immediately respond when a load step-up occurs. This allows the phases to respond more quickly when a load increase takes place.

DELAY TIMER

The delay times for the start-up timing sequence are set with a capacitor from the DELAY pin to ground. In UVLO or when EN is logic low, the DELAY pin is held at ground. After the

DELAY pin timing capacitor with the start-up sequence timing.

OUTPUT ENABLE AND UVLO

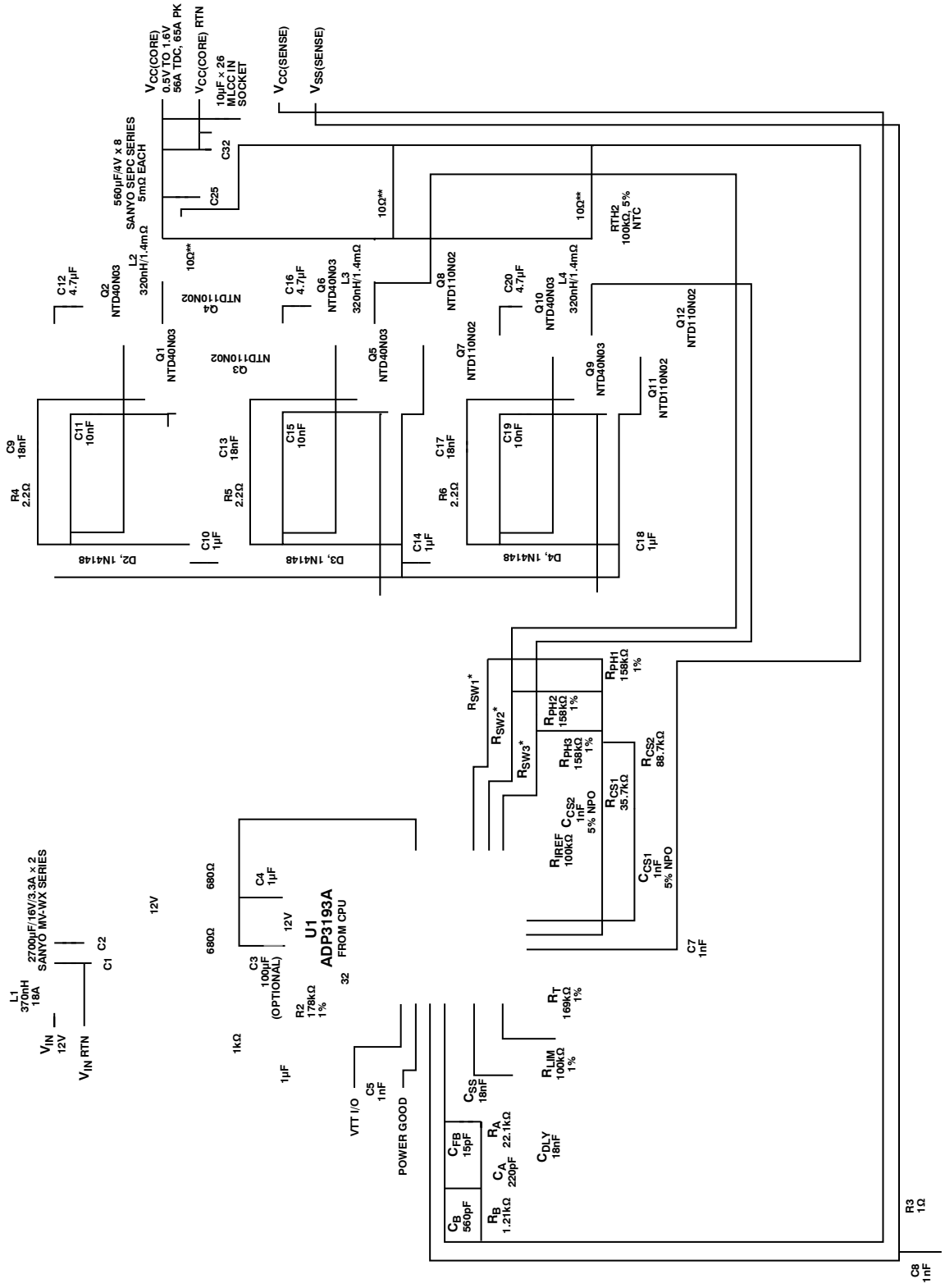
For the ADP3193A to begin switching, the input supply (VCC) to the controller must be higher than the UVLO threshold and the EN pin must be higher than its 0.85 V threshold. This initiates a system start-up sequence. If either UVLO or EN is less than its respective threshold, the ADP3193A is disabled. This holds the PWM outputs at ground, shorts the DELAY capacitor to ground, and forces PWRGD and $\overline{OD}$ signals low.

In the application circuit (see Figure 10), the $\overline{OD}$ pin should be connected to the $\overline{OD}$ inputs of the ADP3120A drivers. Grounding $\overline{OD}$ disables the drivers such that both DRVH and DRVL are grounded. This feature is important in preventing the discharge of the output capacitors when the controller is shut off. If the driver outputs are not disabled, a negative voltage can be generated during output due to the high current discharge of the output capacitors through the inductors.

	VR11 DAC Codes: VIDSEL = High								VR10.x DAC Codes: VIDSEL = Low						
Output	**VID7**	**VID6**	**VID5**	**VID4**	**VID3**	**VID2**	**VID1**	**VID0**	**VID4**	**VID3**	**VID2**	**VID1**	**VID0**	**VID5**	**VID6**
1.32500	0	0	1	0	1	1	1	0	1	0	1	0	1	1	1
1.31875	0	0	1	0	1	1	1	1	1	0	1	0	1	1	0
1.31250	0	0	1	1	0	0	0	0	1	0	1	1	0	0	1
1.30625	0	0	1	1	0	0	0	1	1	0	1	1	0	0	0
1.30000	0	0	1	1	0	0	1	0	1	0	1	1	0	1	1
1.29375	0	0	1	1	0	0	1	1	1	0	1	1	0	1	0
1.28750	0	0	1	1	0	1	0	0	1	0	1	1	1	0	1
1.28125	0	0	1	1	0	1	0	1	1	0	1	1	1	0	0
1.27500	0	0	1	1	0	1	1	0	1	0	1	1	1	1	1
1.26875	0	0	1	1	0	1	1	1	1	0	1	1	1	1	0
1.26250	0	0	1	1	1	0	0	0	1	1	0	0	0	0	1
1.25625	0	0	1	1	1	0	0	1	1	1	0	0	0	0	0
1.25000	0	0	1	1	1	0	1	0	1	1	0	0	0	1	1
1.24375	0	0	1	1	1	0	1	1	1	1	0	0	0	1	0
1.23750	0	0	1	1	1	1	0	0	1	1	0	0	1	0	1
1.23125	0	0	1	1	1	1	0	1	1	1	0	0	1	0	0
1.22500	0	0	1	1	1	1	1	0	1	1	0	0	1	1	1
1.21875	0	0	1	1	1	1	1	1	1	1	0	0	1	1	0
1.21250	0	1	0	0	0	0	0	0	1	1	0	1	0	0	1
1.20625	0	1	0	0	0	0	0	1	1	1	0	1	0	0	0
1.20000	0	1	0	0	0	0	1	0	1	1	0	1	0	1	1
1.19375	0	1	0	0	0	0	1	1	1	1	0	1	0	1	0
1.18750	0	1	0	0	0	1	0	0	1	1	0	1	1	0	1
1.18125	0	1	0	0	0	1	0	1	1	1	0	1	1	0	0
1.17500	0	1	0	0	0	1	1	0	1	1	0	1	1	1	1
1.16875	0	1	0	0	0	1	1	1	1	1	0	1	1	1	0
1.16250	0	1	0	0	1	0	0	0	1	1	1	0	0	0	1
1.15625	0	1	0	0	1	0	0	1	1	1	1	0	0	0	0
1.15000	0	1	0	0	1	0	1	0	1	1	1	0	0	1	1
1.14375	0	1	0	0	1	0	1	1	1	1	1	0	0	1	0
1.13750	0	1	0	0	1	1	0	0	1	1	1	0	1	0	1
1.13125	0	1	0	0	1	1	0	1	1	1	1	0	1	0	0
1.12500	0	1	0	0	1	1	1	0	1	1	1	0	1	1	1
1.11875	0	1	0	0	1	1	1	1	1	1	1	0	1	1	0
1.11250	0	1	0	1	0	0	0	0	1	1	1	1	0	0	1
1.10625	0	1	0	1	0	0	0	1	1	1	1	1	0	0	0
1.10000	0	1	0	1	0	0	1	0	1	1	1	1	0	1	1
1.09375	0	1	0	1	0	0	1	1	1	1	1	1	0	1	0
Off	N/A								1	1	1	1	1	0	1
Off	N/A								1	1	1	1	1	0	0
Off	N/A								1	1	1	1	1	1	1
Off	N/A								1	1	1	1	1	1	0
1.08750	0	1	0	1	0	1	0	0	0	0	0	0	0	0	1
1.08125	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0
1.07500	0	1	0	1	0	1	1	0	0	0	0	0	0	1	1
1.06875	0	1	0	1	0	1	1	1	0	0	0	0	0	1	0
1.06250	0	1	0	1	1	0	0	0	0	0	0	0	1	0	1
1.05625	0	1	0	1	1	0	0	1	0	0	0	0	1	0	0
1.05000	0	1	0	1	1	0	1	0	0	0	0	0	1	1	1
1.04375	0	1	0	1	1	0	1	1	0	0	0	0	1	1	0
1.03750	0	1	0	1	1	1	0	0	0	0	0	1	0	0	1
1.03125	0	1	0	1	1	1	0	1	0	0	0	1	0	0	0
1.02500	0	1	0	1	1	1	1	0	0	0	0	1	0	1	1
1.01875	0	1	0	1	1	1	1	1	0	0	0	1	0	1	0
1.01250	0	1	1	0	0	0	0	0	0	0	0	1	1	0	1
1.00625	0	1	1	0	0	0	0	1	0	0	0	1	1	0	0
1.00000	0	1	1	0	0	0	1	0	0	0	0	1	1	1	1
0.99375	0	1	1	0	0	0	1	1	0	0	0	1	1	1	0

	VR11 DAC Codes: VIDSEL = High								VR10.x DAC Codes: VIDSEL = Low						
Output	**VID7**	**VID6**	**VID5**	**VID4**	**VID3**	**VID2**	**VID1**	**VID0**	**VID4**	**VID3**	**VID2**	**VID1**	**VID0**	**VID5**	**VID6**
0.98750	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1

	VR11 DAC Codes: VIDSEL = High								VR10.x DAC Codes: VIDSEL = Low						
Output	**VID7**	**VID6**	**VID5**	**VID4**	**VID3**	**VID2**	**VID1**	**VID0**	**VID4**	**VID3**	**VID2**	**VID1**	**VID0**	**VID5**	**VID6**
0.62500	1	0	0	1	1	1	1	0	N/A						
0.61875	1	0	0	1	1	1	1	1	N/A						
0.61250	1	0	1	0	0	0	0	0	N/A						
0.60625	1	0	1	0	0	0	0	1	N/A						
0.60000	1	0	1	0	0	0	1	0	N/A						
0.59375	1	0	1	0	0	0	1	1	N/A						
0.58750	1	0	1	0	0	1	0	0	N/A						
0.58125	1	0	1	0	0	1	0	1	N/A						
0.57500	1	0	1	0	0	1	1	0	N/A						
0.56875	1	0	1	0	0	1	1	1	N/A						
0.56250	1	0	1	0	1	0	0	0	N/A						
0.55625	1	0	1	0	1	0	0	1	N/A						
0.55000	1	0	1	0	1	0	1	0	N/A						
0.54375	1	0	1	0	1	0	1	1	N/A						
0.53750	1	0	1	0	1	1	0	0	N/A						
0.53125	1	0	1	0	1	1	0	1	N/A						
0.52500	1	0	1	0	1	1	1	0	N/A						
0.51875	1	0	1	0	1	1	1	1	N/A						
0.51250	1	0	1	1	0	0	0	0	N/A						
0.50625	1	0	1	1	0	0	0	1	N/A						
0.50000	1	0	1	1	0	0	1	0	N/A						
Off	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0
Off	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1


VCC(CORE) 0.5V TO 1.6V 56A TDC, 65A PK
VCC(CORE) RTN
10µF × 26 MLCC IN SOCKET
VCC(SENSE)
VSS(SENSE)
560µF/4V x 8 SANYO SEPC SERIES 5mΩ EACH
C32
C25
10Ω**
RTH2 100kΩ, 5% NTC
L2 320nH/1.4mΩ
L3 320nH/1.4mΩ
L4 320nH/1.4mΩ
C12 4.7µF
C16 4.7µF
C20 4.7µF
Q2 NTD40N03
Q4 NTD110N02
Q6 NTD40N03
Q8 NTD110N02
Q10 NTD40N03
Q12 NTD110N02
Q1 NTD40N03
Q3 NTD110N02
Q5 NTD40N03
Q7 NTD110N02
Q9 NTD40N03
Q11 NTD110N02
C9 18nF
C11 10nF
C13 18nF
C15 10nF
C17 18nF
C19 10nF
R4 2.2Ω
R5 2.2Ω
R6 2.2Ω
C10 1µF
C14 1µF
C18 1µF
D2, 1N4148
D3, 1N4148
D4, 1N4148
RSW1*
RSW2*
RSW3*
RPH1 158kΩ 1%
RPH2 158kΩ 1%
RPH3 158kΩ 1%
RCS2 88.7kΩ
RCS1 35.7kΩ
CCS2 10F 5% NPO
RIREF 100kΩ
CCS1 1nF 5% NPO
C7 1nF
L1 370nH 18A
2700µF/16V/3.3A x 2 SANYO MV-WX SERIES
C2
C1
VIN 12V
VIN RTN
12V
680Ω
680Ω
C4 1µF
C3 100µF (OPTIONAL)
12V
U1
ADP3193A
FROM CPU
32
R2 178kΩ 1%
1kΩ
1µF
VTT I/O
C5 1nF
POWER GOOD
CSS 18nF
RLIM 100kΩ 1%
RT 169kΩ 1%
CFB 15pF
RA 22.1kΩ
CA 220pF
CDLY 18nF
CB 560pF
RB 1.21kΩ
R3 1Ω
C8 1nF

APPLICATION INFORMATION

The design parameters for a typical Intel VRD 11 compliant CPU application are as follows:

Input voltage (V_{IN}) = 12 V
VID setting voltage (V_{VID}) = 1.400 V
Duty cycle (D) = 0.117
Nominal output voltage at no load (V_{ONL}) = 1.381 V
Nominal output voltage at 65 A load (V_{OFL}) = 1.316 V
Static output voltage drop based on a 1.0 mΩ load line (R_O) from no load to full load (V_D) = $V_{ONL} - V_{OFL}$ = 1.381 V − 1.316 V = 65 mV
Maximum output current (I_O) = 65 A
Maximum output current step (ΔI_O) = 50 A
Maximum output current slew rate (S_R) = 200 A/μs
Number of phases (n) = 3
Switching frequency per phase (f_{SW}) = 330 kHz

SETTING THE CLOCK FREQUENCY

The ADP3193A uses a fixed-frequency control architecture. The frequency is set by an external timing resistor (R_T). The clock frequency and the number of phases determine the switching frequency per phase, which relates directly to switching losses as well as to the sizes of the inductors, the input capacitors, and the output capacitors. With n = 3 for three phases, a clock frequency of 990 kHz sets the switching frequency (f_{SW}) of each

C_{OUT} SELECTION

The required output decoupling for the regulator is typically

POWER MOSFETS

For our example, the N-channel power MOSFETs have been selected for one high-side switch and two low-side switches per phase. The main selection parameters for the power MOSFETs are $V_{GS(TH)}$, Q_G, C_{ISS}, C_{RSS}, and $R_{DS(ON)}$. The minimum gate drive voltage (the supply voltage to the ADP3120A) dictates whether standard threshold or logic-level threshold MOSFETs must be used. With V_{GATE} ~10 V, logic-level threshold MOSFETs ($V_{GS(TH)}$ < 2.5 V) are recommended.

The maximum output current (I_O) determines the $R_{DS(ON)}$ requirement for the low-side (synchronous) MOSFETs. With

Also shown is the standby dissipation factor ($I_{CC} \times V_{CC}$) of the driver. For the ADP3120A, the maximum dissipation should be less than 400 mW. In this example, with I_{CC} = 7 mA, Q_{GMF} = 5.8 nC, and Q_{GSF} = 48 nC, there is 191 mW in each driver, which is below the 400 mW dissipation limit. See the ADP3120A data sheet for more details.

RAMP RESISTOR SELECTION

The ramp resistor (R_R) is used for setting the size of the internal PWM ramp. The value of this resistor should be chosen to provide the best combination of thermal balance, stability, and transient response. Equation 23 is used for determining the optimum value.

FEEDBACK LOOP COMPENSATION DESIGN

TUNING PROCEDURE FOR ADP3193A

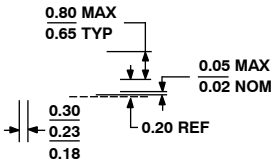
Set Up and Test the Circuit

1. Build a circuit based on the compensation values computed from the design spreadsheet.
2. Connect a dc load to the circuit.
3. Turn on the ADP3193A and verify that it operates properly.
4. Check for jitter with no load and full load conditions.

Set the DC Load Line

1. Measure the output voltage with no load (V_{NL}) and verify that it is within the specified tolerance range.
2. Measure the output voltage with a full load when the device is cold (V_{FLCOLD}). Allow the board to run for ~10 minutes at full load, and then measure the output when the device is hot (V_{FLHOT}). If the difference between the two

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2