6-Bit Programmable 2- to 4-Phase Synchronous Buck Controller

ADP3196

FEATURES

Selectable 2-, 3-, or 4-phase operation at up to 1 MHz per phase
±10 mV worst-case differential sensing error over temperature
Logic-level PWM outputs for interface to external high power drivers
Enhanced PWM flex mode for excellent load transient performance

Ayla(cas)12ch-sp5 1 oeacascas

VRM modules

GENERAL DESCRIPTION

The ADP3196[1] is a highly efficient multiphase synchronous buck switching regulator controller optimized for converting a 12 V main supply into the core supply voltage required by high performance Advanced Micro Devices, Inc. (AMD) processors. It uses an internal 6-bit DAC to read a voltage identification (VID) code directly from the processor, which is used to set the output voltage between 0.3750 V and 1.55 V.

This device uses a multimode PWM architecture to drive the logic-level outputs at a programmable switching frequency that can be optimized for VR size and efficiency. The phase relationship of the output signals can be programmed to provide 2-, 3-, or 4-phase operation, allowing for the construction of up to four complementary buck switching stages.

The ADP3196 supports a programmable slope function to adjust the output voltage as a function of the load current so that it is always optimally positioned for a system transient. This can be disabled by connecting Pin LLSET to Pin CSREF.

FUNCTIONAL BLOCK DIAGRAM

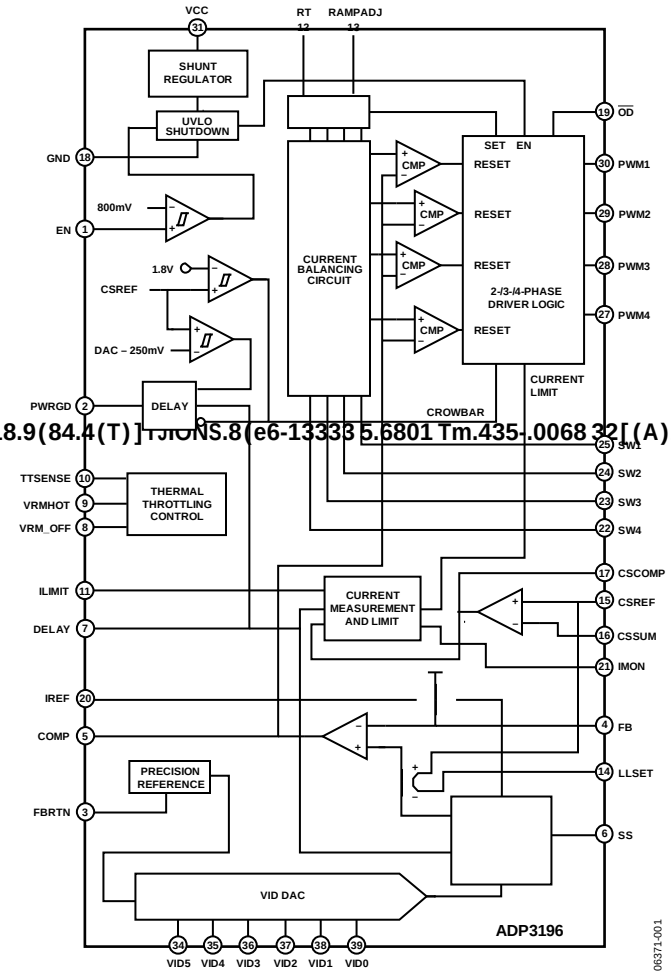


Figure 1. Functional Block Diagram

The ADP3196 also provides accurate and reliable short-circuit protection, adjustable current limiting, and a delayed power-good output that accommodates on-the-fly output voltage changes requested by the CPU. The ADP3196 has a built-in shunt regulator that allows the part to be connected to the 12 V system supply through a series resistor.

The ADP3196 is specified over the extended commercial temperature range of 0°C to +85°C and is available in a 40-lead LFCSP.

TABLE OF CONTENTS

Features....1
Applications....1

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
						µ

TEST CIRCUITS

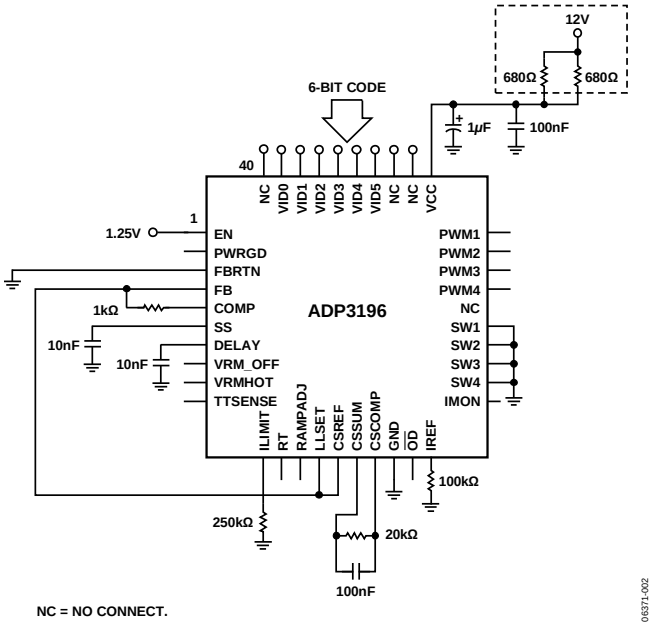
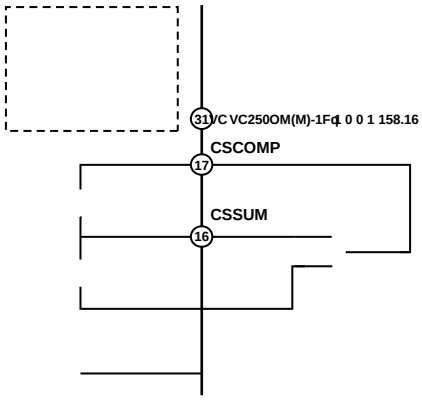
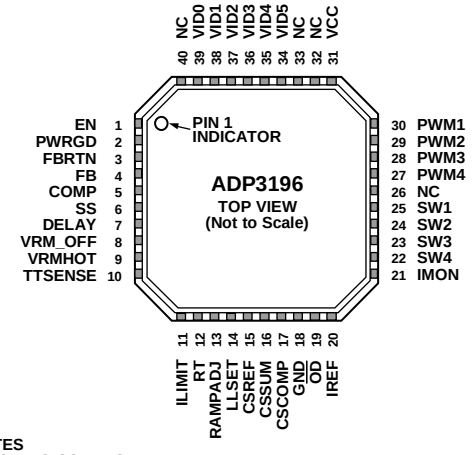


Fig e 2.C l ed-L O \i l age Acc ac



1 0 0 1 158.16 306.84 cm 0 2792.28 0 3.96 1.68 3.96 3.72 c3.96 6 2.28 7.68 0 7.68 c-2.28 7.68 -4.08 6 -4.08 3.72 c-4.08 1.68 -2.28 0 0 0 c Q BT 4.9964 0 0 4.996 155.4 308.88 Tm 0 286

PIN CONFIGURATION AND FUNCTION DESCRIPTION



NOTES
1. NC = NO CONNECT.
2. THE EXPOSED EPAD ON BOTTOM SIDE OF PACKAGE IS AN ELECTRICAL CONNECTION AND SHOULD BE SOLDERED TO GROUND.

Fig e 5. Pi C fig a i

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description

ADP3196

THEORY OF OPERATION

The ADP3196 combines a multimode, fixed frequency PWM control with multiphase logic outputs for use in 2-, 3-, and 4-phase synchronous buck CPU core supply power converters. The internal VID DAC is designed to interface with the AMD 6-bit CPUs.

Multiphase operation is important for producing the high

MASTER CLOCK FREQUENCY

To increase the current in any given phase, make R_{SW} for that phase larger (make R_{SW} = 0 for the hottest phase and do not change during balancing). Increasing R_{SW} to only 500 Ω makes a substantial increase in phase current. Increase each R_{SW} value by small amounts to achieve balance, starting with the coolest phase first.

VOLTAGE CONTROL MODE

A high gain, high bandwidth voltage mode error amplifier is

Table 4. VID Codes

OUTPUT	VID5	VID4	VID3	VID2	VID1	VID0
[illegible]						
[illegible]						[illegible]
[illegible]					[illegible]	
[illegible]					[illegible]	[illegible]
[illegible]				[illegible]		
[illegible]				[illegible]		[illegible]
[illegible]				[illegible]	[illegible]	
[illegible]				[illegible]	[illegible]	[illegible]
[illegible]			[illegible]			
[illegible]			[illegible]			[illegible]
[illegible]			[illegible]		[illegible]	
[illegible]			[illegible]		[illegible]	[illegible]
[illegible]			[illegible]	[illegible]		
[illegible]			[illegible]	[illegible]		[illegible]
[illegible]			[illegible]	[illegible]	[illegible]	
[illegible]			[illegible]	[illegible]	[illegible]	[illegible]
[illegible]		[illegible]				
[illegible]		[illegible]				[illegible]
[illegible]		[illegible]			[illegible]	
[illegible]		[illegible]			[illegible]	[illegible]
[illegible]		[illegible]		[illegible]		
[illegible]		[illegible]		[illegible]		[illegible]
[illegible]		[illegible]		[illegible]	[illegible]	
[illegible]		[illegible]		[illegible]	[illegible]	[illegible]
[illegible]		[illegible]	[illegible]			
[illegible]		[illegible]	[illegible]			[illegible]
[illegible]		[illegible]	[illegible]		[illegible]	
[illegible]		[illegible]	[illegible]		[illegible]	[illegible]
[illegible]		[illegible]	[illegible]	[illegible]		
[illegible]		[illegible]	[illegible]	[illegible]		[illegible]
[illegible]		[illegible]	[illegible]	[illegible]	[illegible]	
[illegible]		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

OUTPUT	VID5	VID4	VID3	VID2	VID1	VID0

LAYOUT AND COMPONENT PLACEMENT

The following guidelines are recommended for optimal performance of a switching regulator in a PC system.

G [illegible]

For good results, a PCB with at least four layers is recommended. This provides the needed versatility for control circuitry interconnections with optimal placement, power planes for ground, input and output power, and wide interconnection traces in the remainder of the power delivery current paths. Keep in mind that each square unit of 1-ounce copper trace has a resistance of ~0.53 mΩ at room temperature.

Whenever high currents must be routed between PCB layers, use vias liberally to create several parallel current paths, so the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.

If critical signal lines (including the output voltage sense lines of the ADP3196) must cross through power circuitry, it is best to interpose a signal ground plane between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of making signal ground a bit noisier.

An analog ground plane should be used around and under the ADP3196 as a reference for the components associated with the controller. This plane should be tied to the nearest output decoupling capacitor ground and should not be tied to any other power circuitry to prevent power currents from flowing into it.

The components around the ADP3196 should be located close to the controller with short traces. The most important traces to keep short and away from other traces are the FB pin and CSSUM pin. The output capacitors should be connected as close as possible to the load (or connector), for example, a microprocessor core, that receives the power. If the load is distributed, the capacitors should also be distributed and generally be in proportion to where the load tends to be more dynamic.

Avoid crossing any signal lines over the switching power path loop (described in the Power Circuitry Recommendations section).

P C [illegible]

The switching power path should be routed on the PCB to encompass the shortest possible length to minimize radiated switching noise energy (EMI) and conduction losses in the board. Failure to take proper precautions often results in EMI problems for the entire PC system and noise-related operational problems in the power converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors and the power MOSFETs, including all interconnecting PCB traces and planes. Using short and wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which can cause high energy ringing; and it accommodates the high current demand with minimal voltage loss.

When a power dissipating component, for example, a power MOSFET, is soldered to a PCB, it is recommended to liberally use the vias, both directly on the mounting pad and immediately surrounding it. Two important reasons for this are improved current rating through the vias and improved thermal performance from vias extended to the opposite side of the PCB, where a plane can more readily transfer the heat to the air. Make a mirror image of any pad being used to heat sink the MOSFETs on the opposite side of the PCB to achieve the best thermal dissipation in the air around the board. To further improve thermal performance, use the largest possible pad area.

The output power path should also be routed to encompass a short distance. The output power path is formed by the current path through the inductor, the output capacitors, and the load.

For best EMI containment, a solid power ground plane should be used as one of the inner layers extending fully under all the power components.

C [illegible]

The output voltage is sensed and regulated between the FB pin and the FBRTN pin, which connect to the signal ground at the load. To avoid differential mode noise pickup in the sensed signal, the loop area should be small. Thus, the FB trace and FBRTN trace should be routed adjacent to each other on top of the power ground plane back to the controller.

The feedback traces from the switch nodes should be connected as close as possible to the inductor. The CSREF signal should be connected to the output voltage at the nearest inductor to the controller.