8-Bit Programmable 2- to 4-Phase Synchronous Buck Controller

ADP3198

FEATURES

Se ec ab e 2-, 3-, 4- a e e a , a
1 MH e a e
–11 V -ca ed ffe e a e , e e
e e a e
L c- e e PWM f face e e , a
e d e
E a ced PWM f e de f e ce e ad a e
e f a ce
Ac e c e ba a c, be ee a, a e
B -, e - d/c ba b a , - e-f
VID c de c a e
D a, a ab e 0.5 V 1.6 V b
VR10. a d VR11 ec f ca ,
P a ab e -c c ec , a ab e
a c - ff de a

APPLICATIONS

De PC e e f , e e a ,
l e ce
VRM d e

GENERAL DESCRIPTION

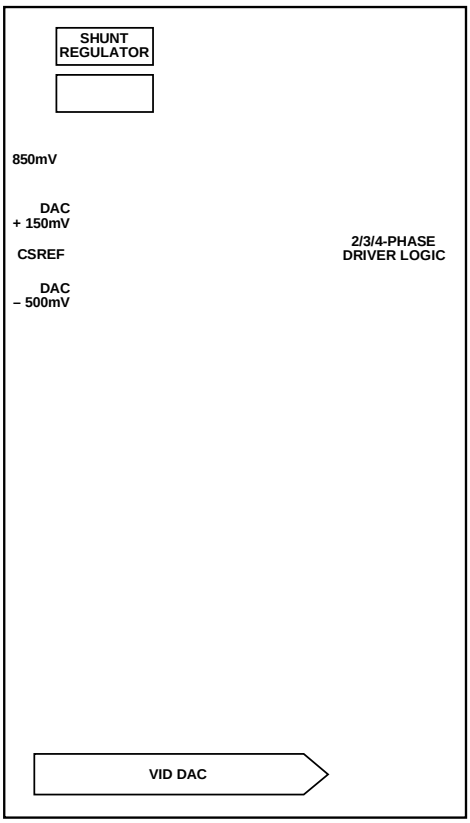
The ADP3198[1] is a highly efficient, multiphase, synchronous buck switching regulator controller optimized for converting a 12 V main supply into the core supply voltage required by high performance Intel processors. It uses an internal 8-bit DAC to read a voltage identification (VID) code directly from the processor, which is used to set the output voltage between 0.5 V and 1.6 V.

This device uses a multimode PWM architecture to drive the logic-level outputs at a programmable switching frequency that can be optimized for VR size and efficiency. The phase relationship of the output signals can be programmed to provide 2-, 3-, or 4-phase operation, allowing for the construction of up to four complementary buck switching stages.

The ADP3198 also includes programmable no load offset and slope functions to adjust the output voltage as a function of the load current, optimally positioning it for a system transient. The ADP3198 also provides accurate and reliable short-circuit protection, adjustable current limiting, and a delayed power-good output that accommodates on-the-fly output voltage changes requested by the CPU.

[1] P . b U.S. P N b 6,683,441; .

FUNCTIONAL BLOCK DIAGRAM



P b N b :
ADP3198/D

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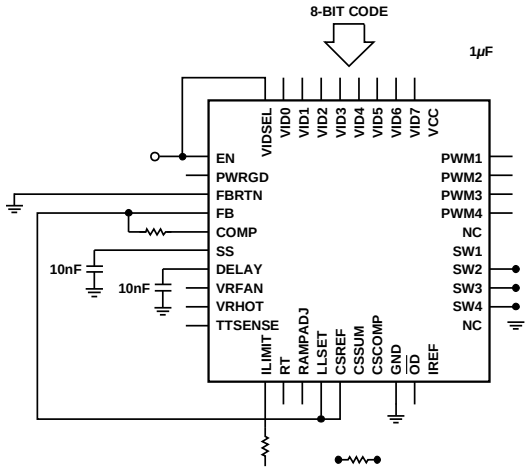
SPECIFICATIONS

VCC = 5 V, FBRTN = GND, T_A = 0°C to 85°C, unless otherwise noted.[1]

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
REFERENCE CURRENT						
Reference Current	I_{REF}			1.5		
Reference Current	I_{REF}	R_{REF} = 100 kΩ	14.25	15	15.75	
REFERENCE VOLTAGE						
Reference Voltage	V_{REF}		0		4.4	

TEST CIRCUITS



ABSOLUTE MAXIMUM RATINGS

Table 2.

P. N.	M e . c	De c . ,
20	R F'	C R . . . . . F D 'Y, SS, , S NS .'
21	'N	' . R .
22 25	S 4 S 1	C . . . . . S b .
26	N	N C . .
27 30	P 4 P 1	. - P ' . . . . 'SF . . . DP3110 C . P 4, P 3 CC . , . DP3198 2-, 3-, 4- . .
31	CC	S D . . 340 b . b 12 CC . . . . CC = 5 .
32 39	D7 D0	. DC . . GND, . 0 . . , DC F 0.5 1.6 (b 4).
40	DS '	D DC S . P . . . . D DC . D0 D7 R10 R11 . .

MASTER CLOCK FREQUENCY

The clock frequency of the ADP3198 is set with an external

CURRENT-LIMIT, SHORT-CIRCUIT, AND LATCH-OFF PROTECTION

The ADP3198 compares a programmable current-limit set point to the voltage from the output of the current-sense

OUTPUT CROWBAR

To protect the load and output components of the supply, the PWM outputs are driven low, which turns on the low-side MOSFETs when the output voltage exceeds the upper crowbar threshold. This crowbar action stops once the output voltage falls below the release threshold of approximately 375 mV.

Turning on the low-side MOSFETs pulls down the output as the reverse current builds up in the inductors. If the output overvoltage is due to a short in the high-side MOSFET, this action current limits the input supply or blows its fuse, protecting the microprocessor from being destroyed.

OUTPUT ENABLE AND UVLO

For the ADP3198 to begin switching, the input supply (VCC) to the controller must be higher than the UVLO threshold and the EN pin must be higher than its 0.85 V threshold. This initiates a system start-up sequence. If either UVLO or EN is less than their respective thresholds, the ADP3198 is disabled. This holds the PWM outputs at ground, shorts the DELAY capacitor to ground, and forces PWRGD and $\overline{OD}$ signals low.

In the application circuit (see Figure 10), the $\overline{OD}$ pin should be connected to the $\overline{OD}$ inputs of the ADP3110A drivers.

Grounding $\overline{OD}$ disables the drivers such that both DRVH and DRVL are grounded. This feature is important in preventing the discharge of the output capacitors when the controller is shut off. If the driver outputs are not disabled, a negative voltage can be generated during output due to the high current discharge of the output capacitors through the inductors.

THERMAL MONITORING

The ADP3198 includes a thermal-monitoring circuit to detect when a point on the VR has exceeded two different user-defined temperatures. The thermal-monitoring circuit requires an NTC thermistor to be placed between TTSENSE and GND.

A fixed current of 8 × IREF (normally giving 123 µA) is sourced out of the TTSENSE pin and into the thermistor. The current source is internally limited to 5 V. An internal circuit compares the TTSENSE voltage to a 1.105 V and a 0.81 V threshold, and outputs an open-drain signal at the VRFAN and VRHOT outputs, respectively. Once the voltage on the TTSENSE pin drops below its respective threshold, the open-drain outputs assert high to signal the system that an overtemperature event has occurred. Because the TTSENSE voltage changes slowly with respect to time, 50 mV of hysteresis is built into these comparators. The thermal monitoring circuitry does not depend on EN and is active when UVLO is above its threshold. When UVLO is below its threshold, VRFAN and VRHOT are forced low.

Table 4.VR11 and VR10.x VID Codes for the ADP3198

The user has the flexibility to choose either R_{CS} or $R_{PH(X)}$. However, it is best to select R_{CS} equal to 100 kΩ, and then solve for $R_{PH(X)}$ by rearranging Equation 6. Here, $R_{CSA} = R_O = 1$ mΩ because this is equal to the design load line.

$$R_{PH(\ )} = \frac{R_L}{R_{C\bullet A}} \times R_{C\bullet}$$

$$R_{PH(\ )} = \frac{1.4\ \text{m}\Omega}{1.0\ \text{m}\Omega} \times 100\ \text{k}\Omega = 140\ \text{k}\Omega$$

Next, use Equation 7 to solve for C_{CS}.

$$C_{C\bullet} = \frac{320\ \text{nH}}{1.4\ \text{m}\Omega \times 100\ \text{k}\Omega} = 2.28\ \text{nF}$$

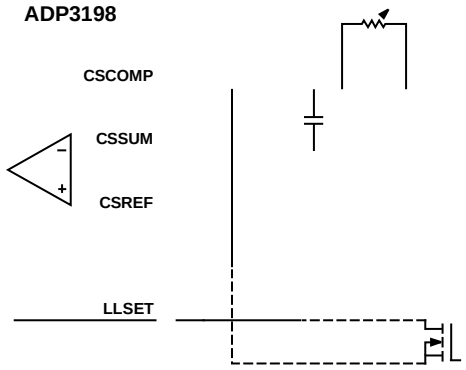
It is best to have a dual location for C_{CS} in the layout so that standard values can be used in parallel to get as close to the desired value. For best accuracy, C_{CS} should be a 5% or 10% NPO capacitor. This example uses a 5% combination for C_{CS} of two 1 nF capacitors in parallel. Recalculating R_{CS} and $R_{PH(X)}$ using this capacitor combination yields 114 kΩ and 160 kΩ. The closest standard 1% value for $R_{PH(X)}$ is 158 kΩ.

INDUCTOR DCR TEMPERATURE CORRECTION

When the inductor DCR is used as the sense element and

Load Line Setting

For load line values greater than 1 mΩ, R_{CSA} can be set equal to R_O, and the LLSET pin can be directly connected to the CSCOMP pin. When the load line value needs to be less than 1 mΩ, two additional resistors are required. Figure 12 shows the placement of these resistors.



POWER MOSFETS

For this example, the N-channel power MOSFETs have been selected for one high-side switch and two low-side switches per phase. The main selection parameters for the power MOSFETs are $V_{GS(TH)}$, Q_G, C_{ISS}, C_{RSS}, and $R_{DS(ON)}$. The minimum gate drive voltage (the supply voltage to the ADP3110A) dictates whether standard threshold or logic-level threshold MOSFETs must be used. With V_{GATE} ~10 V, logic-level threshold MOSFETs ($V_{GS(TH)}$ < 2.5 V) are recommended.

The maximum output current (I_O) determines the $R_{DS(ON)}$ requirement for the low-side (synchronous) MOSFETs. With the ADP3198, currents are balanced between phases, thus, the current in each low-side MOSFET is the output current divided by the total number of MOSFETs (n_{SF}). With conduction losses being dominant, Equation 24 shows the total power that is dissipated in each synchronous MOSFET in terms of the ripple current per phase (I_R) and average total output current (I_O):

$$P_{\blacksquare F} = (1-D) \times \left(\frac{I_O}{\blacksquare F} \right)^2 + \frac{1}{12} \times \left(\frac{I_R}{\blacksquare F} \right)^2 \times R_{D\blacksquare(\blacksquare F)} \qquad (24)$$

Knowing the maximum output current being designed for and the maximum allowed power dissipation, the user can find the required $R_{DS(ON)}$ for the MOSFET. For D-PAK MOSFETs up to an ambient temperature of 50°C, a safe limit for P_{SF} is 1 W to

RAMP RESISTOR SELECTION

The ramp resistor (R_R) is used for setting the size of the internal PWM ramp. The value of this resistor is chosen to provide the best combination of thermal balance, stability, and transient response. Equation 28 is used for determining the optimum value.

$$R_R = \frac{A_R \times L}{3 \times A_D \times R_{D,} \times C_R} \quad (28)$$

$$R_R = \frac{0.2 \times 320\ \text{nH}}{3 \times 5 \times 2.4\ \text{m}\Omega \times 5\ \text{pF}} = 356\ \text{k}\Omega$$

where:

A_R is the internal ramp amplifier gain.
A_D is the current balancing amplifier gain.
$R_{D,}$ is the total low-side MOSFET on resistance.
C_R is the internal ramp capacitor value.

The internal ramp voltage magnitude can be calculated by using

$$_R = \frac{A_R \times (1-D) \times \ _{ID}}{R_R \times C_R \times \ _,} \quad (29)$$

$$_R = \frac{0.2 \times (1-0.108) \times 1.3\ \text{V}}{357\ \text{k}\Omega \times 5\ \text{pF} \times 330\ \text{kHz}} = 394\ \text{mV}$$

The size of the internal ramp can be made larger or smaller.

Because of the multimode feedback structure of the ADP3198, the feedback compensation must be set to make the converter output impedance work in parallel with the output decoupling to make the load look entirely resistive. Compensation is needed for several poles and zeros created by the output inductor and the decoupling capacitors (output filter).

A type-three compensator on the voltage feedback is adequate for proper compensation of the output filter. Equation 35 to Equation 39 are intended to yield an optimal starting point for the design; some adjustments may be necessary to account for PCB and component parasitic effects (see the Tuning the ADP3198 section).

First, compute the time constants for all the poles and zeros in the system using Equation 35 to Equation 39.

$$R_E = \times R_O + A_D \times R_{D,} + \frac{R_L \times}{ID} + \frac{2 \times L \times (1 - \times D) \times}{\times C \times R_O \times ID}$$

$$R_E = 4 \times 1\,\text{m}\Omega + 5 \times 2.4\,\text{m}\Omega + \frac{1.4\,\text{m}\Omega \times 0.51\,\text{V}}{1.3\,\text{V}} + \frac{2 \times 320\,\text{nH} \times (1 - 0.432) \times 0.51\,\text{V}}{4 \times 5.6\,\text{mF} \times 1\,\text{m}\Omega \times 1.3\,\text{V}} = 22.9\,\text{m}\Omega \quad (35)$$

$$A = C \times (R_O - R') + \frac{L}{R_O} \times \frac{R_O - R'}{R} = 5.6\,\text{mF} \times (1\,\text{m}\Omega - 0.5\,\text{m}\Omega) + \frac{240\,\text{pH}}{1\,\text{m}\Omega} \times \frac{1\,\text{m}\Omega - 0.5\,\text{m}\Omega}{0.6\,\text{m}\Omega} = 3.00\,\mu\text{s} \quad (36)$$

$$B = (R + R' - R_O) \times C = (0.6\,\text{m}\Omega + 0.5\,\text{m}\Omega - 1\,\text{m}\Omega) \times 5.6\,\text{mF} = 560\,\text{ns} \quad (37)$$

$$C = \frac{R \times L - \frac{A_D \times R_{D,}}{2 \times}}{ID \times R_E} = \frac{0.51\,\text{V} \times 320\,\text{nH} - \frac{5 \times 2.4\,\text{m}\Omega}{2 \times 330\,\text{kHz}}}{1.3\,\text{V} \times 22.9\,\text{m}\Omega} = 5.17\,\mu\text{s} \quad (38)$$

$$D = \frac{C \times C \times R_O^2}{C \times (R_O - R') + C \times R_O} = \frac{5.6\,\text{mF} \times 180\,\mu\text{F} \times (1\,\text{m}\Omega)^2}{5.6\,\text{mF} \times (1\,\text{m}\Omega - 0.5\,\text{m}\Omega) + 180\,\mu\text{F} \times 1\,\text{m}\Omega} = 338\,\text{ns} \quad (39)$$

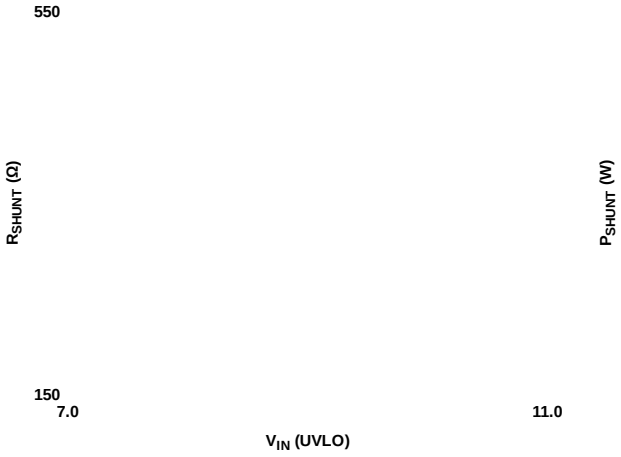
where:

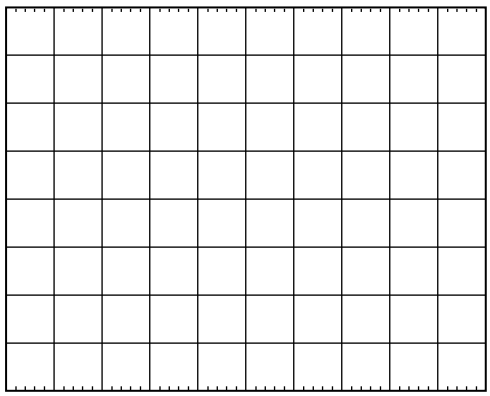
R' is the PCB resistance from the bulk capacitors to the ceramics.
$R_{D,}$ is the total low-side MOSFET on resistance per phase.
In this example, A_D

Figure 13 and Figure 14 show the typical transient response using these compensation values.

SHUNT RESISTOR DESIGN

The ADP3198 uses a shunt to generate 5 V from the 12 V supply range. A trade-off can be made between the power dissipated in the shunt resistor and the UVLO threshold. Figure 16 shows the typical resistor value needed to realize certain UVLO voltages. It also gives the maximum power dissipated in the shunt resistor for these UVLO voltages.





General Recommendations

For good results, a PCB with at least four layers is recommended. This provides the needed versatility for control circuitry interconnections with optimal placement, power planes for ground, input and output power, and wide interconnection traces in the remainder of the power delivery current paths. Keep in mind that each square unit of 1 ounce copper trace has a resistance of ~0.53 mΩ at room temperature.

Whenever high currents must be routed between PCB layers, use vias liberally to create several parallel current paths, so the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.

If critical signal lines (including the output voltage sense lines of the ADP3198) must cross through power circuitry, it is best to interpose a signal ground plane between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of making signal ground a bit noisier.

An analog ground plane should be used around and under the ADP3198 as a reference for the components associated with the controller. This plane should be tied to the nearest output decoupling capacitor ground and should not be tied to any other power circuitry to prevent power currents from flowing into it.

The components around the ADP3198 should be located close to the controller with short traces. The most important traces to keep short and away from other traces are the FB pin and CSSUM pin. The output capacitors should be connected as close as possible to the load (or connector), for example, a microprocessor core, that receives the power. If the load is distributed, the