ADP3207C

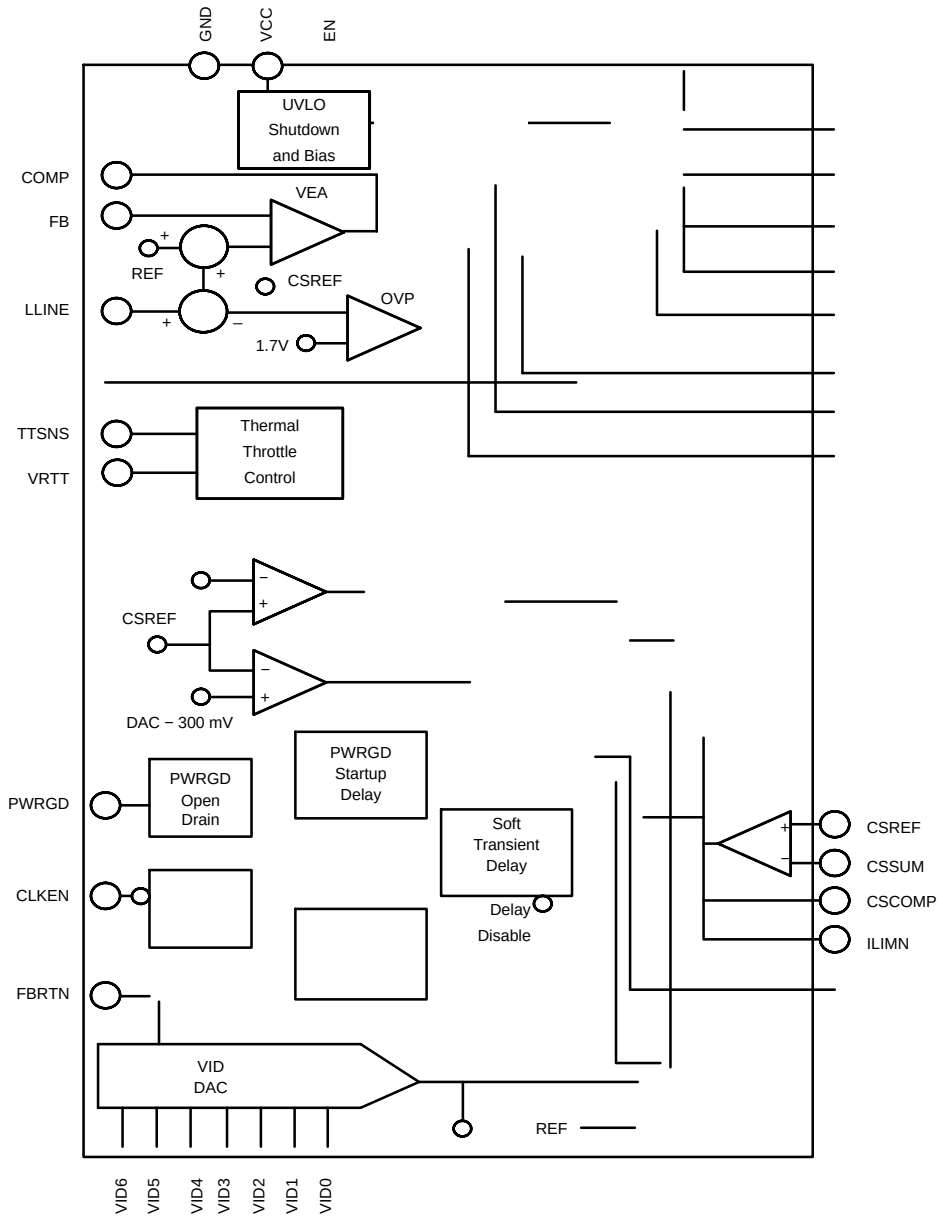
7-Bit Programmable, Multi-Phase Mobile, CPU Synchronous Buck Controller

The ADP3207C is a high efficiency, multi−phase, synchronous, buck−switching regulator controller optimized for converting notebook battery voltage into the core supply voltage required by high performance Intel processors. The part uses an internal 7−bit Digital−to−Analog Converter (DAC) to read Voltage Identification (VID) code directly from the processor that sets the output voltage. The phase relationship of the output signals can be programmed to provide 1−, 2−, or 3 −

LFCSP40
CASE 932AC

−See detailed ordering andshipping information in the package dimensions section on page 31 of this data sheet.

December, 2009 − Rev. 0
Publication Order Number:
ADP3207C/D


GND
VCC
EN
UVLO
Shutdown
and Bias
COMP
VEA
FB
REF
CSREF
LLINE
OVP
1.7V
TTSNS
VRTT
Thermal
Throttle
Control
CSREF
DAC − 300 mV
PWRGD
PWRGD
Open
Drain
PWRGD
Startup
Delay
Soft
Transient
Delay
Delay
Disable
CLKEN
FBRTN
VID
DAC
REF
CSREF
CSSUM
CSCOMP
ILIMN
VID6
VID5
VID4
VID3
VID2
VID1
VID0

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
V_{CC}	−0.3 to +6.0	V
FBRTN	−0.3 to +0.3	V
SW1 to SW3 DC t < 200 ns	 −5 to +22 −10 to +28	V
RAMPADJ (In Shutdown)	−0.3 to +22	V
All Other Inputs and Outputs	−0.3 to V_{CC} + 0.3	V
Storage Temperature Range	−65 to +150	°C
Operating Ambient Temperature Range	−10 to 100	°C
Operating Junction Temperature	125	°C
Thermal Impedance (θ_{JA})	98	°C/W
Lead Temperature Soldering (10 sec) Infrared (15 sec)	 300 260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

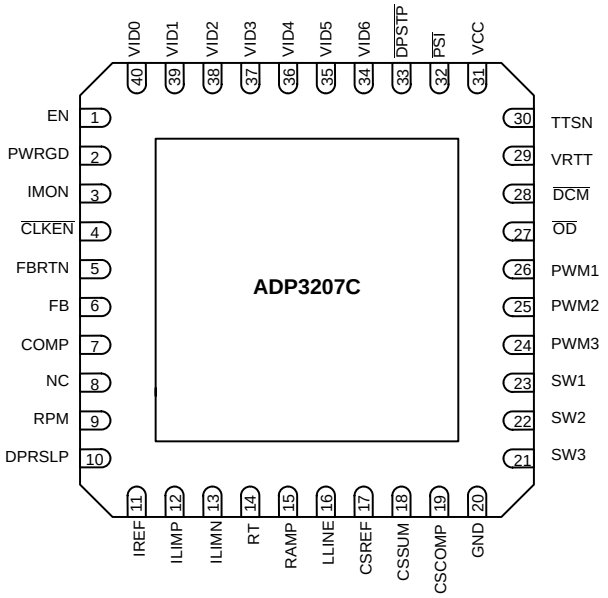


Figure 2. Pin Configuration
(Top View)

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0 V, FBRTN = GND, EN = V_{CC}, V_{VID} = 0.50 V to 1.5000 V, $\overline{PSI}$ = 1.05 V, DPRSLP = GND, $\overline{DPRSTP}$= 1.05 V, LLSET = CSREF, T_A = −10°C to 100°C, unless otherwise noted (Note 1). R_{REF} = 80 kΩ. Current entering a pin (sunk by the device) has a positive sign.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VOLTAGE MONITORING AND PROTECTION − Power Good						
CSREF Reverse Voltage Threshold	$V_{RVCSREF}$	Relative to FBRTN, Latchoff mode: CSREF Falling CSREF Rising	−350	 −300 −70	 −5.0	mV
PWRGD Low Voltage	V_{PWRGD}	$I_{PWRGD(SINK)}$ = 4 mA		85	150	mV
PWRGD High, Leakage Current	I_{PWRGD}	V_{PWRDG} = 5.0 V			1.0	μA
PWRGD Startup Delay	$T_{SSPWRGD}$	Measured from CLKEN neg edge to PWRGD Pos Edge		8.0		ms
PWRGD Latchoff Delay	$T_{LOFFPWRGD}$	Measured from Out−off−Good−Window event to Latchoff (switching stops)		8.0		ms
PWRGD Propagation Delay	$T_{PDPWRGD}$	Measured from Out−off−Good−Window event to PWRGD neg edge		200		ns
Crowbar Latchoff Delay (Note 2)	T_{LOFFCB}	Measured from Crowbar event to Latchoff (switching stops)		200		ns
PWRGD Masking Time		Triggered by any VID change or OCP event				

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0 V, FBRTN = GND, EN = V_{CC}, V_{VID} = 0.50 V to 1.5000 V, $\overline{PSI}$ = 1.05 V, DPRSLP = GND, $\overline{DPRSTP}$= 1.05 V, LLSET = CSREF, T_A = −10°C to 100°C, unless otherwise noted (Note 1). R_{REF} = 80 kΩ. Current entering a pin (sunk by the device) has a positive sign.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DPRSLP						
Input Voltage		Refers to driving signal level Logic low, I_{sink} ≤ 1 μA Logic high, I_{source} −5 μA	 2.3		 0.4	V
Input Current		DPRSLP = low DPRSLP = high		−1.0 +2.0		μA
$\overline{DPRSTP}$						
Input Voltage (Note 2)		Refers to driving signal level Logic low, I_{sink} ≤ 1 μA Logic high, I_{source} −5 μA	 0.7		 0.3	V
Input Current (Note 2)						

TEST CIRCUITS

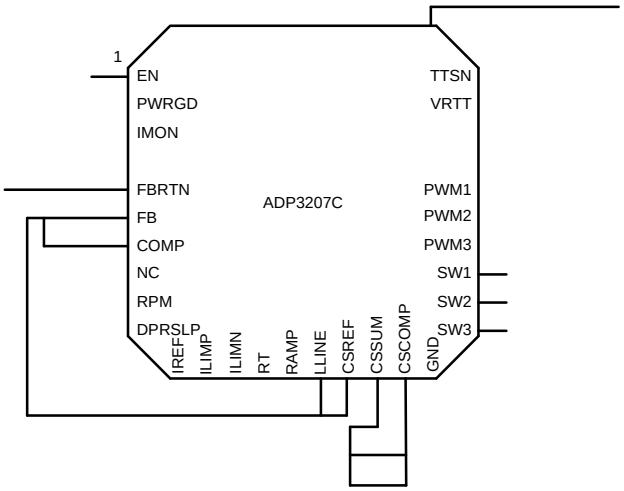


Figure 3. Closed−Loop Output Voltage Accuracy

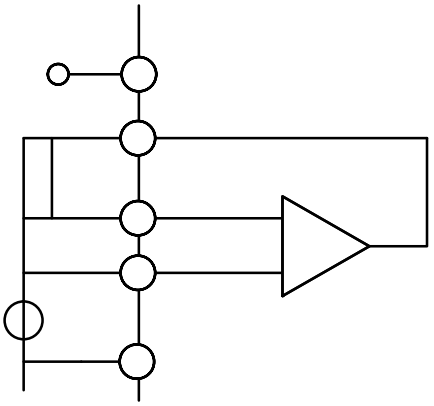
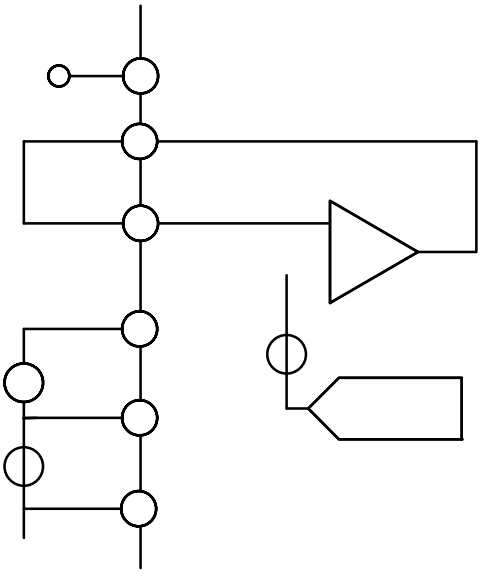


Figure 4. Current Sense Amplifier V_{OS}



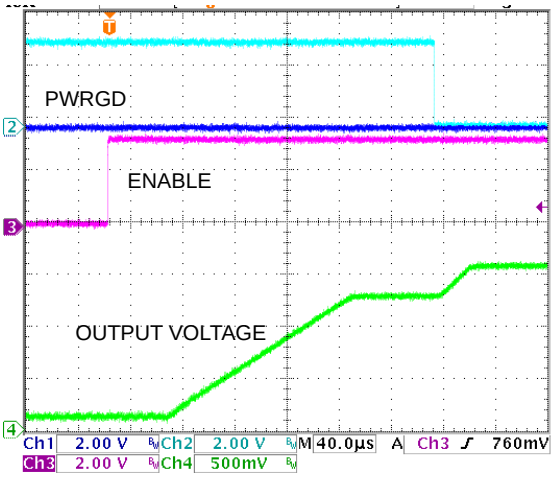


Figure 6. ADP3207CF Startup

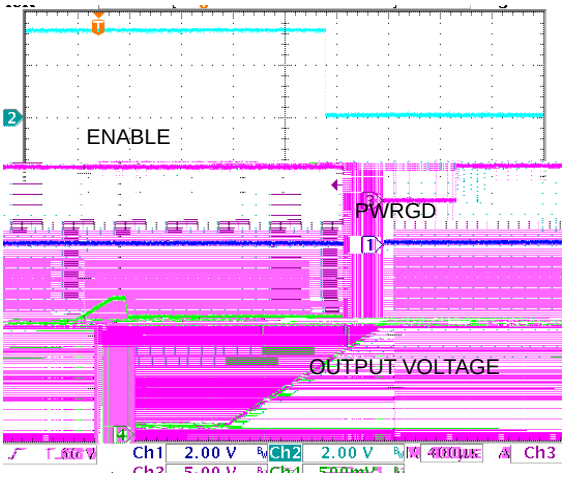


Figure 7. ADP3207C Startup

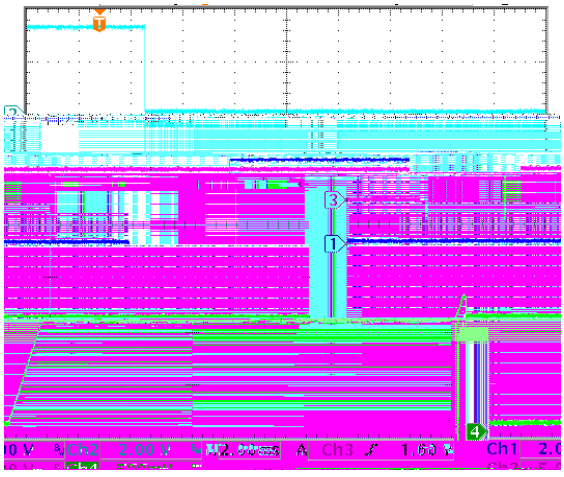


Figure 8. ADP3207C Startup

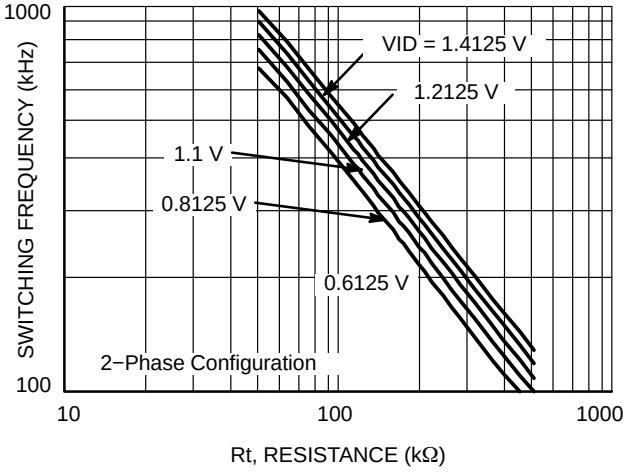


Figure 9. Per Phase Switching Frequency vs. RT Resistance

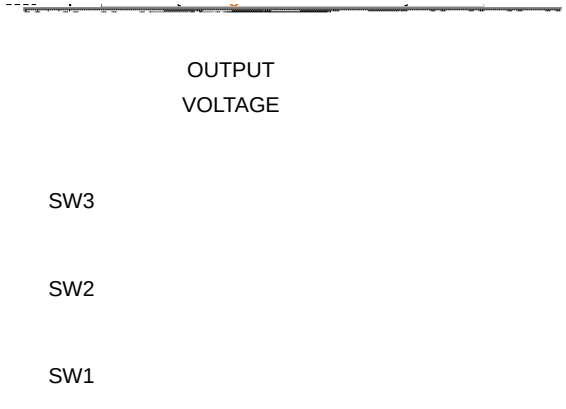


Figure 10. Load Transient

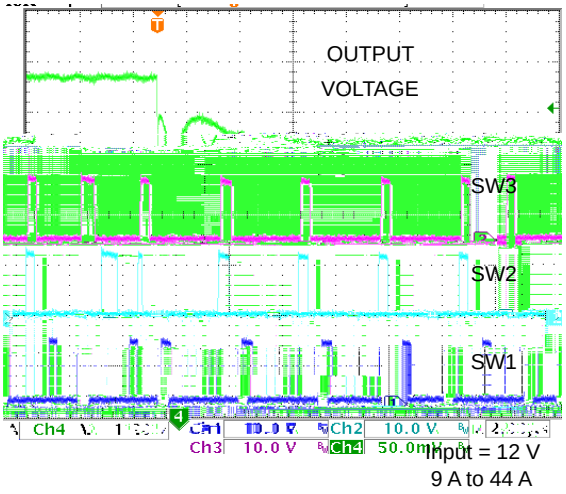
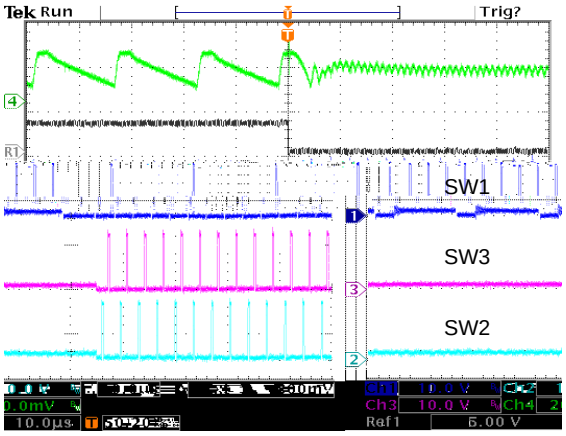


Figure 11. Load Transient


Tek Run
Trig?
SW1
SW3
SW2
Ch1 10.0 V
Ch3 10.0 V
Ch4
Ref1 5.00 V
10.0µs

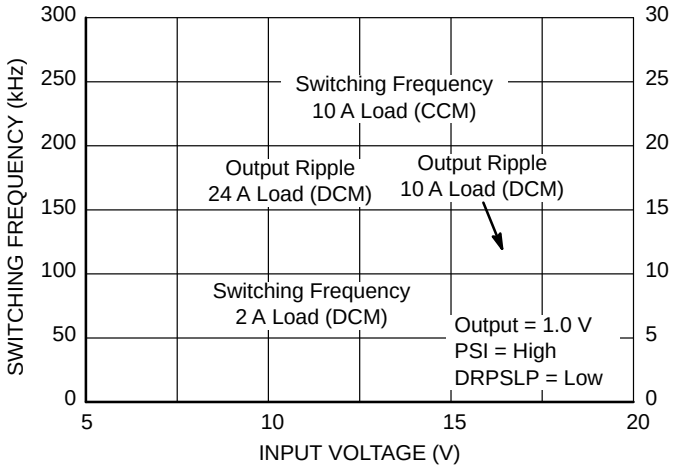


Figure 22. Switching Frequency and Output Ripple in RPM

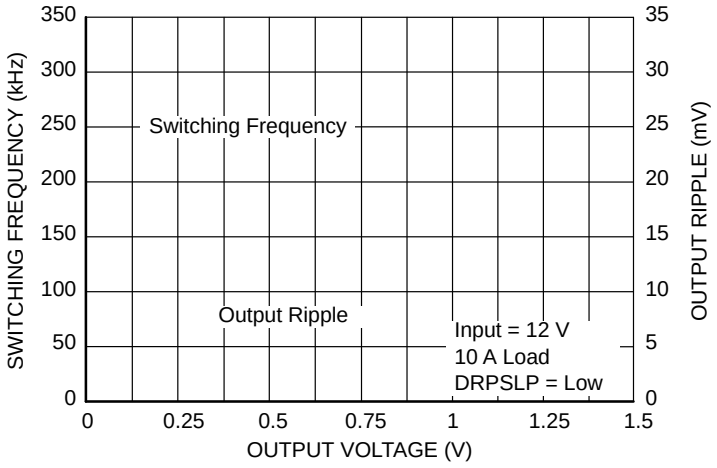


Figure 23. Switching Frequency and Output Ripple in RPM

Theory of Operation

The ADP3207C combines a multi−mode Ramp Pulse Modulated (PWM/RPM) control with multi−

Table 1. Phase Number and Operation Modes

$\overline{\text{PSI}}$	DPRSLP	VID Transient Period (Note 1)	Hit Current Limit	No. of Phases Selected by User	No. of Phases in Operation	Operation Mode
DNC	DNC	Yes	DNC	N 3, 2, or 1	N	PWM, CCM Only
1	0	No	DNC	N 3, 2, or 1	N	PWM, CCM Only
0	0	No	No	DNC	Phase 1 only	RPM, CCM Only
0	0	No	Yes	DNC	N	PWM, CCM Only
DNC	1	No	No	DNC	Phase 1 only	RPM, Automatic CCM / DCM
DNC	1	No	Yes	DNC	N	PWM, CCM Only

1. VID transient period is the time following any VID change, including entrance and exit of deeper sleep mode. The duration of VID transient period is the same as that of PWRGD masking time.
2. DNC = Do Not Care.
3. CCM = Continuous Conduction Mode.
4. DCM = Discontinuous Conduction Mode.

Switch Frequency Setting

Master Clock Frequency for PWM Mode

The clock frequency of the ADP3207C is set by an external resistor connected from the RT pin to ground. The frequency varies with the VID voltage; the lower the VID voltage, the lower the clock frequency. The variation of clock frequency with VID voltage makes VCore ripple remain constant and improves power conversion efficiency at a lower VID voltage.

To determine the switching frequency per phase, the clock is divided by the number of phases in use. If PWM3 is pulled up to V_{CC}, then the master clock is divided by 2 for the frequency of the r Ifr2374 Twfr2374 Twfr23744 Tm2r.2(4 I) nlledW

then given as the voltage difference of CSREF − LLSET. The configuration in the previous paragraph makes it possible for the load line slope to be set independent of the current limit threshold. In the event that the current limit threshold and load line do not have to be independent, the resistor divider between CSREF and CSCOMP can be omitted and the CSCOMP pin can be connected directly to LLSET. To disable voltage positioning entirely (that is, to set no load line), tie LLSET to CSREF.

To provide the best accuracy for current sensing, the CSA is designed to have a low offset input voltage. In addition, the sensing gain is set by an external resistor ratio.

Active Impedance Control Mode

To control the dynamic output voltage droop as a function of the output current, the signal proportional to the total output current is converted to a voltage that appears between CSREF and LLINE. This voltage can be scaled to equal the droop voltage, which is calculated by multiplying the droop impedance of the regulator with the output current. The droop voltage is then used as the control voltage of the PWM regulator. The droop voltage is subtracted from the DAC reference output voltage and determines the voltage positioning setpoint. The setup results in an enhanced feed forward response.

Current Control Mode and Thermal Balance

The ADP3207C has individual inputs for monitoring the current in each phase. The phase current information is combined with an internal ramp to create a current balancing feedback system that is optimized for initial current accuracy and dynamic thermal balance. The current balance information is independent of the total inductor current information used for voltage positioning described in the Active Impedance Control Mode section.

The magnitude of the internal ramp can be set so the transient response of the system becomes optimal. The ADP3207C also monitors the supply voltage to achieve feed−forward control whenever the supply voltage changes. A resistor connected from the power input voltage rail to the RAMP pin determines the slope of the internal PWM ramp. Detailed information about programming the ramp is given in the Ramp Resistor Selection section.

External resistors are in series with the SW1 pin, SW2 pin, and the SW3 pin to create an intentional current imbalance. Such a condition can exist when one phase has better cooling and supports higher currents than the other phase. Resistor RSW2 and Resistor RSW3 (see the Typical Application Circuit in Figure 28) can be used to adjust thermal balance. It is recommended to add these resistors during the initial design to make sure placeholders are provided in the layout.

To increase the current in any given phase, users should make RSW for that phase larger (that is, make RSW = 1.5 kΩ for the hottest phase and do not change it during balance optimization). Increasing RSW to 1.5 kΩ makes a substantial increase in phase current. Increase each RSW value by small amounts to achieve thermal balance starting with the coolest phase.

If adjusting current balance between phases is not needed, RSW should be 1 kΩ for all phases.

Voltage Control Mode

A high gain bandwidth error amplifier is used for the voltage−mode control loop. The non−inverting input voltage is set via the 7−bit VID DAC. The VID codes are listed in Table 3. The non−inverting input voltage is offset by the droop voltage as a function of current, commonly known as active voltage positioning. The output of the error amplifier is the COMP pin, which sets the termination voltage for the internal PWM ramps.

The negative input, FB, is tied to the output sense location through a resistor, RB, for sensing and controlling the output voltage at the remote sense point. The main loop compensation is incorporated in the feedback network connected between FB and COMP.

Enhanced PWM Mode

Enhanced PWM mode is intended to improve the transient response to a load step up. In traditional PWM controllers, when a load step up occurred, the controller had to wait until the next turn on of the PWM signal to respond to the load change. Enhanced PWM mode allows the controller to respond immediately when a load step up occurs. This allows the phases to respond when the load increase transition takes place. EWPM is disabled in RPM operation.

Power−Good Monitoring

The power−good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open drain output that can be pulled up through an external resistor to a voltage rail that is not necessarily the same V_{CC} voltage rail of the controller. Logic high level indicates that the output voltage is within the voltage limits defined by a window around the VID voltage setting. PWRGD goes low when the output voltage is outside of that window.

Following the IMVP−6 specification, the PWRGD window is defined as −300 mV below and +200 mV above the actual VID DAC output voltage. For any DAC voltage below 300 mV, only the upper limit of the PWRGD window is monitored. To prevent false alarm, the power−good circuit is masked during various system transitions, including any VID change and entrance/exit out of deeper sleep. The duration of the PWRGD mask is set by an internal timer to be about 100 μs. In conditions where a larger than 200 mV voltage drop occurs during deeper sleep entry or slow deeper sleep exit, the duration of PWRGD masking is extended by an internal logic circuit.

Powerup Sequence and Soft−Start

The power−on, ramp−up time of the output voltage is set internally. The reference voltage of the voltage error amplifier is connected to an internal DAC. This DAC converts the VID

code to an analog reference voltage. During startup, the DAC ignores the VID code. The internal DAC steps through each VID code from 0 V to the boot voltage. The DAC steps to the next VID code every 16 μs. With 12.5 mV difference between VID codes, the soft−

Current Monitor Output

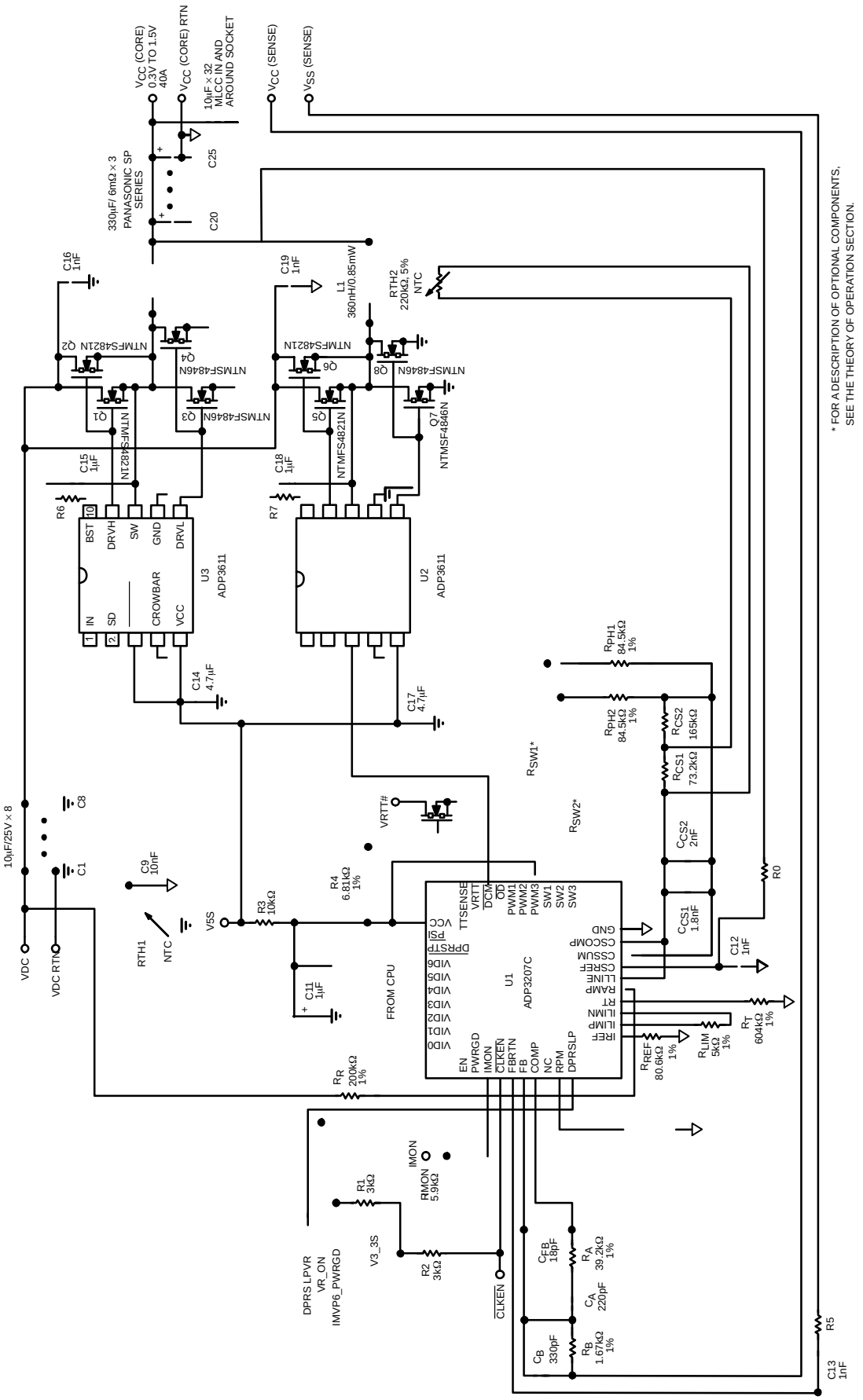
The ADP3207C has an output current monitor. The I_{MON} pin sources a current proportional to the inductor current. A resistor from I_{MON} pin to FBRTN sets the gain. A 0.1 μF is added in parallel with R_{MON} to filter the inductor ripple. The I_{MON} pin is clamped to prevent it from going above 1.15 V

Table 3. VID Code Table

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output (V)
0	0	0	0	0	0	0	1.5000
0	0	0	0	0	0	1	1.4875
0	0	0	0	0	1	0	1.4750
0	0	0	0	0	1	1	1.4625
0							

Table 3. VID Code Table

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output (V)
1	0	1	1	0	1	1	0.3625
1	0	1	1	1	0	0	0.3500
1	0	1	1	1	0	1	0.3375
1	0	1	1	1	1	0	0.3250
1	0	1	1	1	1	1	0.3125
1	1	0	0	0	0	0	0.3000
1	1	0	0	0	0	1	0.2875
1	1	0	0	0	1	0	0.2750
1	1	0	0	0	1	1	0.2625
1	1	0	0	1	0	0	0.2500
1	1	0	0	1	0	1	0.2375
1	1	0	0	1	1	0	0.2250
1	1	0	0	1	1	1	0.2125
1	1	0	1	0	0	0	0.2000
1	1	0	1	0	0	1	0.1875
1	1	0	1	0	1	0	0.1750
1	1	0	1	0	1	1	0.1625
1	1	0	1	1	0	0	0.1500
1	1	0	1	1	0	1	0.1375
1	1	0	1	1	1	0	0.1250
1	1	0	1	1	1	1	0.1125
1	1	1	0	0	0	0	0.1000
1	1	1	0	0	0	1	0.0875
1	1	1	0	0	1	0	0.0750
1	1	1	0	0	1	1	0.0625
1	1	1	0	1	0	0	0.0500
1	1	1	0	1	0	1	0.0375
1	1	1	0	1	1	0	0.0250
1	1	1	0	1	1	1	0.0125
1	1	1	1	0	0	0	0.0000
1	1	1	1	0	0	1	0.0000
1	1	1	1	0	1	0	0.0000
1	1	1	1	0	1	1	0.0000
1	1	1	1	1	0	0	0.0000
1	1	1	1	1	0	1	0.0000
1	1	1	1	1	1	0	0.0000
1	1	1	1	1	1	1	0.0000


VCC (CORE) 0.3V TO 1.5V 40A
VCC (CORE) RTN
10μF × 32 MLCC IN AND AROUND SOCKET
VCC (SENSE)
VSS (SENSE)
330μF/ 6mΩ × 3 PANASONIC SP SERIES
C25
C20
C16 1nF
C19 1nF
L1 360nH/0.85mW
RTH2 220kΩ, 5% NTC
NTMFS4821N Q2
NTMSF4846N Q4
NTMFS4821N Q6
NTMSF4846N Q8
NTMSF4846N Q1
NTMSF4846N Q3
NTMFS4821N Q5
NTMSF4846N Q7
C15 1μF
C18 1μF
R6
R7
BST
DRVH
SW
GND
DRVL
IN
SD
CROWBAR
VCC
U3 ADP3611
U2 ADP3611
C14 4.7μF
C17 4.7μF
10μF/25V × 8
C8
C1
VDC
VDC RTN
C9 10nF
RTH1 NTC
V5S
R3 10kΩ
R4 6.81kΩ 1%
VRTT#
RSW1*
RSW2*
RPH1 84.5kΩ 1%
RPH2 84.5kΩ 1%
RCS2 165kΩ
RCS1 73.2kΩ
CCS2 2nF
CCS1 1.8nF
R0
C12 1nF
C11 1μF
FROM CPU
U1 ADP3207C
VCC
PSI
DPRSTP
VID6
VID5
VID4
VID3
VID2
VID1
VID0
EN
PWRGD
IMON
CLKEN
FBRTN
FB
COMP
NC
RPM
DPRSLP
TTSENSE
VRTT
DCM
OD
PWM1
PWM2
PWM3
SW1
SW2
SW3
GND
CSCOMP
CSSUM
CSREF
CLINE
RAMP
RT
ILIMN
ILIMP
REF
RR 200kΩ 1%
RREF 80.6kΩ 1%
RLIM 5kΩ 1%
RT 604kΩ 1%
R1 3kΩ
IMON
RIMON 5.9kΩ
V3_3S
R2 3kΩ
DPRS LPVR
VR_ON
IMVP6_PWRGD
CEB 18pF
RA 39.2kΩ 1%
CA 220pF
CB 330pF
RB 1.67kΩ 1%
CLKEN
R5
C13 1nF
* FOR A DESCRIPTION OF OPTIONAL COMPONENTS, SEE THE THEORY OF OPERATION SECTION.

C_{OUT} Selection

The required output decoupling for processors and platforms is typically recommended by Intel. The following

Knowing the maximum output thermal current and the maximum allowed power dissipation, users can find the required $R_{DS(on)}$ for the MOSFET. For 8−lead SOIC or 8−lead SOIC−compatible packaged MOSFETs the junction to ambient (PCB) thermal impedance is 50°C/W. In the worst case, the PCB temperature is 90°C during heavy load operation of the notebook; a safe limit for P_{SF} is 0.6 W at 120°C junction temperature. Therefore, for this example (32 A maximum thermal current), $R_{DS(SF)}$ (per MOSFET) is less than 9.6 mΩ for two pieces of low−side MOSFET. This $R_{DS(SF)}$ is also at a junction temperature of about 120°C; therefore, the $R_{DS(SF)}$ (per MOSFET) should be lower than 6.8 mΩ at room temperature, giving 9.6 mΩ at high temperature.

Another important factor for the synchronous MOSFET is the input capacitance and feedback capacitance. The ratio of feedback to input needs to be small (less than 10% is recommended) to prevent accidental turn−on of the synchronous MOSFETs when the switch node goes high.

The high−side (main) MOSFET has to be able to handle two main power dissipation components, conduction and

ramp size that gives an optimal balance for good stability, transient response, and thermal balance.

COMP Pin Ramp

There is a ramp signal on the COMP pin due to the droop voltage and output voltage ramps. This ramp amplitude adds to the internal ramp to produce the following overall ramp signal at the PWM input:

$$V_{RT} = \frac{V_R}{\sqrt{1 - \frac{2\times(1-n\times D)}{n\times f_{SW}\times C_X\times R_O}}} \quad \text{(eq. 21)}$$

For this example, the overall ramp signal is found to be 2.2 V.

Setting the Switching Frequency for RPM Mode Operation of Phase.

During the RPM mode operation of Phase 1, the ADP3207C runs in pseudo constant frequency, given that the load current is high enough for continuous current mode. While in discontinuous current mode, the switching frequency is reduced with the load current in a linear manner. When considering power conversion efficiency in light load, lower switching frequency is usually preferred for RPM mode. However, the VCore ripple specification in the IMVP−6 sets the limitation for lowest switching frequency. Therefore, depending on the inductor and output capacitors, the switching frequency in RPM mode can be equal, larger, or smaller than its counterpart in PWM mode.

A resistor from RPM to GND sets the pseudo constant frequency as following:

$$R_{RPM} = \frac{2 \times R_T}{V_{VID} + 1.0\ V} \times \frac{A_R \times (1 - D) \times V_{VID}}{R_R \times C_R \times f_{SW}} - 0.5\ k\Omega \quad \text{(eq. 22)}$$

Where:
A_R is the internal ramp amplifier gain.
C_R is the internal ramp capacitor value.
R_R is an external resistor on the RAMPADJ pin to set the internal ramp magnitude.

Because R_R = 280 kΩ, the following resistance sets up 300 kHz switching frequency in RPM operation:

$$R_{RPM} = \frac{2 \times 280\ k\Omega}{1.150\ V + 1.0\ V} \times \frac{0.5 \times (1 - 0.061) \times 1.150}{462\ k\Omega \times 5\ pF \times 300\ kHz} - 5\ \Omega = 202\ k\Omega \quad \text{(eq. 23)}$$

Output Current Monitor

The ADP3207C has output current monitor. The I_{MON} pin sources a current proportional to the total inductor current. A resistor, R_{MON}, from I_{MON} to FBRTN sets the gain of the output current monitor. A 0.1 μF is placed in parallel with R_{MON} to filter the inductor current ripple and high frequency load transients. Since the I_{MON} pin is connected directly to the CPU, it is clamped to prevent it from going above 1.15 V.

The I_{MON} pin current is equal to the R_{LIM} times a fixed gain of 10. R_{MON} can be found using the following equation:

$$R_{MON} = \frac{1.15\ V \times R_{LIM}}{10 \times R_O \times I_{FS}} \quad \text{(eq. 24)}$$

Where:
R_{MON} is the current monitor resistor. R_{MON} is connected from I_{MON} pin to FBRTN.
R_{LIM} is the current limit resistor.
R_O is the output load line resistance.
I_{FS} is the output current when the voltage on I_{MON} is at full scale.

Current Limit Setpoint

To select the current limit setpoint, we need to find the resistor value for R_{LIM}. The current limit threshold for the ADP3207C is set when the current in R_{LIM} is equal to the internal reference current of 20 μA. The current in R_{LIM} is equal to the inductor current times R_O. R_{LIM} can be found using the following equation:

$$R_{LIM} = \frac{I_{LIM} \times R_O}{20\ \mu A} \quad \text{(eq. 25)}$$

Where:
R_{LIM} is the current limit resistor. R_{LIM} is connected from the I_{LIM} pin to ground.
R_O is the output load line resistance.
I_{LIM} is the current limit set point. This is the peak inductor current that will trip current limit.

In this example, if choosing 55 A for I_{LIM}, R_{LIM} is 5.775 kΩ, which is close to a standard 1% resistance of 5.76 kΩ.

The per phase current limit described earlier has its limit determined by the following:

$$I_{PHLIM} \cong \frac{V_{COMP(MAX)} - V_R - V_{BIAS}}{A_D \times R_{DS(MAX)}} + \frac{I_R}{2} \quad \text{(eq. 26)}$$

For the ADP3207C, the maximum COMP voltage ($V_{COMP(MAX)}$) is 3.3 V, the COMP pin bias voltage (V_{BIAS}) is 1.0 V, and the current balancing amplifier gain (A_D) is 5. Using a V_R of 0.55 V, and a $R_{DS(MAX)}$ of 3.8 mΩ (low−side on−resistance at 150°C) results in a per phase limit of 85 A. Although this number seems high, this current level can only be reached with a absolute short at the output and the current limit latchoff function shutting down the regulator before overheating occurs.

This limit can be adjusted by changing the ramp voltage V_R. However, users should not set the per phase limit lower than the average per phase current (I_{LIM}/n).

There is also a per phase initial duty−cycle limit at maximum input voltage:

$$D_{LIM} = D_{MIN} \times \frac{V_{COMP(MAX)} - V_{BIAS}}{V_R} \quad \text{(eq. 27)}$$

For this example, the duty−cycle limit at maximum input voltage is found to be 0.25 when D is 0.061.

Feedback Loop Compensation Design

Optimized compensation of the ADP3207C allows the best possible response of the regulator's output to a load change. The basis for determining the optimum compensation is to make the regulator and output decoupling appear as an output

Selecting Thermal Monitor Components

For single−point hot spot thermal monitoring, simply set R_{TTSET1} equal to the NTC thermistor's resistance at the

15. Users should see a waveform that is similar to the one in Figure 33. Use the horizontal cursors to measure V_{ACDRP} and V_{DCDRP} as shown. Do not measure the undershoot or overshoot that occurs immediately after the step.
16. If the V_{ACDRP} and V_{DCDRP} are different by more than a couple of mV, use the following to adjust C_{CS}. (Note that users may need to parallel different values to get the right one due to the limited standard capacitor values available. It is also wise to have locations for two capacitors in the layout for this.)

$$C_{CS(NEW)} = C_{CS(OLD)} \times \frac{V_{ACDRP}}{V_{DCDRP}} \quad \text{(eq. 44)}$$

17. Repeat Step 15 and Step 16. Repeat adjustments if necessary. Once completed, do not change C_{CS} for the rest of the procedure.
18. Set dynamic load step to maximum step size. Do not use a step size larger than needed. Verify that the output waveform is square, which means V_{ACDRP} and V_{DCDRP} are equal. Note: Make sure that the load step slew rate and turn−on are set for a slew rate of ~150 A/μs to 250 A/μs (for example, a load step of 50 A should take 200 ns to 300 ns) with no overshoot. Some dynamic loads have an excessive turn−on overshoot if a minimum current is not set properly (this is an issue if using a V_{TT}

The best location for the ADP3207C is close to the CPU corner where all the related signal pins are located: VID0 to VID6, $\overline{PSI}$, V_{CC}SENSE, and V_{SS}SENSE. The components around the ADP3207C should be located close to the controller with short traces. The most important traces to keep short and away from other traces are the FB and CSSUM pins (refer to Figure 28 for more details on layout for the CSSUM node.) The MLCC for the V_{CC} decoupling should be placed as close to the V_{CC} pin as possible. In addition, the noise filtering capacitor on the TTSENSE pin should also be as close to that pin as possible.

The output capacitors should be connected as closely as possible to the load (or connector) that receives the power (for example, a microprocessor core). If the load is distributed, then the capacitors should also be distributed, and generally in proportion to where the load tends to be more dynamic.

Power Circuitry

Avoid crossing any signal lines over the switching power path loop. This path should be routed on the PCB to encompass the shortest possible length to minimize radiated switching noise energy (that is, EMI) and conduction losses in the board. Failure to take proper precautions often results in EMI problems for the entire PC system as well as noise−related operational problems in the power converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors and the power MOSFETs, including all interconnecting PCB traces and planes. The use of short and wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which can cause high energy ringing, and it accommodates the high current demand with minimal voltage loss.

Whenever a power−dissipating component (for example, a power MOSFET) is soldered to a PCB, the liberal use of vias, both directly on the mounting pad and immediately surrounding it, is recommended. Two important reasons for this are: improved current rating through the vias, and improved thermal performance from vias extended to the opposite side of the PCB where a plane can more readily transfer the heat to the air. Make a mirror image of any pad being used to heat sink the MOSFETs on the opposite side of the PCB to achieve the best thermal dissipation to the air around the board. To further improve thermal performance, the largest possible pad area should be used.

The output power path should also be routed to encompass a short distance. The output power path is formed by the current path through the inductor, the output capacitors, and the load.

For best EMI containment, use a solid power ground plane as one of the inner layers extending fully under all the power components.

It is important for conversion efficiency that MOSFET drivers, such as ADP3611, are placed as close to the MOSFETs as possible. Thick and short traces are required between the driver and MOSFET gate, especially for the SR MOSFETs. Ground the MOSFET driver's GND pin through the closest vias.

Signal Circuitry

The output voltage is sensed and regulated between the FB pin and the FBRTN pin, which connects to the signal ground at the load. To avoid differential mode noise pickup in the sensed signal, the loop area should be small. Therefore, route the FB and FBRTN traces adjacent to each other atop the power ground plane back to the controller. To filter any noise from the FBRTN trace, using a 1000 pF MLCC is suggested. It should be placed between the FBRTN pin and local ground and as close to the FBRTN pin as possible.

Connect the feedback traces from the switch nodes as close as possible to the inductor. The CSREF signal should be Kelvin connected to the center point of the copper bar, which is the VCore common node for the inductors of all phases.

On the back side of the ADP3207C package, a metal pad can be used as the device heat sink. In addition, running vias under the ADP3207C is not recommended because the metal pad can cause shorting between vias.

ORDERING INFORMATION

Device	Temperature Range	Package	Shipping†
ADP3207CJCPZ−RL	0°C to 100°C	LFCSP40	2500 / Tape & Reel
ADP3207CFJCPZ−RL	0°C to 100°C	LFCSP40	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*The "Z" suffix indicates Pb−Free part.

LFCSP40 6x6, 0.5P
CASE 932AC
ISSUE A

DATE 23 JAN 2009

SCALE 2:1