ADP3208D

7-Bit, Programmable, Dual-Phase, Mobile, CPU, Synchronous Buck Controller

The ADP3208D is a highly efficient, multiphase, synchronous buck switching regulator controller. With its integrated drivers, the ADP3208D is optimized for converting the notebook battery voltage into the core supply voltage required by high performance Intel processors. An internal 7−bit DAC is used to read a VID code directly from the processor and to set the CPU core voltage to a value within the range of 0.3 V to 1.5 V. The phase relationship of the output signals ensures interleaved 2−phase operation.

The ADP3208D uses a multi−mode architecture run at a programmable switching frequency and optimized for efficiency depending on the output current requirement. The ADP3208D switches between single− and dual−phase operation to maximize efficiency with all load conditions. The chip includes a programmable load line slope function to adjust the output voltage as a function of the load current so that the core voltage is always optimally positioned for a load transient. The ADP3208D also provides accurate and reliable short−circuit protection, adjustable current limiting, and a delayed power−good output. The IC supports On−The−Fly (OTF) output voltage changes requested by the CPU.

The ADP3208D is specified over the extended commercial temperature range of −10°C to 100°C and is available in a 48−lead LFCSP.

ON Semiconductor

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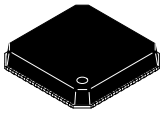
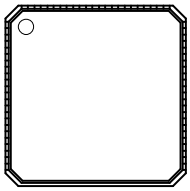


LFCSP48
CASE 932AD

MARKING DIAGRAM



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ORDERING INFORMATION

Features

- Single−Chip Solution
- Case−Differentially Sensed Core Voltage Error Overtemperature
- Automatic Power−Saving Mode Maximizes Efficiency with Light Load During Deeper Sleep Operation
- Soft Transient Control Reduces Inrush Current and Audio Noise
- Active Current Balancing Between Output Phases
- Independent Current Limit and Load Line Setting Inputs for Additional Design Flexibility
- Built−In Power−Good Blanking Supports Voltage Identification (VID) OTF Transients
- 7−Bit, Digitally Programmable DAC with 0.3 V to 1.5 V Output
- Short−Circuit Protection with Latchoff Delay
- Clock Enable Output Delays the CPU Clock Until the Core Voltage is Stable
- Output Load Current Monitor
- This is a Pb−Free Device

Applications

- Notebook Power Supplies for Next Generation Intel® Processors

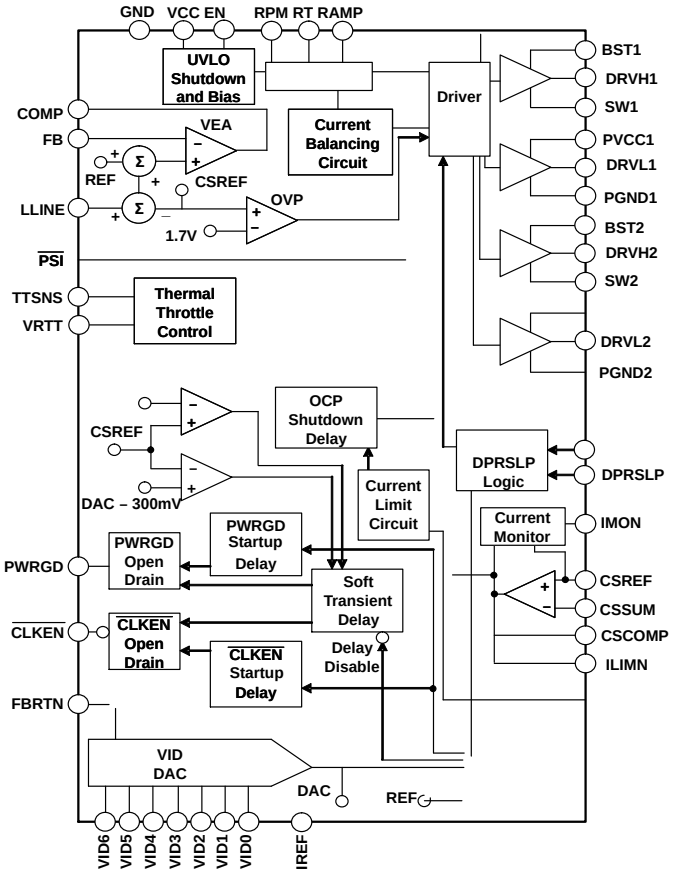


Figure 1. Functional Block Diagram

TEST CIRCUITS

Figure 2. Closed−Loop Output Voltage Accuracy

Figure 3. Current Sense Amplifier, V_{OS}

Figure 4. Positioning Accuracy

PIN FUNCTION DESCRIPTIONS

ELECTRICAL CHARACTERISTICS

– ° °

Ω

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VOLTAGE CONTROL – Voltage Error Amplifier (VEAMP)						
			–			
			–			
			–			
	–		–	–	–	
				–		
				–		μ
		– Ω				
VID DAC VOLTAGE REFERENCE						
	–		– –			
–			–			
	Δ					
–						μ
–		–				
		–				μ
		– – –				μ
						μ
VOLTAGE MONITORING AND PROTECTION – Power Good						
			– –	– –	– –	
			–	– –	–	

ELECTRICAL CHARACTERISTICS

– ° °

Ω

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VOLTAGE MONITORING AND PROTECTION – Power Good						
						µ
		– – –				
		– – –				
						µ
–						Ω
CURRENT CONTROL – Current Sense Amplifier (CSAMP)						
–						
		° – – ° ° – – ° °	– – –			
			–			

ELECTRICAL CHARACTERISTICS

Ω

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DPRSLP						
		≥ μ ≤ − μ				

ELECTRICAL CHARACTERISTICS

TYPICAL PERFORMANCE CHARACTERISTICS

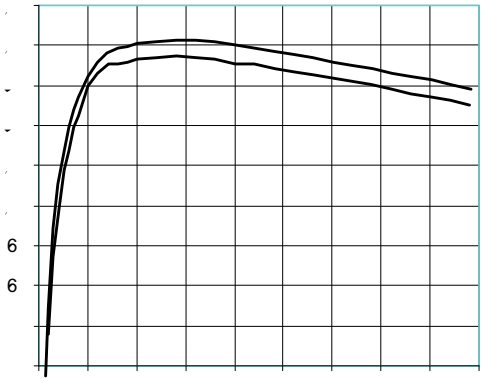


Figure 7. PWM Mode Efficiency vs. Load Current

Figure 8. Load Transient with 2−Phases

Figure 9. Load Transient with 2 Phases

Figure 10. Switching Waveforms in 2 Phase

Figure 11. Switching Waveforms in 2−Phase

Figure 12. Switching Frequency vs. VID Output Voltage in PWM Mode

TYPICAL PERFORMANCE CHARACTERISTICS

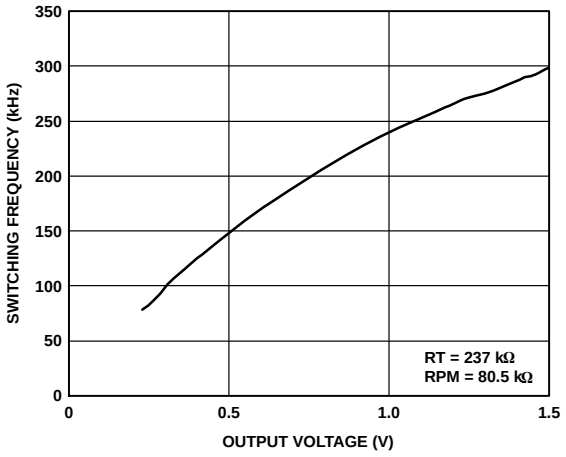


Figure 13. Switching Frequency vs. Output Voltage in RPM Mode

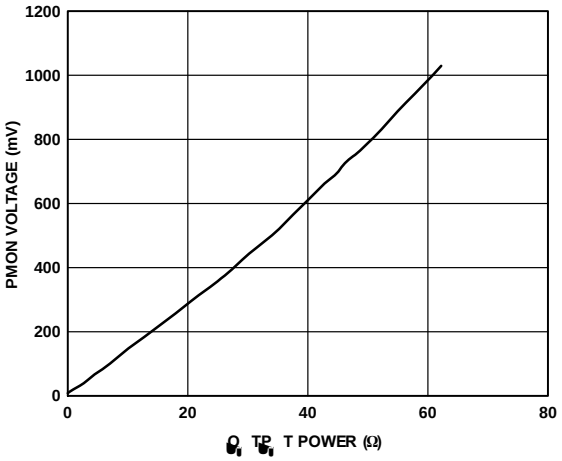


Figure 14. IMON Voltage vs. Output Current

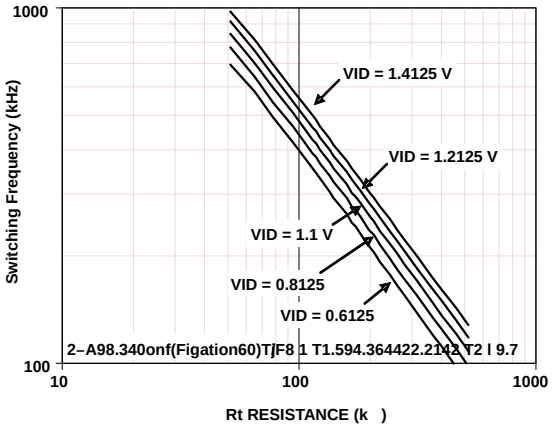


Figure 15. Per Phase Switching Frequency vs. RT Resistance

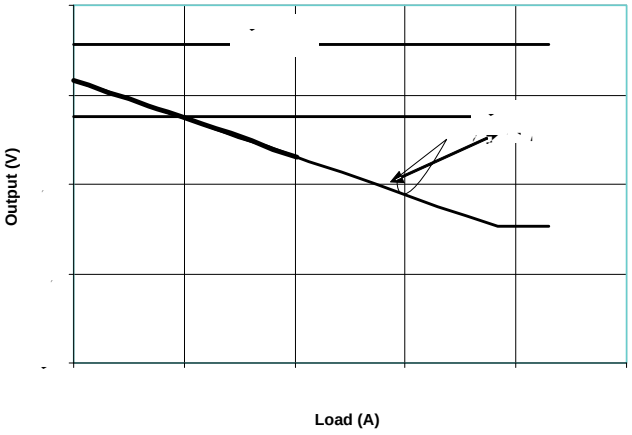


Figure 16. Load Line Accuracy

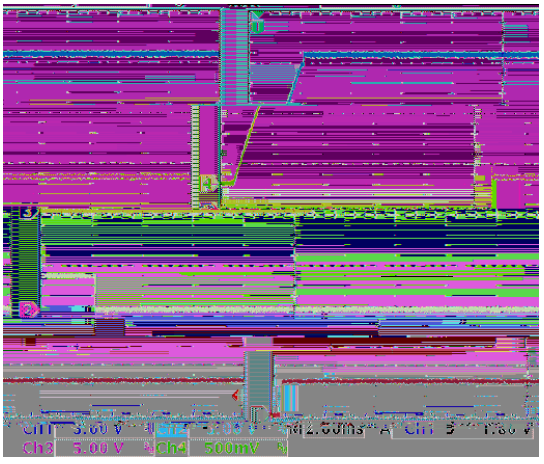
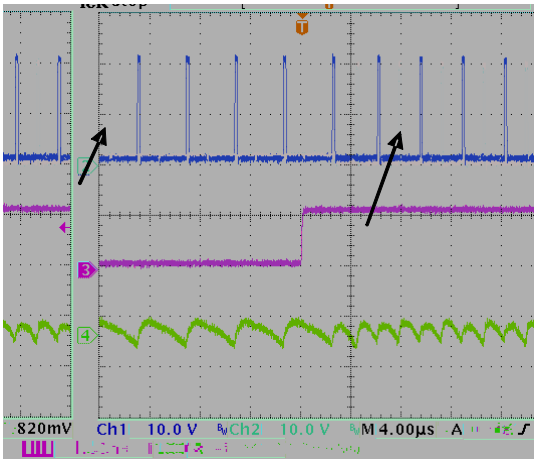


Figure 17. VCC Current vs. VCC Voltage with Enable Low

Figure 18. Startup Waveforms


820mV
Ch1 10.0 V
Ch2 10.0 V
M 4.00µs A


Ch3 5.00 V
Ch4 20.0mV

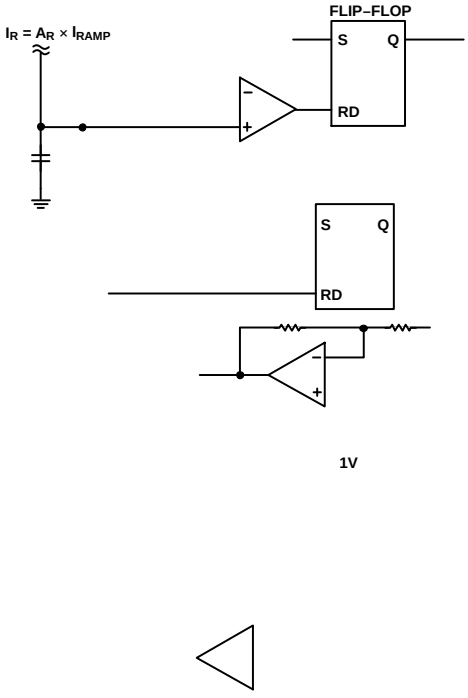


Figure 26. Single−Phase RPM Mode Operation

Output Current Sensing

The ADP3208D includes a dedicated Current Sense

is set via the 7−bit VID DAC. The VID codes are listed in the VID Code table. The noninverting input voltage is offset by the droop voltage as a function of current, commonly known as active voltage positioning. The output of the error amplifier is the COMP pin, which sets the termination voltage of the internal PWM ramps.

At the negative input, the FB pin is tied to the output sense location using R_B, a resistor for sensing and controlling the output voltage at the remote sensing point. The main loop compensation is incorporated in the feedback network connected between the FB and COMP pins.

Power−Good Monitoring

The power−good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open−drain output that can be pulled up through an external resistor to a voltage rail, not necessarily the same VCC voltage rail that is running the controller. A logic high level indicates that the output voltage is within the voltage limits defined by a range around the VID voltage setting. PWRGD goes low when the output voltage is outside of this range.

Following the IMVP−6+ specification, the PWRGD range is defined to be 300 mV less than and 200 mV greater than the actual VID DAC output voltage. For any DAC voltage less than 300 mV, only the upper limit of the PWRGD range is monitored. To prevent a false alarm, the power−good circuit is masked during various system transitions, including a VID change and entrance into or exit out of deeper sleep. The duration of the PWRGD mask is set to approximately 130 μs by an internal timer. If the voltage drop is greater than 200 mV during deeper sleep entry or slow deeper sleep exit, the duration of PWRGD masking is extended by the internal logic circuit.

Powerup Sequence and Soft−Start

The power−on ramp−up time of the output voltage is set internally. The powerup sequence, including the soft−start is illustrated in Figure 29.

After EN is asserted high, the soft−start sequence starts. The core voltage ramps up linearly to the boot voltage. The ADP3208D regulates at the boot voltage for 100 μs. After the boot time is completed, $\overline{\text{CLKEN}}$ is asserted low. After $\overline{\text{CLKEN}}$ is asserted low for 9ms, PWRGD is asserted high.

In VCC UVLO or in shutdown, a small MOSFET turns on connecting the CSREF to GND. The MOSFET on the CSREF pin has a resistance of approximately 100Ω. When VCC ramps above the upper UVLO threshold and EN is asserted high, the ADP3208D enables internal bias and starts a reset cycle that lasts about 50 μs to 60 μs. Next, when initial reset is over, the chip detects the number of phases set by the user, and gives a go signal to start soft−start. The ADP3208D reads the VID codes provided by the CPU on VID0 to VID6 input pins after $\overline{\text{CLKEN}}$ is asserted low. The PWRGD signal is asserted after a t_{CPU_PWRGD} delay of about 9 ms, as specified by IMVP−6+. The power−good delay is programmed internally.

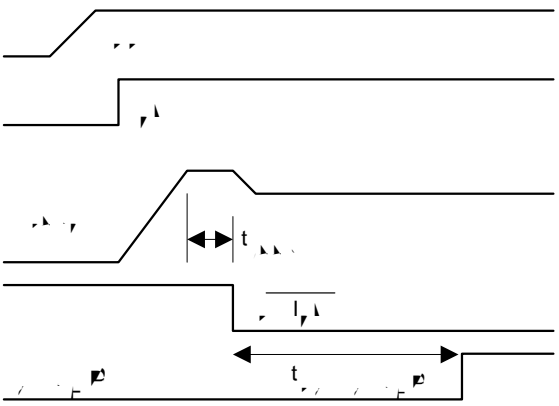


Figure 29. Powerup Sequence of ADP3208D

If EN is taken low or VCC drops below the VCC UVLO threshold, both the SS capacitor and the PGDELAY capacitor are reset to ground to prepare the chip for a subsequent soft−start cycle.

Soft Transient

When a VID input changes, the ADP3208D detects the change but ignores new code for a minimum of 400 ns. This delay is required to prevent the device from reacting to digital signal skew while the 7−bit VID input code is in transition. Additionally, the VID change triggers a PWRGD masking timer to prevent a PWRGD failure. Each VID change resets and retriggers the internal PWRGD masking timer.

The ADP3208D provides a soft transient function to reduce inrush current during VID transitions. Reducing the inrush current helps decrease the acoustic noise generated by the MLCC input capacitors and inductors.

The soft transient feature is implemented internally. When a new VID code is detected, the ADP3208D steps sequentially through each VID voltage to the final VID voltage. There is a PWRGD masking time of 100μs after the last VID code is changed internally. Table 2 lists the soft transient slew rate.

Table 2. Soft Transient Slew Rate

VID Transient	DPRSLP	Slew Rate
		− μ
		μ
		μ
		± μ

Current Limit

The ADP3208D compares the differential output of a current sense amplifier to a programmable current limit setpoint to provide current limiting function. The current limit set point is set with a resistor connected from I_{LIM} pin to CSCOMP pin. This is the R_{lim} resistor. During normal

operation, the voltage on the I_{LIM} pin is equal to the CSREF pin. The voltage across R_{LIM} is equal to the voltage across the CSA (from CSREF pin to CSCOMP pin). This voltage is proportional to output current. The current through R_{LIM} is proportional to the output inductor current. The current through R_{LIM} is compared with an internal reference current. When the R_{LIM} current goes above the internal reference current, the ADP3208D goes into current limit. The current limit circuit is shown in Figure 30.

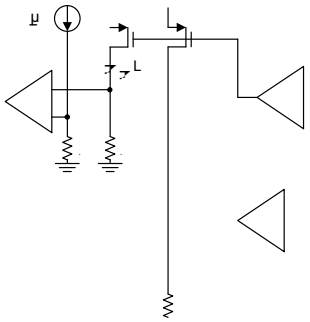


Figure 30. Current Limit Circuit

If DPRSLP is pulled high, the ADP3208D operates in RPM mode. If the load condition is light, the chip enters Discontinuous Conduction Mode (DCM). Figure 33 shows a typical single−phase buck with one upper FET, one lower FET, an output inductor, an output capacitor, and a load resistor. Figure 34 shows the path of the inductor current with the upper FET on and the lower FET off. In Figure 35 the high−side FET is off and the low−side FET is on. In CCM, if one FET is on, its complementary FET must be off; however, in DCM, both high− and low−side FETs are off and no current flows into the inductor (see Figure 36). Figure 37 shows the inductor current and switch node voltage in DCM.

In DCM with a light load, the ADP3208D monitors the switch node voltage to determine when to turn off the low−side FET. Figure 38 shows a typical waveform in DCM with a 1 A load current. Between t_1 and t_2, the inductor current ramps down. The current flows through the source drain of the low−side FET and creates a voltage drop across the FET with a slightly negative switch node. As the inductor current ramps down to 0 A, the switch voltage approaches 0 V, as seen just before t_2. When the switch voltage is approximately −6 mV, the low−side FET is turned off.

Figure 37 shows a small, dampened ringing at t_2. This is caused by the LC created from capacitance on the switch node, including the C_{DS} of the FETs and the output inductor. This ringing is normal.

The ADP3208D automatically goes into DCM with a light load. Figure 38 shows the typical DCM waveform of the ADP3208D. As the load increases, the ADP3208D enters into

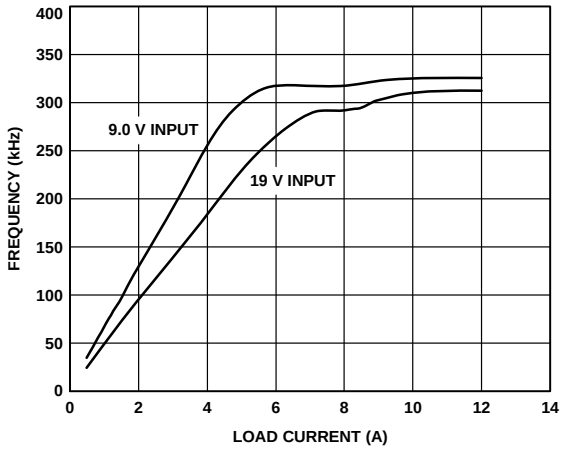


Figure 39. Single−Phase CCM/DCM Frequency vs. Load Current

Output Crowbar

To prevent the CPU and other external components from damage due to overvoltage, the ADP3208D turns off the DRVH1 and DRVH2 outputs and turns on the DRVL1 and DRVL2 outputs when the output voltage exceeds the OVP threshold (1.7 V typical).

Turning on the low−side MOSFETs forces the output capacitor to discharge and the current to reverse due to current build up in the inductors. If the output overvoltage is due to a drain−source short of the high−side MOSFET, turning on the low−side MOSFET results in a crowbar across the input voltage rail. The crowbar action blows the fuse of the input rail, breaking the circuit and thus protecting the microprocessor from destruction.

When the OVP feature is triggered, the ADP3208D is latched off. The latchoff function can be reset by removing and reapplying VCC to the ADP3208D or by briefly pulling the EN pin low.

Pulling TTSNS to less than 1.0 V disables the overvoltage protection function. In this configuration, VRTT should be tied to ground.

Reverse Voltage Protection

Very large reverse current in inductors can cause negative V_{CORE} voltage, which is harmful to the CPU and other output components. The ADP3208D provides a reverse voltage protection (RVP) function without additional system cost. The V_{CORE} voltage is monitored through the CSREF pin. When the CSREF pin voltage drops to less than −300 mV, the ADP3208D triggers the RVP function by disabling all PWM outputs and driving DRVL1 and DRVL2

Table 3. VID Code Table

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output (V)

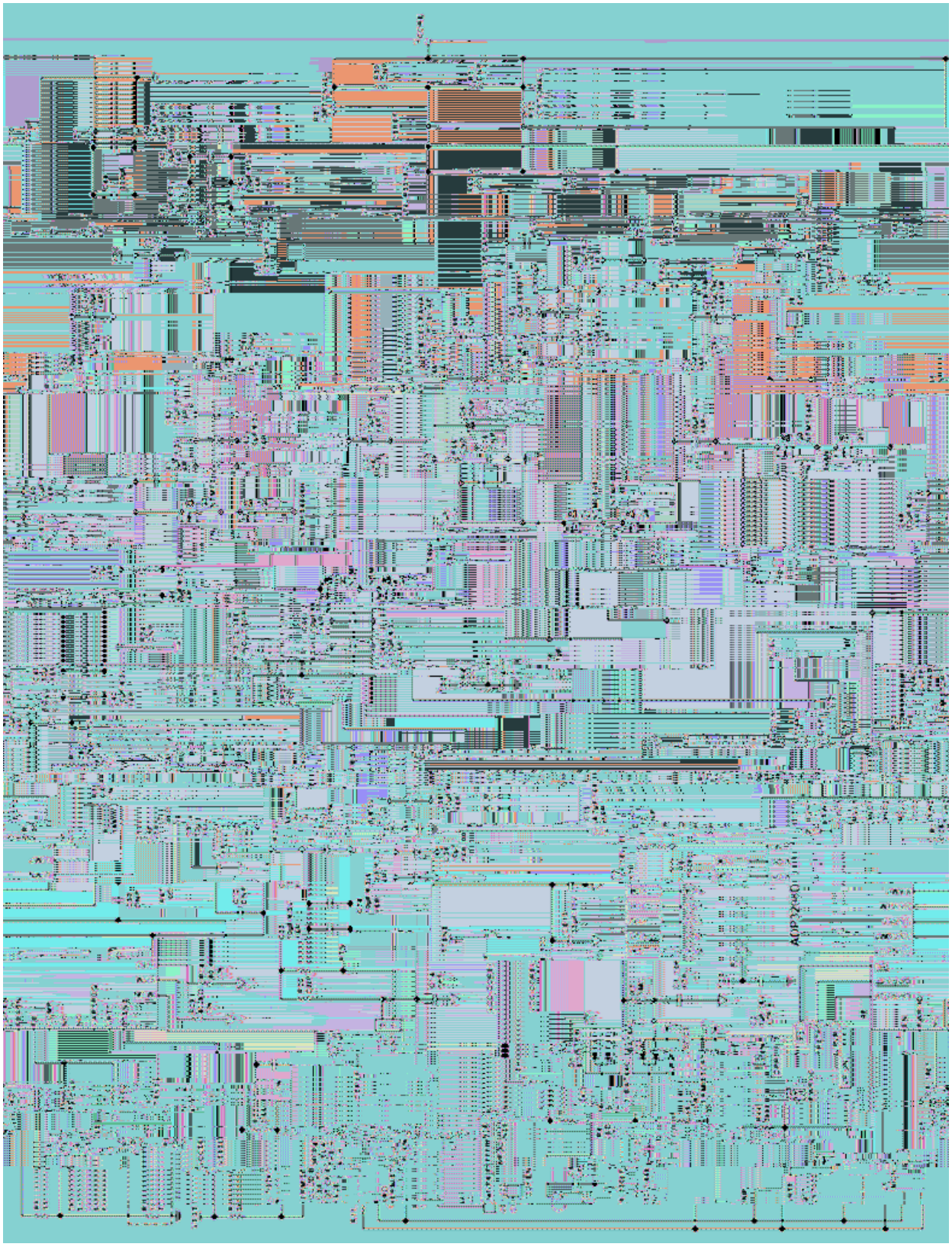


Figure 41. Typical 2−Phase Application Circuit

Application Information

The design parameters for a typical IMVP−6+ compliant CPU core VR application are as follows:

- Maximum input voltage (V_{INMAX}) = 19 V
- Minimum input voltage (V_{INMIN}) = 8.0 V
- Output voltage by VID setting (V_{VID}) = 1.4375 V
- Maximum output current (I_O) = 40 A
- Droop resistance (R_O) = 2.1 mΩ
- Nominal output voltage at 40 A load (V_{OFL}) = 1.3535 V
- Static output voltage drop from no load to full load (ΔV) = V_{ONL} − V_{OFL} = 1.4375 V − 1.3535 V = 84 mV
- Maximum output current step (ΔI_O) = 27.9 A
- Number of phases (n) = 2
- Switching frequency per phase (f_{SW}) = 300 kHz
- Duty cycle at maximum input voltage (D_{MAX}) = 0.18 V
- Duty cycle at minimum input voltage (D_{MIN}) = 0.076 V

Setting the Clock Frequency for PWM

In PWM operation, the ADP3208D uses a fixed−frequency control architecture. The frequency is set by an external timing resistor (RT). The clock frequency and the number of phases determine the switching frequency per phase, which relates directly to the switching losses and the sizes of the inductors and input and output capacitors. For a dual−phase design, a clock frequency of 600 kHz sets the switching frequency to 300 kHz per phase. This selection represents the trade−off between the switching losses and the minimum sizes of the output filter components. To achieve a 600 kHz oscillator frequency at a VID voltage of 1.2 V, RT must be 187 kΩ. Alternatively, the value for RT can be calculated by using the following equation:

$$= \frac{+}{\times \quad \times f \quad \times} - \qquad \Omega$$

where:

9 pF and 16 kΩ are internal IC component values.

V_{VID} is the VID voltage in volts.

n is the number of phases.

f_{SW} is the switching frequency in hertz for each phase.

For good initial accuracy and frequency stability, it is recommended to use a 1% resistor.

When VARFREQ pin is connected to ground, the switching frequency does not change with VID. The value for RT can be calculated by using the following equation.

$$= \frac{}{\times f \quad \times} - \qquad \Omega$$

For good initial accuracy and frequency stability, it is recommended to use a 1% resistor.

Setting the Switching Frequency for RPM Operation of Phase 1

During the RPM mode operation of Phase 1, the ADP3208D runs in pseudo constant frequency, given that the load current is high enough for continuous current mode. While in discontinuous current mode, the switching frequency is reduced with the load current in a linear manner. When considering power conversion efficiency in light load, lower switching frequency is usually preferred for RPM mode. However, the V_{CORE} ripple specification in the IMVP−6 sets the limitation for lowest switching frequency. Therefore, depending on the inductor and output capacitors, the switching frequency in RPM mode can be equal, larger, or smaller than its counterpart in PWM mode.

A resistor from RPM to GND sets the pseudo constant frequency as following:

$$= \quad \times f \quad \times \frac{\times}{} \times \quad \times \frac{}{} \times$$

where:

A_R is the internal ramp amplifier gain.

C_R is the internal ramp capacitor value.

R_R is an external resistor on the RAMPADJ pin to set the internal ramp magnitude.

Because R_R = 280 kΩ, the following resistance sets up 300 kHz switching frequency in RPM operation.

$$= \quad \times f \quad \times \frac{\times}{} \times \quad \times \frac{}{} \times$$

Inductor Selection

The choice of inductance determines the ripple current of the inductor. Less inductance results in more ripple current, which increases the output ripple voltage and the conduction losses in the MOSFETs. However, this allows the use of smaller−size inductors, and for a specified peak−to−peak transient deviation, it allows less total output capacitance. Conversely, a higher inductance results in lower ripple current and reduced conduction losses, but it requires larger−size inductors and more output capacitance for the same peak−to−peak transient deviation. For a multiphase converter, the practical value for peak−to−peak inductor ripple current is less than 50% of the maximum dc current of that inductor. Equation 5 shows the relationship between the inductance, oscillator frequency, and peak−to−peak ripple current. Equation 6 can be used to determine the minimum inductance based on a given output ripple voltage.

$$= \frac{\times \left(- \quad \right)}{f \quad \times}$$

$$\times$$

$$\geq$$

a calculated ripple current of 9.0 A. The inductor should not saturate at the peak current of 24.5 A, and it should be able to handle the sum of the power dissipation caused by the winding's average current (20 A) plus the ac core loss. In this example, 330 nH is used.

Another important factor in the inductor design is the DCR, which is used for measuring the phase currents. Too large of a DCR causes excessive power losses, whereas too small of a value leads to increased measurement error. For this example, an inductor with a DCR of 0.8 mΩ is used.

Selecting a Standard Inductor

After the inductance and DCR are known, select a standard inductor that best meets the overall design goals. It

4. Compute the relative values for r_{CS1}, r_{CS2}, and r_{TH} by using the following equations:

=

$$\frac{- \times \times - \times - \times + \times - \times}{\times - \times - \times - \times - \times - -}$$

$$= \frac{-}{\frac{}{-} - \frac{}{-}}$$

$$= \frac{}{\frac{}{-} - }$$

5. Calculate $R_{TH} = r_{TH} \times R_{CS}$, and then select a thermistor of the closest value available. In addition, compute a scaling factor k based on the ratio of the actual thermistor value used relative to the computed one:

$$= \frac{}{}$$

6. Calculate values for R_{CS1} and R_{CS2} by using the following equations:

$$= \times \times$$

$$= \times - + \times$$

For example, if a thermistor value of 100 kΩ is selected in Step 1, an available 0603−size thermistor with a value close to R_{CS} is the Vishay NTHS0603N04 NTC thermistor, which has resistance values of A = 0.3359 and B = 0.0771. Using the equations in Step 4, r_{CS1} is 0.359, r_{CS2} is 0.729, and r_{TH} is 1.094. Solving for r

L_X is about 150 pH for the six SP capacitors, which is low enough to avoid ringing during a load change. If the L_X of the chosen bulk capacitor bank is too large, the number of ceramic capacitors may need to be increased to prevent excessive ringing.

For this multi−mode control technique, an all ceramic capacitor design can be used if the conditions of Equations 16, 17, and 18 are satisfied.

Power MOSFETs

For typical 20 A per phase applications, the N−channel power MOSFETs are selected for two high−side switches and two or three low−side switches per phase. The main selection parameters for the power MOSFETs are $V_{GS(TH)}$, Q_G, C_{ISS}, C_{RSS}, and $R_{DS(ON)}$. Because the voltage of the gate driver is 5.0 V, logic−level threshold MOSFETs must be used.

The maximum output current, I_O, determines the $R_{DS(ON)}$ requirement for the low−side (synchronous) MOSFETs. In the ADP3208D, currents are balanced between phases; the current in each low−side MOSFET is the output current divided by the total number of MOSFETs (n_{SF}). With conduction

The previous equation also shows the standby dissipation (I_{CC} times the VCC) of the driver.

Ramp Resistor Selection

The ramp resistor (R_R) is used to set the size of the internal PWM ramp. The value of this resistor is chosen to provide the best combination of thermal balance, stability, and transient response. Use the following expression to determine a starting value:

$$= \frac{\times}{\times \quad \times \quad \times}$$

$$= \frac{\times}{\times \quad \times \quad \Omega \times} = \qquad \Omega$$

where:
A_R is the internal ramp amplifier gain.
A_D is the current balancing amplifier gain.
R_{DS} is the total low−side MOSFET ON−resistance;
C_R is the internal ramp capacitor value.

Another consideration in the selection of R_R is the size of the internal ramp voltage (see Equation 25). For stability and noise immunity, keep the ramp size larger than 0.5 V. Taking this into consideration, the value of R_R in this example is selected as 280 kΩ.

The internal ramp voltage magnitude can be calculated as follows:

$$= \frac{\times \quad - \quad \times}{\times \quad \times f}$$

$$= \frac{\times \quad - \quad \times}{\Omega \times \quad \times} =$$

The size of the internal ramp can be increased or decreased. If it is increased, stability and transient response improves but thermal balance degrades. Conversely, if the ramp size is decreased, thermal balance improves but stability and transient response degrade. In the denominator of Equation 24, the factor of 3 sets the minimum ramp size that produces an optimal combination of good stability, transient response, and thermal balance.

COMP Pin Ramp

In addition to the internal ramp, there is a ramp signal on the COMP pin due to the droop voltage and output voltage ramps. This ramp amplitude adds to the internal ramp to produce the following overall ramp signal at the PWM input:

$$= \frac{}{\left(- \frac{\times \quad - \quad \times}{\times f \quad \times \quad \times} \right)}$$

where C_X is the total bulk capacitance, and R_O is the droop resistance of the regulator.

For this example, the overall ramp signal is 1.85 V.

Current Limit Setpoint

To select the current limit setpoint, the resistor value for R_{CLIM} must be determined. The current limit threshold for the ADP3208D is set with R_{CLIM}. R_{CLIM} can be found using the following equation:

$$= \frac{\times}{\mu}$$

where:
R_{LIM} is the current limit resistor.
R_O is the output load line.
I_{LIM} is the current limit set point.

When the ADP3208D is configured for 2−phase operation, the equation above is used to set the current limit. When the ADP3208D switches from 2−phase to 1−phase operation by $\overline{PSI}$ or DPRSLP signal, the current is single−phase is one half of the current limit in 2−phase.

When the ADP3208D is configured for 1−phase operation, the equation above is used to set the current limit.

Output Current Monitor

The ADP3208D has output current monitor. The IMON pin sources a current proportional to the total inductor current. A resistor, R_{MON}, from IMON to FBRTN sets the gain of the output current monitor. A 0.1 μF is placed in parallel with R_{MON} to filter the inductor current ripple and high frequency load transients. Since the IMON pin is connected directly to the CPU, it is clamped to prevent it from going above 1.15V.

The IMON pin current is equal to the R_{LIM} times a fixed gain of 10. R_{MON} can be found using the following equation:

$$= \frac{\times}{\times \quad \times}$$

where:
R_{MON} is the current monitor resistor. R_{MON} is connected from IMON pin to FBRTN.
R_{LIM} is the current limit resistor.
R_O is the output load line resistance.
I_{FS} is the output current when the voltage on IMON is at full scale.

Feedback Loop Compensation Design

Optimized compensation of the ADP3208D allows the best possible response of the regulator's output to a load change. The basis for determining the optimum compensation is to make the regulator and output decoupling appear as an output impedance that is entirely resistive over the widest possible frequency range, including dc, and that is equal to the droop resistance (R_O). With the resistive output impedance, the output voltage droops in proportion with the load current at any load current slew rate, ensuring the optimal position and allowing the minimization of the output decoupling.

With the multi−mode feedback structure of the ADP3208D, it is necessary to set the feedback compensation so that the converter's output impedance works in parallel with the output decoupling. In addition, it is necessary to compensate for the several poles and zeros created by the output inductor and decoupling capacitors (output filter).

A Type III compensator on the voltage feedback is adequate for proper compensation of the output filter. Figure 43 shows the Type III amplifier used in the ADP3208D. Figure 44 shows the locations of the two poles and two zeros created by this amplifier.

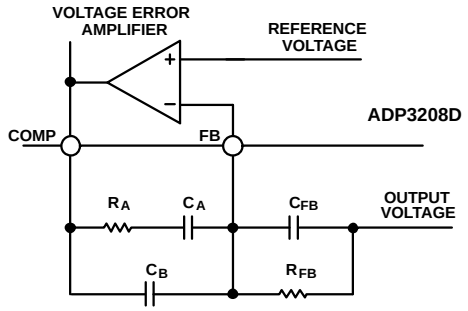


Figure 43. Voltage Error Amplifier

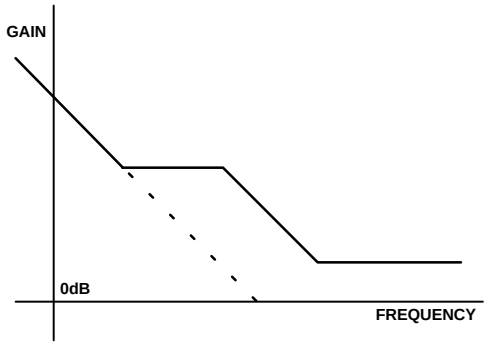


Figure 44. Poles and Zeros of Voltage Error Amplifier

Selecting Thermal Monitor Components

To monitor the temperature of a single−point hot spot, set R_{TTSET1} equal to the NTC thermistor's resistance at the alarm temperature. For example, if the alarm temperature for VRTT is 100°C and a Vishey thermistor (NTHS−0603N011003J) with a resistance of 100 kΩ at 25°C, or 6.8 kΩ at 100°C, is used, the user can set R_{TTSET1} equal to 6.8 kΩ (the R_{TH1} at 100°C).

Figure 45. Single−Point Thermal Monitoring

5. The resulting waveform will be similar to that shown in Figure 47. Use the horizontal cursors to measure V_{ACDRP} and V_{DCDRP}, as shown in Figure 47. Do not measure the undershoot or overshoot that occurs immediately after the step.

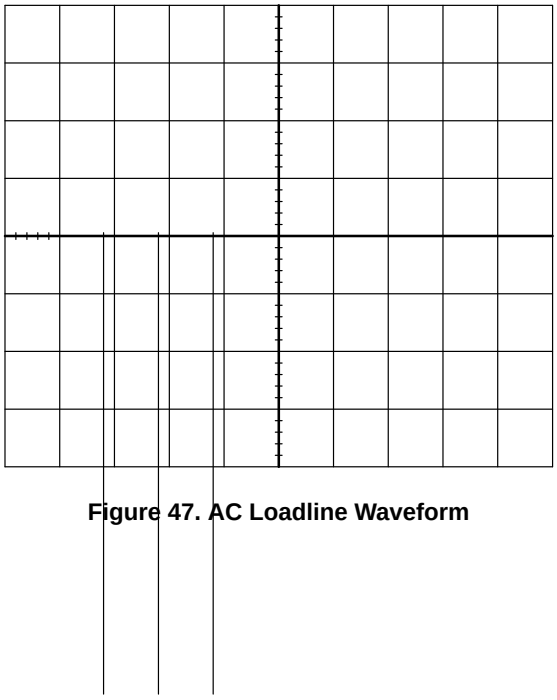


Figure 47. AC Loadline Waveform

Layout and Component Placement

The following guidelines are recommended for optimal performance of a switching regulator in a PC system.

General Recommendations

1. 1. For best results, use a PCB of four or more layers. This should provide the needed versatility for control circuitry interconnections with optimal placement; power planes for ground, input, and output; and wide interconnection traces in the rest of the power delivery current paths. Keep in mind that each square unit of 1 oz copper trace has a

ORDERING INFORMATION

Device	Temperature Range	Package	Package Option	Shipping
–	– ° °	–	– –	

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