PIN FUNCTION DESCRIPTIONS

Pin No	Mnemonic	Description
1	FBRTN	Feedback Return Input/Output. This pin remotely senses the GMCH voltage. It is also used as the ground return for the VID DAC and the voltage error amplifier blocks.
2	FB	Voltage Error Amplifier Feedback Input. The inverting input of the voltage error amplifier.
3	COMP	Voltage Error Amplifier Output and Frequency Compensation Point.
4	CREF	This pins sets the internal bias currents. Connect an 80k resistor from either this pin or IREF pin to ground. If an 80 k resistor is connected from this pin to ground, IREF pin must remain floating.
5	NC	Not Connected.
6	IMON	Current Monitor Output. Open drain output. This pin sources a current proportional to the output load current. A resistor from IMON to FBRTN sets the current monitor gain.
7	IREF	This pins sets the internal bias currents. Connect an 80 k resistor from either this pin or CREF pin to ground. If an 80 k resistor is connected from this pin to ground, CREF pin must remain floating.
8	RPM	RPM Mode Timing Control Input. An external resistor between this pin to ground sets the RPM mode turn on threshold voltage.
9	LLINE	Load Line Programming Input. The center point of a resistor divider connected between CSREF and CSCOMP can be tied to this pin to set the load line slope.
10	CSCOMP	Current Sense Amplifier Output and Frequency Compensation Point.
11	CSREF	Current Sense Reference Input. This pin must be connected to the opposite side of the output inductor.
12	CSFB	Non inverting Input of the Current Sense Amplifier. The combination of a resistor from the switch node to this pin and the feedback network from this pin to the CSCOMP pin sets the gain of the current sense amplifier.
13	RAMP	PWM Ramp Slope Setting Input. An external resistor from the converter input voltage node to this pin sets the slope of the internal PWM stabilizing ramp.
14	ILIMN	Current Limit Set Point. An external resistor between ILIMN and ILIMP sets the current limit set point.
15	ILIMP	Current Limit Set Point. An external resistor between ILIMN and ILIMP sets the current limit set point.
16	RT	PWM Oscillator Frequency Setting Input. An external resistor from this pin to GND sets the PWM oscillator frequency.
17	GND	Analog and Digital Signal Ground.
18	PGND	Low Side Driver Power Ground. This pin should be connected close to the source of the lower MOSFET(s).
19	DRVL	Low Side Gate Drive Output.
20	PVCC	Power Supply Input/Output of Low Side Gate Driver.
21	SW	Current Return For High Side Gate Drive.
22	DRVH	High Side Gate Drive Output.
23	BST	High Side Bootstrap Supply. A capacitor from this pin to SW holds the bootstrapped voltage while the high side MOSFET is on.
24	VCC	Power Supply Input/Output of the Controller.
25 to 29	VID4 to VID0	Voltage Identification DAC Inputs. A 5 bit word (the VID code) programs the DAC output voltage, the reference voltage of the voltage error amplifier without a load (see the VID code table, Table 1). In normal operation mode, the VID DAC output programs the output voltage to a value within the 0 V to 1.25 V range. The input is actively pulled down.
30	EN	Enable Input. Driving this pin low shuts down the chip, disables the driver outputs, and pulls PWRGD low.
31	PWRGD	Power Good Output. Open drain output. A low logic state means that the output voltage is outside of the VID DAC defined range.
32	$\overline{\text{VARFREQ}}$	Variable Frequency Enable Input. Pulling this pin to ground sets the normal RPM mode of operation. Pulling this pin to 5.0 V sets the fixed frequency PWM mode of operation.

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V, FBRTN = GND, $\overline{VARFREQ}$

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V, FBRTN = GND, $\overline{VARFREQ}$ = Low, V_{VID} = 1.25 V, T_A = 10°C to 100°C, unless otherwise noted (Note 1). Current entering a pin (sunk by the device) has a positive sign. R_{REF} = 80 k .

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VOLTAGE MONITORING AND PROTECTION – Power Good						
PWRGD Latchoff Delay	$T_{LOFFPWRGD}$	Measured from Out off Good Window event to Latchoff (switching stops)		8.0		ms
PWRGD Propagation Delay (Note 3)	$T_{PDPWRGD}$	Measured from Out off Good Window event to PWRGD neg edge		200		ns
Crowbar Latchoff Delay (Note 2)	T_{LOFFCB}	Measured from Crowbar event to Latchoff (switching stops)		200		ns
PWRGD Masking Time		Triggered by any VID change or OCP event		100		s
CSREF Soft Stop Resistance		EN = L or Latchoff condition		70		
CURRENT CONTROL – Current Sense Amplifier (CSAMP)						
CSSUM, CSREF Common Mode Range (Note 2)		Voltage range of interest	0		2.0	V
CSSUM, CSREF Offset Voltage	V_{OSCSA}	CSREF CSSUM, T_A = 25°C T_A = 10°C to 85°C	0.5 1.6		+0.5 +1.6	mV
CSSUM Bias Current	I_{BCSSUM}		50		+50	nA
CSREF Bias Current	I_{BCSREF}		2.0		+2.0	A
CSCOMP Voltage Range (Note 2)		Voltage range of interest	0.05		2.0	V
CSCOMP Current	I					

ELECTRICAL CHARACTERISTICS V_{CC}

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V, FBRTN = GND, $\overline{VARFREQ}$ = Low, V_{VID} = 1.25 V, T_A = 10°C to 100°C, unless otherwise noted (Note 1). Current entering a pin (sunk by the device) has a positive sign. R_{REF} = 80 k .

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
HIGH−SIDE MOSFET DRIVER						
Pullup Resistance, Sourcing Current		BST = PVCC		1.8	3.3	
Pulldown Resistance, Sinking Current		BST = PVCC		1.0	3.0	
Transition Times	tr_{DRVH} tf_{DRVH}	BST = PVCC, C_L = 3 nF, Figure 2 BST = PVCC, C_L = 3 nF, Figure 2		15 13	35 31	ns
Dead Delay Times	$tpdh_{DRVH}$	BST = PVCC, Figure 2		30	42	ns
BST Quiescent Current		EN = L (Shutdown) EN = H, no switching		2.0 200	12	A
LOW−SIDE MOSFET DRIVER						
Pullup Resistance, Sourcing Current		BST = PVCC		1.7	3.3	
Pulldown Resistance, Sinking Current		BST = PVCC				

TYPICAL PERFORMANCE CHARACTERISTICS

V_{VID} = 1.5 V, T_A = 20°C to 100°C, unless otherwise noted.

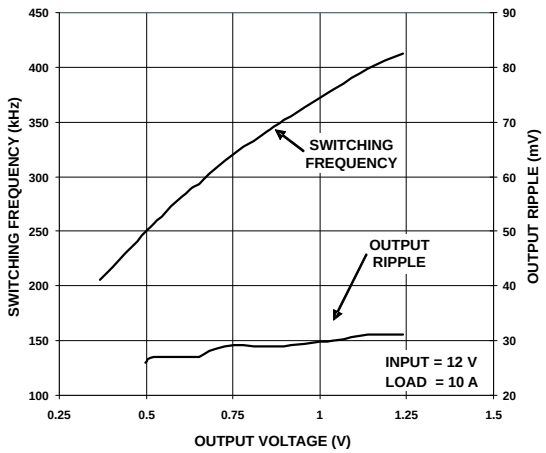

Figure 3. Switching Frequency vs. Load Current in RPM Mode

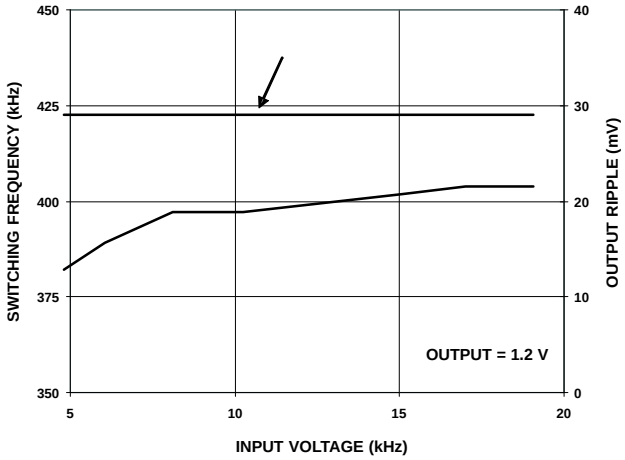

Figure 4. Switching Frequency vs. Input Voltage in RPM Mode

Figure 5. Switching Frequency vs. Input Voltage in RPM Mode

Figure 6. Load Line Accuracy

Figure 7. DCM Waveforms, 0.5 A Load Current

Figure 8. CCM Waveforms, 3 A Load Current

TYPICAL PERFORMANCE CHARACTERISTICS

V_{VID} = 1.5 V, T_A = 20°C to 100°C, unless otherwise noted.

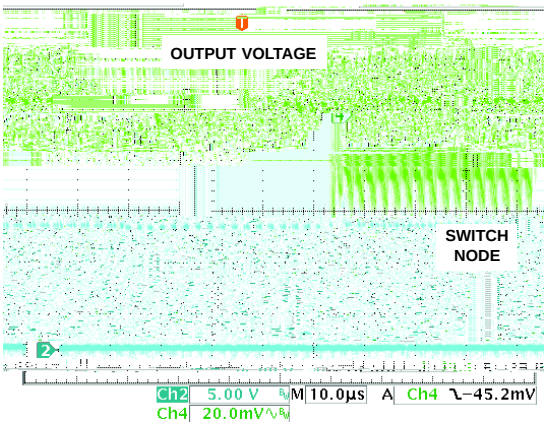

Figure 9. Load Transient, 3 A to 10 A, V_{IN} = 12 V

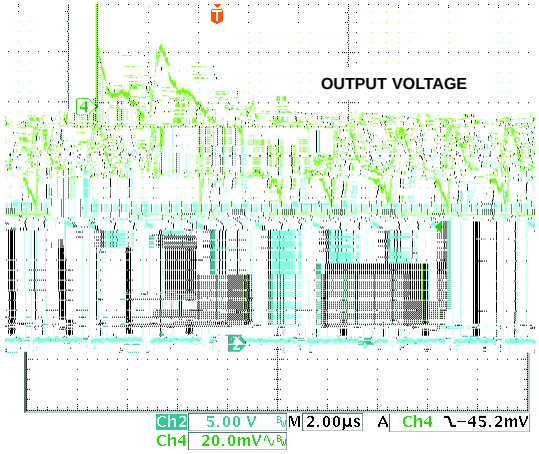

Figure 10. Load Transient, 3 A to 10 A, V_{IN} = 12 V

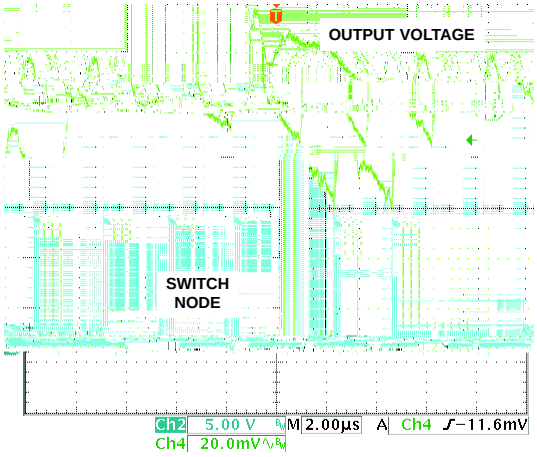

Figure 11. Load Transient, 3 A to 10 A, V_{IN} = 12 V

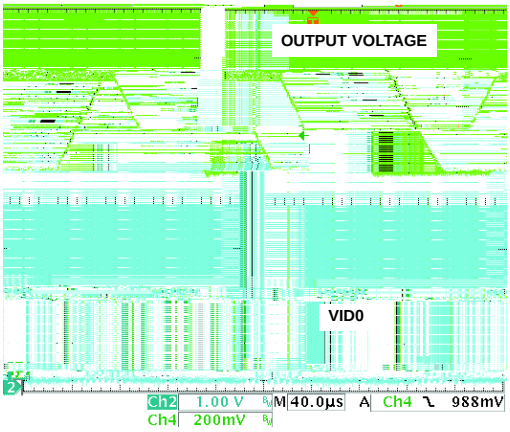

Figure 12. VID OTF, 1.25 V to 0.85 V

Theory of Operation

The ADP3209D is a ramp−pulse−modulated (RPM) controller for synchronous buck Intel GMCH core power supply. The internal 5−bit VID DAC conforms to the Intel IMVP−6+ specifications. The ADP3209D is a stable, high performance architecture that includes

- High speed response at the lowest possible switching frequency and minimal count of output decoupling capacitors
- Minimized thermal switching losses due to lower frequency operation
- High accuracy load line regulation
- High power conversion efficiency with a light load by automatically switching to DCM operation

Operation Modes

The ADP3209D runs in RPM mode for the purpose of fast transient response and high light load efficiency. During the following transients, the ADP3209D runs in PWM mode:

- Soft−Start
- Soft transient: the period of 100 s following any VID change
- Current overload

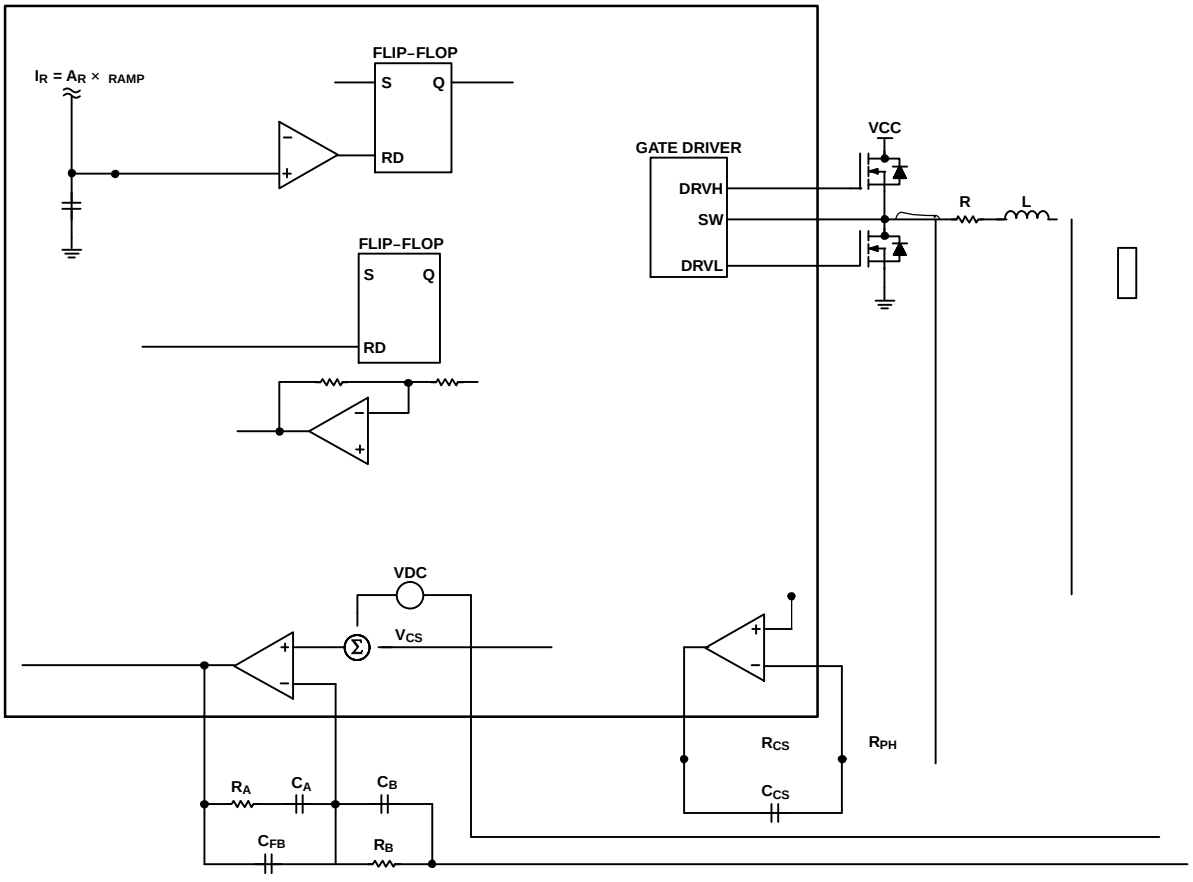

Figure 13. RPM Mode Operation

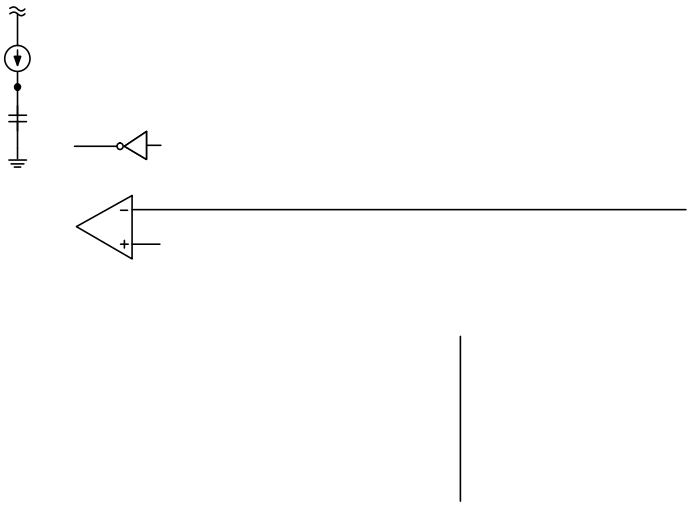

Figure 14. PWM Mode Operation

The ADP3209D provides a soft transient function to reduce inrush current during VID transitions. Reducing the inrush current helps decrease the acoustic noise generated by the MLCC input capacitors and inductors.

The soft transient feature is implemented internally. When a new VID code is detected, the ADP3209D steps sequentially through each VID voltage to the final VID voltage. The ADP3209D steps through VID codes every 0.5¸ s. This gives a soft transient slew rate of 25 mV per 0.5¸ s or 12.5 mV/¸ s. There is a PWRGD masking time of 100¸

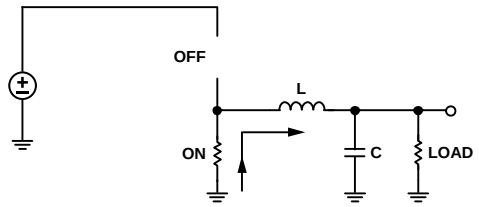

Figure 19. Buck Topology Inductor Current During t_1 and t_2

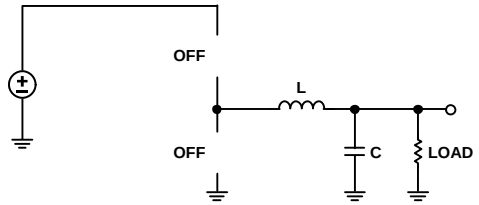

Figure 20. Buck Topology Inductor Current During t_2 and t_3

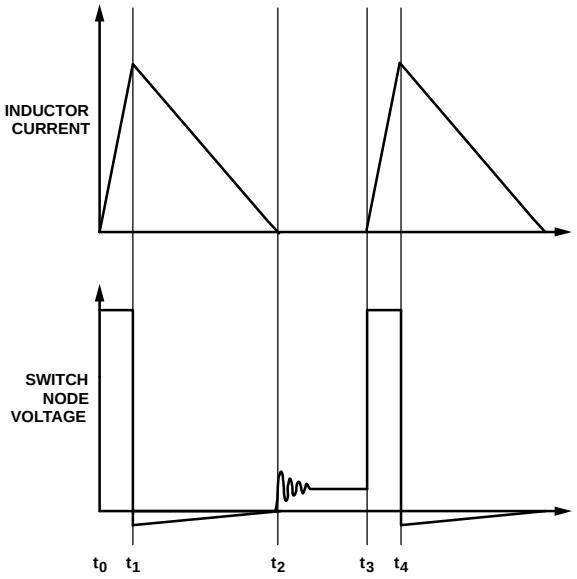

Figure 21. Inductor Current and Switch Node in DCM

Figure 22. Single−Phase Waveforms in DCM with 1 A Load Current

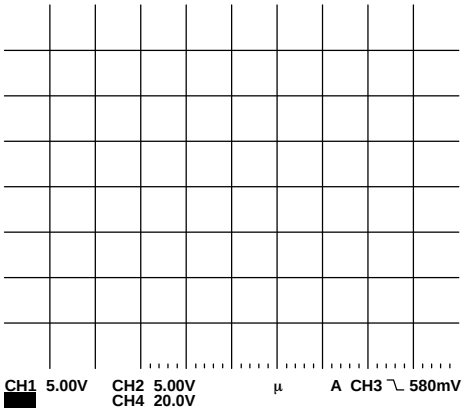

Figure 23. ADP3209D RVP Function

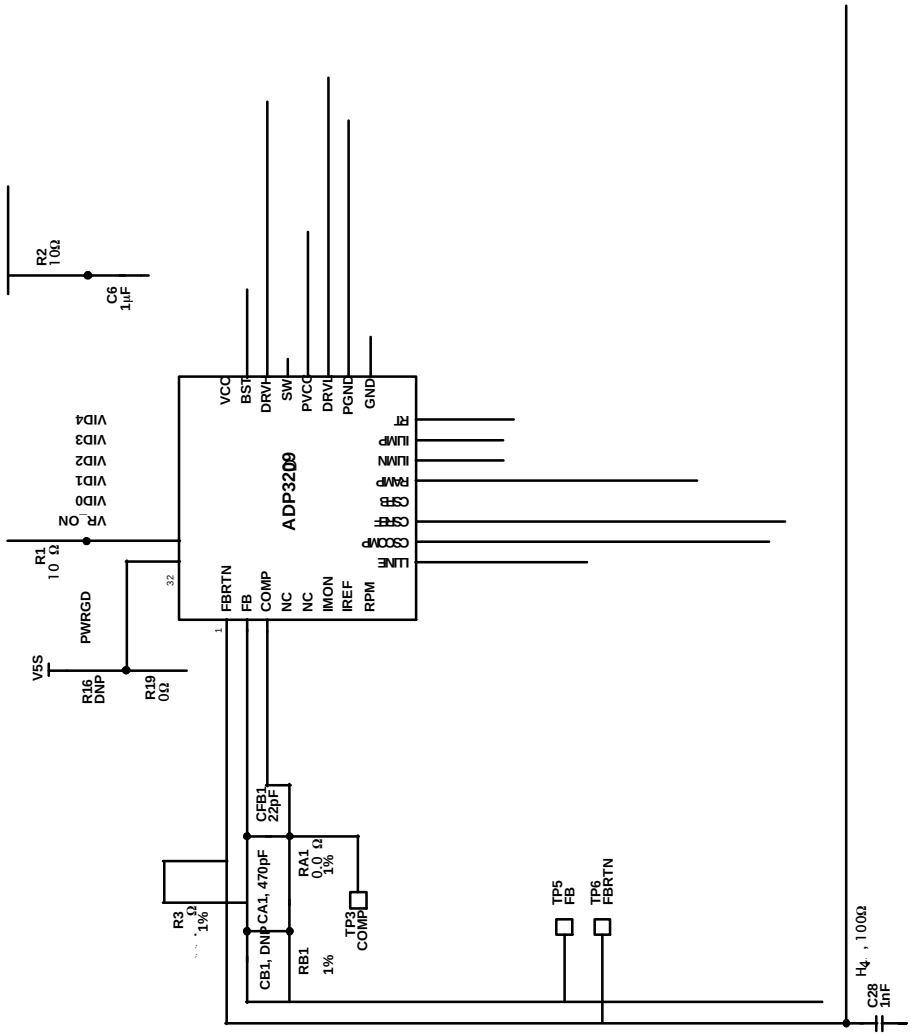

Figure 24. Typical Application Circuit

Application Information

The design parameters for a typical IMVP−6+ compliant GPU core VR application are as follows:

Maximum input voltage (V_{INMAX}) = 19 V

Minimum input voltage (V_{INMIN}) = 8.0 V

Output voltage by VID setting (V_{VID}) = 1.25 V

Maximum output current (I_O) = 15 A

Droop resistance (R_O) = 5.1 m

Nominal output voltage at 15 A load (V_{OFL}) = 1.174 V

Static output voltage drop from no load to full load (ΔV) = V_{ONL} − V_{OFL} = 1.25 V − 1.174 V = 76 mV

Maximum output current step (ΔI_O) = 8 A

Number of phases (n) = 1

Switching frequency (f_{SW}) = 390 kHz

Duty cycle at maximum input voltage (D_{MAX}) = 0.15 V

Duty cycle at minimum input voltage (D_{MIN}) = 0.062 V

Setting the Clock Frequency for PWM

In PWM operation, the ADP3209D uses a fixed−frequency control architecture. The frequency is set by an external timing resistor (RT). The clock frequency determines the switching frequency, which relates directly to the switching losses and the sizes of the inductors and input and output capacitors. For example, a clock frequency of 300 kHz sets the switching frequency to 300 kHz. This selection represents the trade−off between the switching losses and the minimum sizes of the output filter components. To achieve a 300 kHz oscillator frequency at a VID voltage of 1.2 V, RT must be 237 k . Alternatively, the value for RT can be calculated by using the following equation:

$$R_T \approx \frac{V_{VID} - 1.0\ V}{2 \times f_{SW} \times 9\ pF} - 16\ k \qquad \text{(eq. 1)}$$

where:
9 pF and 16 k are internal IC component values.
V_{VID} is the VID voltage in volts.
f_{SW} is the switching frequency in hertz.

For good initial accuracy and frequency stability, it is recommended to use a 1% resistor.

With $\overline{\text{VARFREQ}}$ pulled above 4.0 V, the ADP3209D operates with a constant switching frequency. The switching frequency does not change with VID voltage, input voltage, or load current. In addition, the DCM operation at light load is disabled, so the ADP3209D operates in CCM. The value of RT can be calculated by using the following equation:

$$R_T \approx \frac{1.0\ V}{f_{SW} \times 9\ pF} - 16\ k \qquad \text{(eq. 2)}$$

Ramp Resistor Selection

The ramp resistor (R_R) is used for setting the size of the internal PWM ramp. The value of this resistor is chosen to provide the best combination of thermal balance, stability, and transient response. Use this equation to determine a starting value:

$$R_R \approx \frac{A_R \times L}{3 \times A_D \times R_{DS} \times C_R} \qquad \text{(eq. 3)}$$

$$R_R \approx \frac{0.5 \times 360\ nH}{3 \times 5 \times 5.2\ m \quad \times 5\ pF} - 462\ k$$

where:
A_R is the internal ramp amplifier gain.
A_D is the current balancing amplifier gain.
R_{DS} is the total low−side MOSFET ON−resistance,
C_R is the internal ramp capacitor value.

Another consideration in the selection of R_R is the size of the internal ramp voltage (see Equation 3). For stability and noise immunity, keep this ramp size larger than 0.5 V. Taking this into consideration, the value of R_R

Because R_R = 280 k , the following resistance sets up 300 kHz switching frequency in RPM operation.

$$R_{RPM} \approx \frac{2 \times 280\ k}{1.150\ V - 1.0\ V} \times \frac{0.5 \times (1 - 0.061) \times 1.150}{462\ k \times 5\ pF \times 300\ kHz} \approx 500\ k \times 202\ k \quad \text{(eq. 6)}$$

Inductor Selection

The choice of inductance determines the ripple current of the inductor. Less inductance results in more ripple current, which increases the output ripple voltage and the conduction losses in the MOSFETs. However, this allows the use of smaller−size inductors, and for a specified peak−to−peak transient deviation, it allows less total output capacitance. Conversely, a higher inductance results in lower ripple current and reduced conduction losses, but it requires larger−size inductors and more output capacitance for the same peak−to−peak transient deviation. For a buck converter, the practical value for peak−to−peak inductor ripple current is less than 50% of the maximum dc current of that inductor. Equation 7 shows the relationship between the inductance, oscillator frequency, and peak−to−peak ripple current. Equation 8 can be used to determine the minimum inductance based on a given output ripple voltage.

$$I_R \approx \frac{V_{VID} \times (1 - D_{MIN})}{f_{SW} \times L} \quad \text{(eq. 7)}$$

$$L \approx \frac{V_{VID} \times R_O \times (1 - (n \times D_{MIN}))}{f_{SW} \times V_{RIPPLE}} \quad \text{(eq. 8)}$$

In this example, R_O is assumed to be the ESR of the output capacitance, which results in an optimal transient response. Solving Equation 9 for a 16 mV peak−to−peak output ripple voltage yields:

$$L \approx \frac{1.174\ V \times 5.1\ m\ \ (1 - 0.062)}{390\ kHz \times 16\ mV} \approx 901\ nH \quad \text{(eq. 9)}$$

If the resultant ripple voltage is less than the initially selected value, the inductor can be changed to a smaller value until the ripple value is met. This iteration allows optimal transient response and minimum output decoupling. In this example, the iteration showed that a 560 nH inductor was sufficient to achieve a good ripple.

The smallest possible inductor should be used to minimize the number of output capacitors. Choosing a 560 nH inductor is a good choice for a starting point, and it provides a calculated ripple current of 6.6 A. The inductor should not saturate at the peak current of 18.3 A, and it should be able to handle the sum of the power dissipation caused by the winding's average current (15 A) plus the ac core loss.

Another important factor in the inductor design is the DCR, which is used for measuring the inductor current. Too large of a DCR causes excessive power losses, whereas too small of a value leads to increased measurement error. For this example, an inductor with a DCR of 1.3 m is used.

Selecting a Standard Inductor

After the inductance and DCR are known, select a standard inductor that best meets the overall design goals. It is also important to specify the inductance and DCR tolerance to maintain the accuracy of the system. Using 20% tolerance for the inductance and 15% for the DCR at room temperature are reasonable values that most manufacturers can meet.

Power Inductor Manufacturers

The following companies provide surface−mount power inductors optimized for high power applications upon request.

Vishay Dale Electronics, Inc.

Panasonic

Sumida Electric Company

NEC Tokin Corporation

Output Droop Resistance

The design requires that the regulator output voltage measured at the chipset pins decreases when the output current increases. The specified voltage drop corresponds to the droop resistance (R_O).

The output current is measured by low−pass filtering the voltage across the inductor or current sense resistor. The filter is implemented by the CS amplifier that is configured with R_{PH}, R_{CS}, and C_{CS}. The output resistance of the regulator is set by the following equations:

$$R_O \approx \frac{R_{CS}}{R_{PH(x)}} \times R_{SENSE} \quad \text{(eq. 10)}$$

$$C_{CS} \approx \frac{L}{R_{SENSE} \times R_{CS}} \quad \text{(eq. 11)}$$

where R_{SENSE} is the DCR of the output inductors.

Either R_{CS} or R_{PH} can be chosen for added flexibility. Due to the current drive ability of the CSCOMP pin, the R_{CS} resistance should be greater than 100 k . For example, initially select R_{CS} to be equal to 200 k , and then use Equation 11 to solve for C_{CS}:

$$C_{CS} \approx \frac{560\ nH}{1.3\ m\ \ 200\ k} \approx 2.2\ nF \quad \text{(eq. 12)}$$

If C_{CS} is not a standard capacitance, R_{CS} can be tuned. In this case, the required C_{CS} is a standard value and no tuning is required. For best accuracy, C_{CS} should be a 5% NPO capacitor.

Next, solve for R_{PH} by rearranging Equation 10 as follows:

$$R_{PH} \approx \frac{1.3\ m}{5.1\ m} \times 200\ k\ \ 51.0\ k \quad \text{(eq. 13)}$$

The standard 1% resistor for R_{PH} is 51.1 k .

Inductor DCR Temperature Correction

If the DCR of the inductor is used as a sense element and copper wire is the source of the DCR, the temperature changes associated with the inductor's winding must be compensated for. Fortunately, copper has a well−known temperature coefficient (TC) of 0.39%/°C.

If R_{CS} is designed to have an opposite but equal percentage of change in resistance, it cancels the temperature variation of the inductor's DCR. Due to the nonlinear nature of NTC thermistors, series resistors R_{CS1} and R_{CS2} (see Figure 25) are needed to linearize the NTC and produce the desired temperature coefficient tracking.

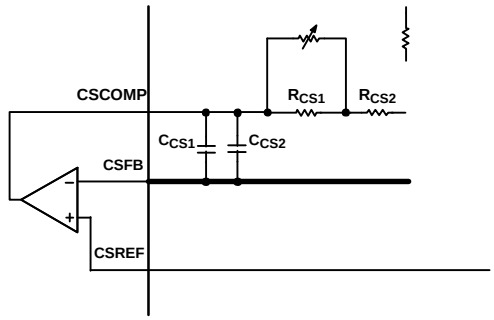

Figure 25. Temperature−Compensation Circuit Values

provides an approximate value for the switching loss per main MOSFET:

$$P_{S(MF)} \approx 2 \cdot f_{SW} \cdot \frac{V_{DC} \cdot I_O}{n_{MF}} \cdot R_G \cdot n_{MF} \cdot C_{ISS} \quad \text{(eq. 22)}$$

where:
n_{MF} is the total number of main MOSFETs.
R_G is the total gate resistance.
C_{ISS} is the input capacitance of the main MOSFET.

The most effective way to reduce switching loss is to use lower gate capacitance devices.

where:
R_{LIM} is the current limit resistor. R_{LIM} is connected from the ILIM pin to ground.
R_O is the output load line resistance.
I_{LIM} is the current limit set point. This is the peak inductor current that will trip current limit.

Current Monitor

The ADP3209D has output current monitor. The IMON pin sources a current proportional to the total inductor current. A resistor, R_{MON}, from IMON to FBRTN sets the gain of the output current monitor. A 0.1 F is placed in parallel with R_{MON} to filter the inductor current ripple and high frequency load transients. Since the IMON pin is connected directly to the CPU, it is clamped to prevent it from going above 1.15V.

The IMON pin current is equal to the R_{LIM} times a fixed gain of 10. R_{MON} can be found using the following equation:

$$R_{MON} = \frac{1.15\ V \cdot R_{LIM}}{10 \cdot R_O \cdot I_{FS}} \quad \text{(eq. 29)}$$

where:
R_{MON} is the current monitor resistor. R_{MON} is connected from IMON pin to FBRTN.
R_{LIM} is the current limit resistor.
R_O is the output load line resistance.
I_{FS} is the output current when the voltage on IMON is at full scale.

Feedback Loop Compensation Design

Optimized compensation of the ADP3209D allows the best possible response of the regulator's output to a load change. The basis for determining the optimum compensation is to make the regulator and output decoupling appear as an output impedance that is entirely resistive over the widest possible frequency range, including dc, and that is equal to the droop resistance (R_O). With the resistive output impedance, the output voltage droops in proportion with the load current at any load current slew rate, ensuring the optimal position and allowing the minimization of the output decoupling.

With the multi−mode feedback structure of the ADP3209D, it is necessary to set the feedback compensation so that the converter's output impedance works in parallel with the output decoupling. In addition, it is necessary to compensate for the several poles and zeros created by the output inductor and decoupling capacitors (output filter).

A Type III compensator on the voltage feedback is adequate for proper compensation of the output filter. Figure 26 shows the Type III amplifier used in the ADP3209D. Figure 27 shows the locations of the two poles and two zeros created by this amplifier.

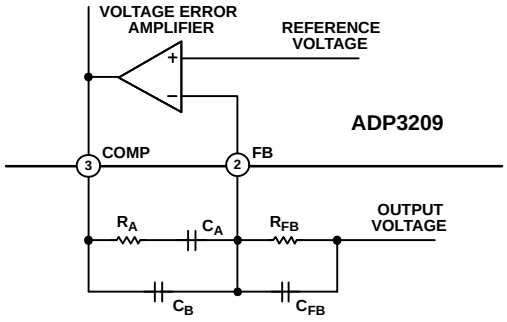

Figure 26. Voltage Error Amplifier

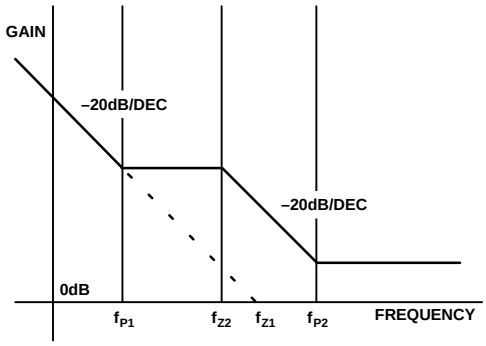

Figure 27. Poles and Zeros of Voltage Error Amplifier

The following equations give the locations of the poles and zeros shown in Figure 27:

$$f_{Z1} = \frac{1}{2 \cdot C_A \cdot R_A} \quad \text{(eq. 30)}$$

$$f_{Z2} = \frac{1}{2 \cdot C_{FB} \cdot R_{FB}} \quad \text{(eq. 31)}$$

$$f_{P1} = \frac{1}{2 \cdot (C_A \cdot C_B) \cdot R_{FB}} \quad \text{(eq. 32)}$$

$$f_{P2} = \frac{C_A \cdot C_B}{2 \cdot R_A \cdot C_B \cdot C_A} \quad \text{(eq. 33)}$$

The expressions that follow compute the time constants for the poles and zeros in the system and are intended to yield an optimal starting point for the design; some adjustments may be necessary to account for PCB and component parasitic effects (see the Tuning Procedure for ADP3209D section):

$$R_E = R_O \cdot A_D \cdot R_{DS} \cdot \frac{R_L \cdot V_{RT}}{V_{ID}} \cdot \frac{2 \cdot L \cdot (1}{} \quad \text{(eq. 34)}$$

$$T_A = C_X \times (R_O + R') \times \frac{L_X}{R_O} \times \frac{R_O + R'}{R_X} \quad \text{(eq. 35)}$$

$$T_B = (R_X + R' + R_O) \times C_X \quad \text{(eq. 36)}$$

$$T_C = \frac{V_{RT} \times \left[L \times \frac{A_D \times R_{DS}}{2 \times f_{SW}}\right]}{V_{VID} \times R_E} \quad \text{(eq. 37)}$$

$$T_D = \frac{C_X \times C_Z \times R_O^{\,2}}{C_X \times (R_O + R') \times C_Z \times R_O} \quad \text{(eq. 38)}$$

where:

R’ is the PCB resistance from the bulk capacitors to the ceramics and is approximately 0.4 m (assuming an 8−layer motherboard).

R_{DS}

7. Measure the output ripple with no load and with a full load with scope, making sure both are within the specifications.

Set the AC Load Line

1. Remove the dc load from the circuit and connect a dynamic load.
2. Connect the scope to the output voltage and set it to dc coupling mode with a time scale of 100 s/div.
3. Set the dynamic load for a transient step of about 40 A at 1 kHz with 50% duty cycle.
4. Measure the output waveform (note that use of a dc offset on the scope may be necessary to see the waveform). Try to use a vertical scale of 100 mV/div or finer.
5. The resulting waveform will be similar to that shown in Figure 28. Use the horizontal cursors to measure V_{ACDRP} and V_{DCDRP}, as shown in Figure 28. Do not measure the undershoot or overshoot that occurs immediately after the step.

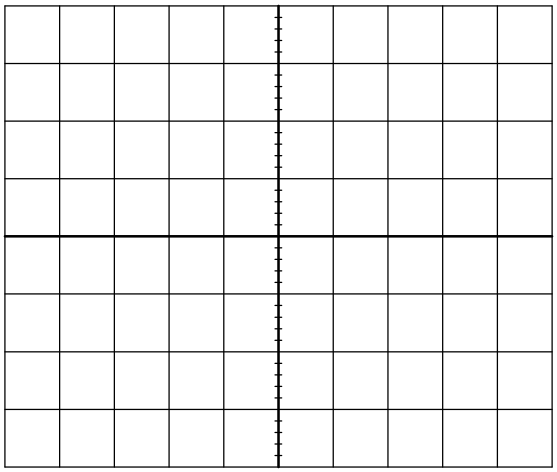

Figure 28. AC Load Line Waveform

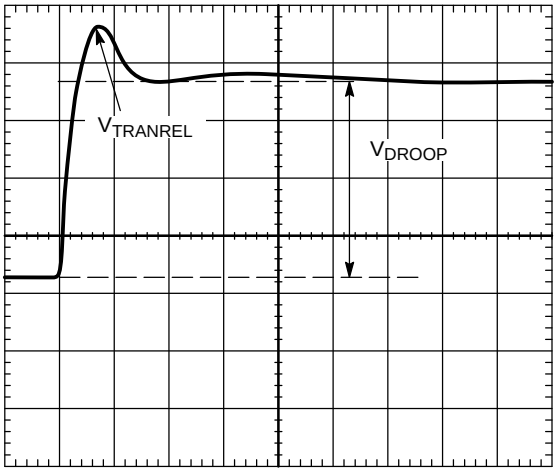

Figure 30. Transient Setting Waveform, Load Release

Layout and Component Placement

The following guidelines are recommended for optimal performance of a switching regulator in a PC system.

General Recommendations

1. For best results, use a PCB of four or more layers. This should provide the needed versatility for control circuitry interconnections with optimal placement; power planes for ground, input, and output; and wide interconnection traces in the rest of the power delivery current paths. Keep in mind