# ADP3210

**ELECTRICAL CHARACTERISTICS** $V_{CC}$ = 5.0 V, FBRTN = GND, EN = $V_{CC}$, $V_{VID}$ = 1.20 V to 1.500 V, $\overline{PSI}$ = 1.1 V, DPRSLP = GND, LLINE = CSREF, Current going into pin is positive. $T_A$ = −10°C to 100°C, unless otherwise noted. (Note 1) $R_{REF}$ = 80 kΩ

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **VOLTAGE CONTROL − Voltage Error Amplifier (VEAMP)** | | | | | | |
| FB, LLINE Voltage Range (Note 2) | $V_{FB}$, $V_{LLINE}$ | Relative to CSREF = $V_{DAC}$ | −200 | | +200 | mV |
| FB, LLINE Offset Voltage (Note 2) | $V_{OSVEA}$ | Relative to CSREF = $V_{DAC}$ | −0.5 | | +0.5 | mV |
| FB Bias Current | $I_{FB}$ | | −1.0 | | 1.0 | A |
| LLINE Bias Current | $I_{LL}$ | | −50 | | 50 | nA |
| LLINE Positioning Accuracy | $V_{FB}$ − $V_{VID}$ | Measured on FB relative to $V_{VID}$, LLINE forced 80 mV below CSREF | −82 | −80 | −78 | mV |
| COMP Voltage Range (Note 2) | $V_{COMP}$ | | 0.85 | | 4.0 | V |
| COMP Current (Note 2) | $I_{COMP}$ | COMP = 2.0 V, CSREF = $V_{DAC}$<br>FB forced 80 mV below CSREF<br>FB forced 80 mV above CSREF | | <br>−0.75<br>10 | | mA |
| COMP Slew Rate (Note 2) | $SR_{COMP}$ | $C_{COMP}$ = 10 pF, CSREF = $V_{DAC}$<br>FB forced 200 mV below CSREF<br>FB forced 200 mV above CSREF | | <br>15<br>−2015 | | |

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| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **VOLTAGE MONITORING AND PROTECTION – Power Good** | | | | | | |
| PWRGD Masking Time | | Triggered by any VID change or OCP event | | 100 | | s |
| CSREF Soft−Stop Resistance | | EN = L or Latchoff condition | | 50 | | Ω |
| **CURRENT CONTROL – Current Sense Amplifier (CSAMP)** | | | | | | |
| CSSUM, CSREF Common−Mode Range (Note 2) | | | 0.05 | | 3.5 | V |
| CSSUM, CSREF Offset Voltage | $V_{OSCSA}$ | CSREF − CSSUM, $T_A$ = 25°C<br>$T_A$ = −10°C to 85°C | −0.3<br>−1.2 | | +0.3<br>+1.2 | mV |

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| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **THERMAL MONITORING AND PROTECTION** | | | | | | |
| TTSENSE Threshold | | $V_{CC}$ = 5.0 V, TTSNS is falling | 2.45 | 2.5 | 2.55 | V |
| TTSENSE Hysteresis | | | 50 | 95 | | mV |
| TTSENSE Bias Current | | TTSENSE = 2.6 V | −2.0 | | 2.0 | A |
| VRTT Output Voltage | $V_{VRTT}$ | Logic Low, $I_{VRTT(SINK)}$ = 400 A<br>Logic High, $I_{VRTT(SOURCE)}$ = −400 A | <br>4.0 | 10<br>5.0 | 100 | mV<br>V |
| **SUPPLY** | | | | | | |
| Supply Voltage Range | $V_{CC}$ | | 4.5 | | 5.5 | V |
| Supply Current | | EN = H<br>EN = 0 V | | 8.0<br>10 | 11<br>50 | mA<br>A |
| $V_{CC}$ OK Threshold | $V_{CCOK}$ | $V_{CC}$ is Rising | | 4.4 | 4.5 | V |
| $V_{CC}$ UVLO Threshold | $V_{CCUVLO}$ | $V_{CC}$ is Falling | 4.0 | 4.15 | | V |
| $V_{CC}$ Hysteresis (Note 2) | | | | 150 | | mV |

1. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC).
2. Guaranteed by design or bench characterization, not production tested.

**Figure 2. Closed−Loop Output Voltage Accuracy**

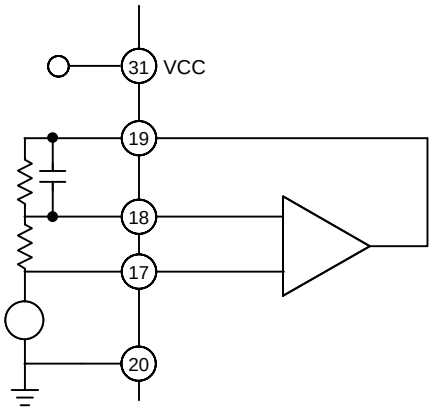



**Figure 3. Current Sense Amplifier $V_{OS}$**

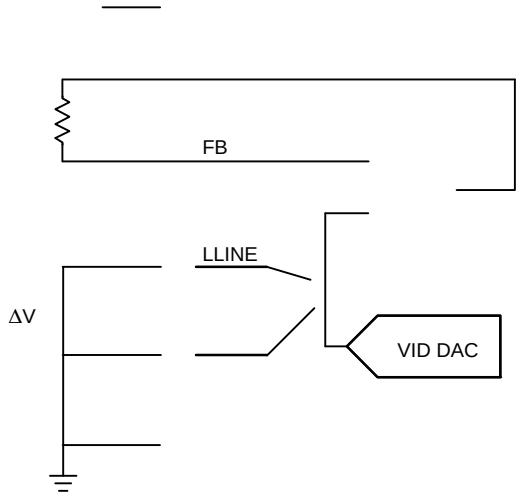



**Figure 4. Positioning Accuracy**

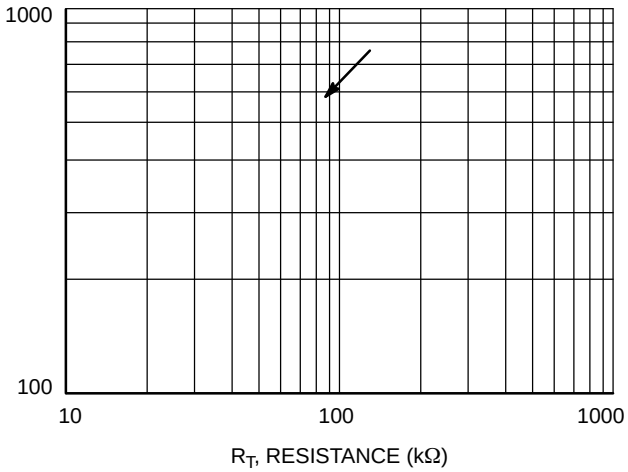



**Figure 5. Master Clock Frequency vs. $R_T$**

**Figure 6. Master Clock vs. VID**

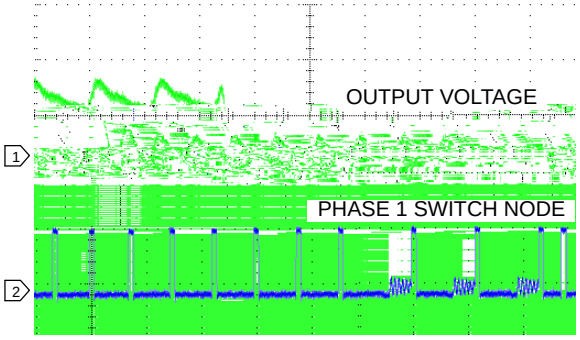
**Figure 7. Load Line Accuracy**

**Figure 8. Startup Waveforms**

**Figure 9. Load Transient with 2−Phases**

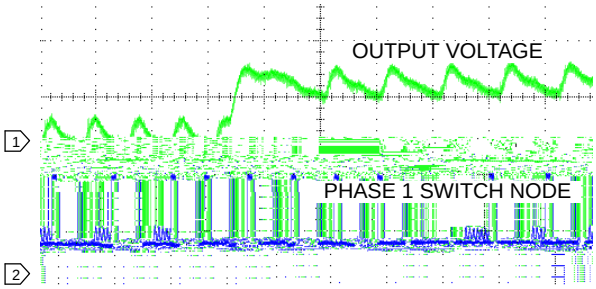
**Figure 10. Load Transient with 2−Phases**

## TYPICAL CHARACTERISTICS



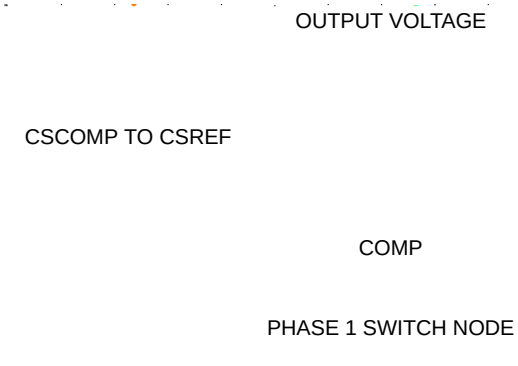

**1:** 50 mV / div **2:** 10 V / div 4 s / div
Input = 12 V, Output = 1.0 V
3.0 A to 15 A Load Step

**Figure 11. Load Transient with 1−Phase**



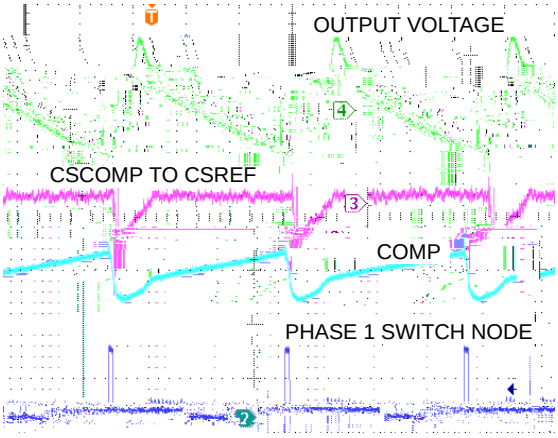

**1:** 50 mV / div **2:** 10 V / div 4 s / div
Input = 12 V, Output = 1.0 V
15 A to 3.0 A Load Step

**Figure 12. Load Transient with 1−Phase**



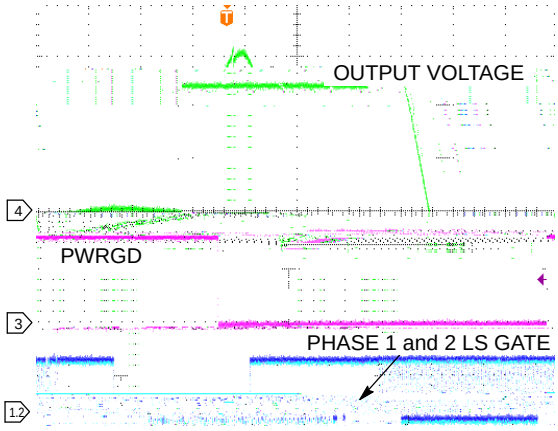

**1:** 10 V / div **3:** 20 mV / div 1 s / div
**2:** 0.5 V / div **4:** 5.0 mV / div
Input = 12 V, Output = 1.0 V
2−Phase

**Figure 13. Switching Waveforms**



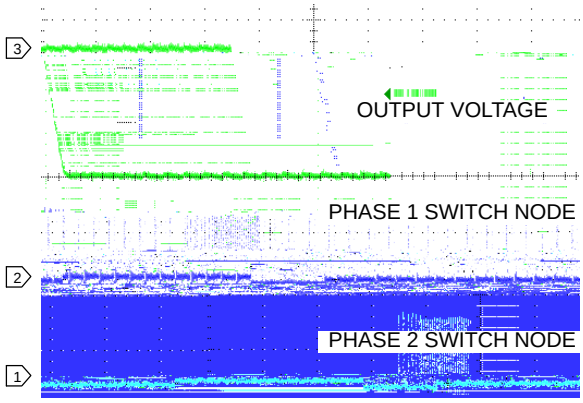

**1:** 10 V / div **3:** 20 mV / div 4 s / div
**2:** 0.5 V / div **4:** 5.0 mV / div
Input = 12 V, Output = 1.0 V
Single−Phase DCM, 1.0 A

**Figure 14. Switching Waveforms**




**1:** 5.0 V / div **3:** 2.0 V / div 40 s / div
**2:** 5.0 V / div **4:** 0.5 V / div
Input = 12 V, Output = 1.0 V
FB shortened to GND

**Figure 15. OVP and RVP Test**




**1:** 10 V / div **2:** 10 V / div **3:** 200 mV / div 100 s / div
Input = 12 V, Output = 0.5 A
1.2 V to 0.7 V VID Step
$\overline{\text{PSI}}$ = High, DPRSLP = High

**Figure 16. VID Step**

## TYPICAL CHARACTERISTICS

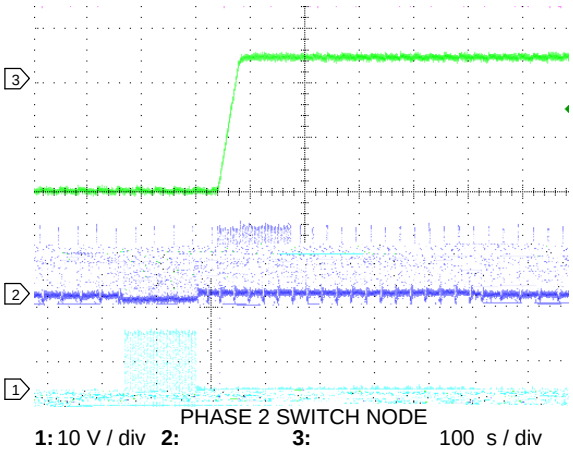



Figure 17. VID Step

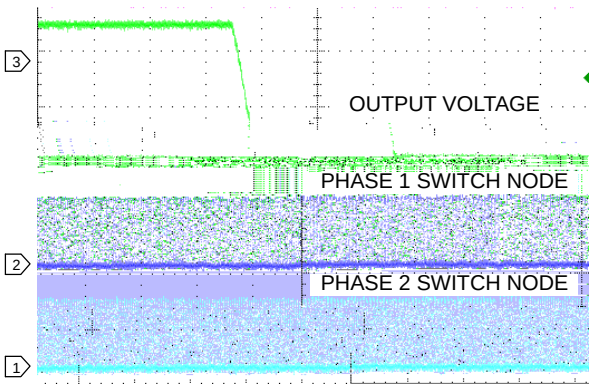



Figure 18. VID Step

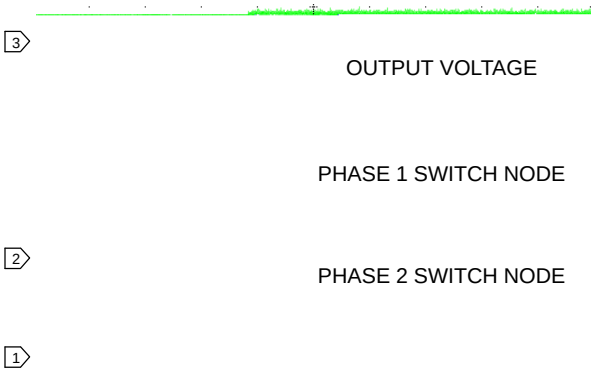



Figure 19. VID Step

### Theory of Operation

The ADP3210 combines a multi−mode PWM Ramp Pulse Modulated (RPM) control with multiphase logic outputs for use in 1−, 2−, and 3−phase synchronous buck CPU core supply power converters. The internal 7−bit VID DAC conforms to Intel IMVP−6.5 specifications. Multiphase operation is important for producing the high currents and low voltages demanded by today's microprocessors. Handling high currents in a single−phase converter puts high thermal stress on the system components such as the inductors and MOSFETs.

The multi−mode control of the ADP3210 ensures a stable high performance topology for:

- Balancing currents and thermals between phases
- High speed response at the lowest possible switching frequency and minimal output decoupling
- Minimizing thermal switching losses due to lower frequency operation
- Tight load line regulation and accuracy
- High current output by supporting up to 3−phase operation
- Reduced output ripple due to multiphase ripple cancellation
- High power conversion efficiency both at heavy load and light load
- PC board layout noise immunity
- Ease of use and design due to independent component selection
- Flexibility in operation by allowing optimization of design for low cost or high performance

### Number of Phases

The number of operational phases and their phase relationship is determined by internal circuitry that monitors the PWM outputs. Normally, the ADP3210 operates as a 3−phase

**Table 1. Phase Number and Operation Modes**

| $\overline{\text{PSI}}$ | DPRSLP | VID Transient Period (Note 1) | Hit Current |
|---|---|---|---|

### Output Current Sensing

The ADP3210 provides a dedicated Current Sense Amplifier (CSA) to monitor the total output current of the converter for proper voltage positioning vs. load current, and for current limit detection. Sensing the load current being delivered to the load is inherently more accurate than detecting peak current or sampling the current across a sense element, such as the low−side MOSFET. The CSA can be configured several ways depending on system requirements.

Output inductor DCR sensing without use of a thermistor for lowest cost

Output inductor DCR sensing with use of a thermistor that tracks inductor temperature to improve accuracy

Discrete resistor sensing for highest accuracy

The positive input of the CSA is connected to the CSREF pin, which is connected to the output voltage. At the negative

controller. Logic high level indicates that the output voltage is within the voltage limits defined by a window around the VID voltage setting. PWRGD goes low when the output voltage is outside of that window.

Following the IMVP−6.5 specification, PWRGD window is defined as −300 mV below and +200 mV above the actual VID DAC output voltage. For any DAC voltage below 300 mV, only the upper limit of the PWRGD window is monitored. To prevent false alarm, the power−good circuit is masked during various system transitions, including any VID change and entrance/exit out of deeper sleep. The duration of the PWRGD mask time is set by an internal clock to approximately 100 s.

During a VID change, the PWRGD signal is masked to prevent false PWRGD glitches. The PWRGD is masked for approximately 100 s after a VID change.

### Powerup Sequence and Soft−Start

The power−on ramp−up time of the output voltage is set internally. During startup, the ADP3210 steps sequentially through each VID code until it reaches the boot voltage. The whole powerup sequence, including soft−

An inherent per phase current limit protects individual phases in case one or more phases stop functioning because of a faulty component. This limit is based on the maximum normal−mode COMP voltage.

After 9 ms in current limit, the ADP3210 will latchoff. The latchoff can be reset by removing and reapplying $V_{CC}$, or by recycling the EN pin low and high for a short time.

### Changing VID OTF

The ADP3210 is designed to track dynamically changing VID code. As a result, the converter output voltage, that is, the CPU $V_{CC}$ voltage, can change without the need to reset either the controller or the CPU. This concept is commonly referred to as VID OTF transient. A VID OTF can occur either under light load or heavy load conditions. The processor signals the controller by changing the VID inputs in LSB incremental steps from the start code to the finish code. The change can be either upwards or downwards steps.

When a VID input changes state, the ADP3210 detects the change but ignores the new code for a minimum of time of 400 ns. This keep out is required to prevent reaction to false code that can occur by a skew in the VID code while the 7−bit VID input code is in transition. Additionally, the VID change triggers a PWRGD masking timer to prevent a PWRGD failure. Each VID change resets and re−triggers the internal PWRGD masking timer. As listed in Table 2, during any VID transient, the ADP3210 forces a multiphase PWM mode regardless of system input signals.

### Output Crowbar

To protect the CPU load and output components of the converter, the PWM outputs are driven low, $\overline{\text{DCM1}}$ and $\overline{\text{OD}}$ are driven high (that is, commanded to turn on the low−side MOSFETs of all phases) when the output voltage exceeds an OVP threshold of 1.55 V as specified by IMVP−6.5.

Turning on the low−side MOSFETs discharges the output capacitor as soon as reverse current builds up in the inductors. If the output overvoltage is due to a short of the high−side MOSFET, then this crowbar action current limits the input supply or causes the input rail fuse to blow, protecting the microprocessor from destruction.

Once overvoltage protection (OVP) is triggered, the ADP3210 is latched off. The latchoff function can be reset by removing and reapplying $V_{CC}$, or by recycling EN low and high for a short time.

### Reverse Voltage Protection

Very large reverse currents in inductors can cause negative $V_{CORE}$

**Table 2. VID Code Table**

| VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | Output (V) |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0.4000 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0.3875 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0.3750 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0.3625 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0.3500 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0.3375 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0.3250 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0.3125 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0.3000 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0.2875 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0.2750 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0.2625 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0.2500 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0.2375 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0.2250 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0.2125 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0.2000 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0.1875 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0.1750 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0.1625 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0.1500 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0.1375 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0.1250 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0.1125 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0.1000 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0.0875 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0.0750 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0.0625 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0.0500 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0.0375 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0.0250 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0.0125 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0.0000 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0.0000 |

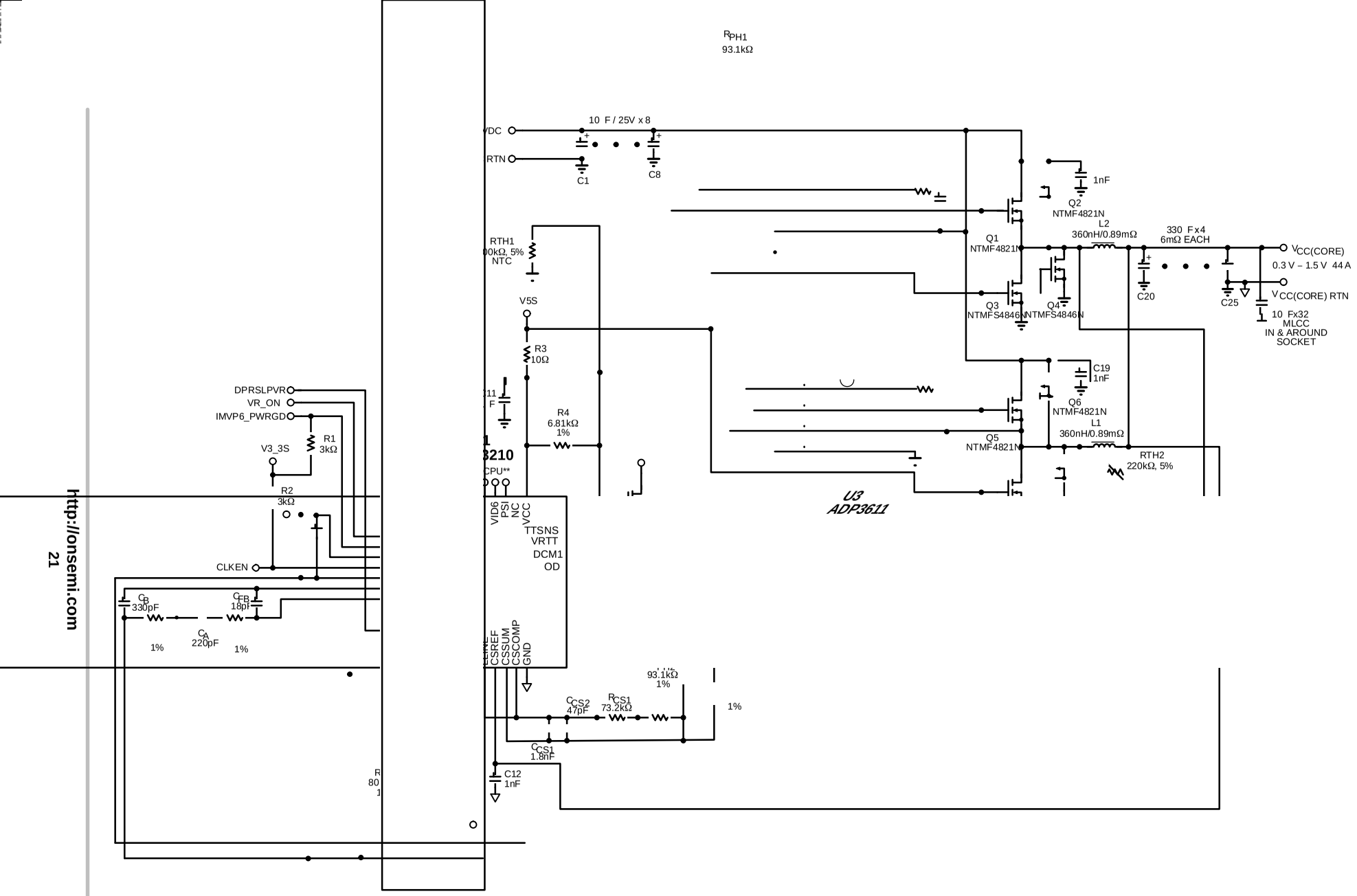



**Figure 24. Typical Application Circuit**

### Application Information

The design parameters for a typical Intel IMVP6.5−compliant CPU Core VR application are as follows: TT5

The output current is measured by summing the currents of the resistors monitoring the voltage across each inductor and by passing the signal through a low−pass filter. This summer−filter is implemented by the CS amplifier that is configured with resistors $R_{PH(X)}$ (summer), and $R_{CS}$ and $C_{CS}$ (filter). The output resistance of the regulator is set by the following equations, where $R_L$ is the DCR of the output inductors:

$$R_O = \frac{R_{CS}}{R_{PH(x)}} \times R_L \quad \text{(eq. 5)}$$

$$C_{CS} = \frac{L}{R_L \cdot R_{CS}} \quad \text{(eq. 6)}$$

Users have the flexibility of choosing either $R_{CS}$ or $R_{PH(X)}$. Due to the current drive ability of the CSCOMP pin, the $R_{CS}$ resistance should be larger than 100 kΩ. For example, users should initially select $R_{CS}$ to be equal to 220 kΩ, then use Equation 6 to solve for $C_{CS}$:

$$C_{CS} = \frac{360\ \text{nH}}{0.89\ \text{m}\Omega \times 220\ \text{k}\Omega} = 1.84\ \text{nF} \quad \text{(eq. 7)}$$

Because $C_{CS}$ is not the standard capacitance, it is implemented with two standard capacitors in parallel: 1.8 nF and 47 pF. For the best accuracy, $C_{CS}$ should be a 5% NPO capacitor. Next, solve $R_{PH(X)}$ by rearranging Equation 5.

$$R_{PH(X)} \geq \frac{0.89\ \text{m}\Omega}{2.1\ \text{m}\Omega} \quad \text{(eq. 8)}$$

6. Finally, calculate values for $R_{CS1}$ and $R_{CS2}$ using:

$$R_{CS1} = R_{CS} \times k \times r_{CS1}$$
$$R_{CS2} = R_{CS} \times ((1 - k) + (k \times r_{CS2})) \quad \text{(eq. 12)}$$

This example starts with a thermistor value of 100 kΩ and uses a Vishay NTHS0603N04 NTC thermistor (a 0603 size thermistor) with A = 0.3359 and B = 0.0771. From this data, $r_{CS1}$ = 0.359, $r_{CS2}$ = 0.729 and $r_{TH}$ = 1.094. Solving for $R_{TH}$ yields 240 kΩ, so 220 kΩ is chosen, making k = 0.914. Finally, $R_{CS1}$ and $R_{CS2}$ are 72.3 kΩ and 166 kΩ. Choosing the closest 1% resistor values yields a choice of 71.5 kΩ and 165 kΩ.

### $C_{OUT}$ Selection

The required output decoupling for processors and platforms is typically recommended by Intel. The following guidelines can also be used if both bulk and ceramic capacitors in the system:

Select the total amount of ceramic capacitance. This is based on the number and type of capacitors to be used. The best location for ceramics is inside the socket; 20 pieces of Size 0805 being the physical limit. Additional capacitors can be placed along the outer edge of the socket.

Select the number of ceramics and find the total ceramic capacitance ($C_Z$). Combined ceramic values of 200 F to 300 F are recommended and are usually made up of multiple 10 F or 22 F capacitors.

Note that there is an upper limit imposed on the total amount of bulk capacitance ($C_X$) when considering the

The maximum output current $I_O$ determines the $R_{DS(ON)}$ requirement

where:
$A_R$ is the internal ramp amplifier gain.
$A_D$ is the current balancing amplifier gain.
$R_{DS}$ is the total low−side MOSFET ON−resistance,
$C_R$ is the internal ramp capacitor value.

Another consideration in the selection of $R_R$ is the size of the internal ramp voltage (see Equation 23). For stability and noise immunity, keep this ramp size larger than 0.5 V. Taking this into consideration, the value of $R_R$ is selected as 280 kΩ.

The internal ramp voltage magnitude can be calculated using:

$$V_R = \frac{A_R \times (1 - D) \times V_{VID}}{R_R \times C_R \times f_{SW}} \quad \text{(eq. 23)}$$

$$V_R = \frac{0.5 \times (1 - 0.061) \times 1.150\ V}{462\ k\Omega \times 5\ pF \times 280\ kHz} = 0.83\ V$$

The size of the internal ramp can be made larger or smaller. If it is made larger, then stability and transient response improves, but thermal balance degrades. Likewise, if the ramp is made smaller, then thermal balance improves at the sacrifice of transient response and stability. The factor of three in the denominator of Equation 22 sets a minimum ramp size that gives an optimal balance for good stability, transient response, and thermal balance.

### Setting the Switching Frequency for RPM Mode Operation of Phase 1

During the RPM mode operation of Phase 1, the ADP3210 runs in pseudo constant frequency, given that the load current is high enough for continuous current mode. While in discontinuous current mode, the switching frequency is reduced with the load current in a linear manner. When considering power conversion efficiency in light load, lower switching frequency is usually preferred for RPM mode. However, the $V_{CORE}$ ripple specification in the IMVP−6 sets the limitation for lowest switching frequency. Therefore, depending on the inductor and output capacitors, the switching frequency in RPM mode can be equal, larger, or smaller than its counterpart in PWM mode.

A resistor from RPM to GND sets the pseudo constant frequency as following:

$$R_{RPM} = \frac{2 \times R_T}{V_{VID} + 1.0\ V} \times \frac{A_R \times (1 - D) \times V_{VID}}{R_R \times C_R \times f_{SW}} - 0.5\ k\Omega \quad \text{(eq. 24)}$$

where:
$A_R$ is the internal ramp amplifier gain.
$C_R$ is the internal ramp capacitor value.
$R_R$ is an external resistor on the RAMPADJ pin to set the internal ramp magnitude.

Because $R_R$ = 280 kΩ, the following resistance sets up 300 kHz switching frequency in RPM operation.

$$R_{RPM} = \frac{2 \times 280\ k\Omega}{1.150\ V + 1.0\ V} \times \frac{0.5 \times (1 - 0.061) \times 1.150}{462\ k\Omega \times 5\ pF \times 300\ kHz} - 500\ \Omega = 202\ k\Omega \quad \text{(eq. 25)}$$

### Current Limit Set−point

To select the current limit set−point, we need to find the resistor value for $R_{LIM}$. The current limit threshold for the ADP3210 is set when the current in $R_{LIM}$ is equal to the internal reference current of 20 A. The current in $R_{LIM}$ is equal to the inductor current times $R_O$. $R_{LIM}$ can be found using the following equation:

$$R_{LIM} = \frac{I_{LIM} \times R_O}{20\ A} \quad \text{(eq. 26)}$$

where:
$R_{LIM}$ is the current limit resistor. $R_{LIM}$ is connected from the $I_{LIM}$ pin to CSCOMP.
$R_O$ is the output load line resistance.
$I_{LIM}$ is the current limit set point. This is the peak inductor current that will trip current limit.

In this example, if choosing 55 A for $I_{LIM}$, $R_{LIM}$ is 5.775 kΩ, which is close to a standard 1% resistance of 5.76 kΩ.

The per−phase current limit described earlier has its limit determined by the following:

$$I_{PHLIM} \cong \frac{V_{COMP(MAX)} - V_R - V_{BIAS}}{A_D \times R_{DS(MAX)}} + \frac{I_R}{2} \quad \text{(eq. 27)}$$

For the ADP3210, the maximum COMP voltage ($V_{COMP(MAX)}$) is 3.3 V, the COMP pin bias voltage ($V_{BIAS}$) is 1.0 V, and the current balancing amplifier gain ($A_D$) is 5. Using a $V_R$ of 0.55 V, and a $R_{DS(MAX)}$ of 3.8 mΩ (low−side on−resistance at 150°C) results in a per−phase limit of 85 A. Although this number seems high, this current level can only be reached with a absolute short at the output and the current limit latchoff function shutting down the regulator before overheating occurs.

This limit can be adjusted by changing the ramp voltage $V_R$. However, users should not set the per−phase limit lower than the average per−phase current ($I_{LIM}$/n).

There is also a per−phase initial duty−cycle limit at maximum input voltage:

$$D_{LIM} = D_{MIN} \times V_{COMP(MAX)} - \text{Vr0187 0 08.660o.dDa54c1.22,R0 0 7} \quad \text{(eq. 28)}$$

where:
$R_{MON}$

Where $R_{Snubber}$ is the snubber resistor.
$C_{Snubber}$ is the snubber capacitor.
$f_{Rininging}$ is the frequency of the ringing on the switch node when the high side MOSFET turns on.
$C_{OSS}$ is the low side MOSFET output capacitance at $V_{Input}$. This is taken from the low side MOSFET data sheet.
$V_{Input}$ is the input voltage.
$f_{Switching}$ is the switching frequency.
$P_{Snubber}$ is the power dissipated in $R_{Snubber}$.

### Selecting Thermal Monitor Components

For single−point hot spot thermal monitoring, simply set $R_{TTSET1}$ equal to the NTC thermistor's resistance at the alarm temperature (see Figure 26). For example, if the $\overline{VRTT}$ alarm temperature is 100°C using a Vishey thermistor (NTHS−0603N011003J) with a resistance of 100 kΩ at 25°C, and 6.8 kΩ at 100°C, simply set $R_{TTSET1} = R_{TH1}(100°C)$ to TH1

**AC Loadline Setting**

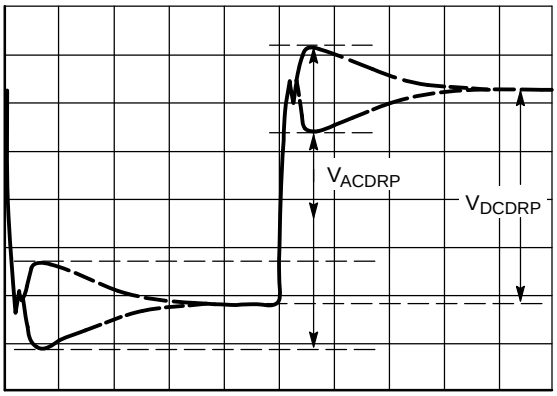



**Figure 28. AC Load Line Waveform**

11. Remove the dc load from the circuit and hook up the dynamic load.
12. Hook up the scope to the output voltage and set it to dc coupling with the time scale at 100 s/div.
13. Set the dynamic load for a transient step of about 40 A at 1 kHz with a 50% duty cycle.
14. Measure the output waveform (using the dc offset on scope to see the waveform, if necessary). Try to use the vertical scale of 100 mV/div or finer.
15. Users should see a waveform that similar to the one in Figure 29. Use the horizontal cursors to measure $V_{ACDRP}$ and $V_{DCDRP}$ as shown. Do not measure the undershoot or overshoot that occurs immediately after the step.
16. If the $V_{ACDRP}$ and $V_{DCDRP}$ are different by more than a couple of mV, use the following to adjust $C_{CS}$ (note that users may need to parallel different values to get the right one due to the limited standard capacitor values available. It is also wise to have locations for two capacitors in the layout for this):

$$C_{CS(NEW)} = C_{CS(OLD)} \times \frac{V_{ACDRP}}{V_{DCDRP}} \quad \text{(eq. 46)}$$

17. Repeat Steps15 and Step 16. Repeat adjustments if necessary. Once complete, do not change $C_{CS}$ for the rest of the procedure.
18. Set dynamic load step to maximum step size. Do not use a step size larger than needed. Verify that the output waveform is square, which means $V_{ACDRP}$ and $V_{DCDRP}$ are equal.
    Note: Make sure that the load step slew rate and turn−on are set for a slew rate of ~150 A/ s to 250 A/ s (for example, a load step of 50 A should take 200 ns to 300 ns) with no overshoot. Some dynamic loads have an excessive turn−on overshoot if a minimum current is not set properly (this is an issue if you are using a VTT tool).

**Initial Transient Setting**

19. With dynamic load still set at the maximum step size, expand the scope time scale to see 2 s/div to 5 s/div. A waveform that has two overshoots and one minor undershoot can result (see Figure 29). Here, $V_{DROOP}$ is the final desired value.

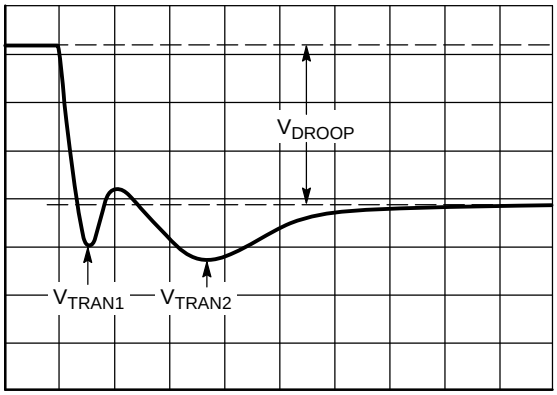



**Figure 29. Transient Setting Waveform, Load Step**

20. If both overshoots are larger than desired, make the following adjustments in the order they appear. Note that if these adjustments do not change the response, then users are limited by the output decoupling. In addition, check the output response each time a change is made, as well as the switching nodes to make sure they are still stable.

Make ramp resistor larger by 25% ($R_{RAMP}$).

For $V_{TRAN1}$, increase $C_B$ or increase switching frequency.

For $V_{TRAN2}$, increase $R_A$ and decrease $C_A$

Connect the feedback traces from the switch nodes as close as possible to the inductor. The CSREF signal should be Kelvin connected to the center point of the copper bar, which is the $V_{CORE}$ common node for the inductors of all phases.

In the back side of the ADP3210 package, a metal pad can be used as the device heat sink. In addition, running vias under the ADP3210 is not recommended because the metal pad can cause shorting between vias.

**ORDERING INFORMATION**

| Device Number | Temperature Range | Package | Shipping† |
|---|---|---|---|
| ADP3210MNR2G | – | | |

**QFN40 6x6, 0.5P**

**SCALE 2:1**