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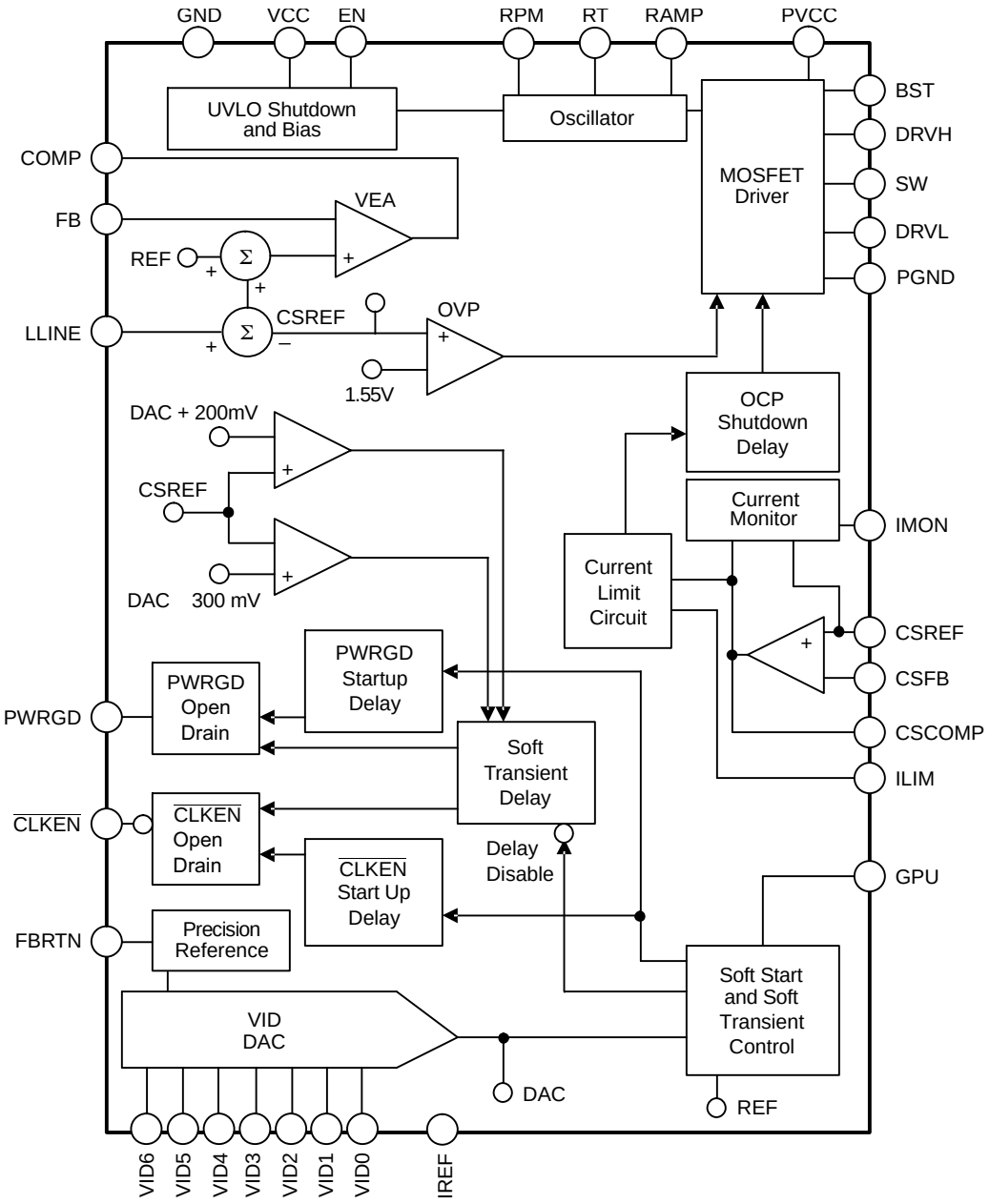


Figure 1. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
V_{CC}	0.3 to +6.0	V
FBRTN, PGND	0.3 to +0.3	V
BST, DRVH DC t < 200 ns	 0.3 to +28 0.3 to +33	V
BST to PV_{CC} DC t < 200 ns	 0.3 to +22 0.3 to +28	V
BST to SW	0.3 to +6.0	V
SW DC t < 200 ns	 1.0 to +22 6.0 to +28	V
DRVH to SW	0.3 to +6.0	V
DRVL to PGND DC t < 200 ns	 0.3 to +6.0 5.0 to +6.0	V
RAMP (in Shutdown) DC t < 200 ns	 0.3 to +22 0.3 to +26	V
All Other Inputs and Outputs	0.3 to +6.0	V
Storage Temperature Range	65 to +150	°C
Operating Ambient Temperature Range	40 to 100	°C
Operating Junction Temperature	125	°C
Thermal Impedance (θ_{JA}) 2 Layer Board	32.6	°C/W
Lead Temperature Soldering (10 sec) Infrared (15 sec)	 300 260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	PWRGD	Power Good Output. Open drain output. A low logic state means that the output voltage is outside of the VID DAC defined range.
2	IMON	Current Monitor Output. This pin sources current proportional to the output load current. A resistor connected to FBRTN sets the current monitor gain.
3	$\overline{\text{CLKEN}}$	Clock Enable Output. Open drain output. The pull high voltage on this pin cannot be higher than VCC.
4	FBRTN	Feedback Return Input/Output. This pin remotely senses the GMCH voltage. It is also used as the ground return for the VID DAC and the voltage error amplifier blocks.
5	FB	Voltage Error Amplifier Feedback Input. The inverting input of the voltage error amplifier.
6	COMP	Voltage Error Amplifier Output and Frequency Compensation Point.
7	GPU	GMCH/CPU select pin. Connect to ground when powering the CPU. Connect to 5.0 V when powering the GMCH. When GPU is connected to ground, the boot voltage is 1.1 V for the ADP3211 and 1.2 V for the ADP3211A. When GPU is connected to 5.0 V, there is no boot voltage.
8	ILIM	Current Limit Set pin. Connect a resistor between ILIM and CSCOMP to the current limit threshold.
9	IREF	This pin sets the internal bias currents. A 80 kΩ is connected from IREF to ground.
10	RPM	RPM Mode Timing Control Input. A resistor is connected from RPM to ground sets the RPM mode turn on threshold voltage.
11	RT	PWM Oscillator Frequency Setting Input. An external resistor from this pin to GND sets the PWM oscillator frequency.
12	RAMP	PWM Ramp Slope Setting Input. An external resistor from the converter input voltage node to this pin sets the slope of the internal PWM stabilizing ramp.
13	LLINE	Load Line Programming Input. The center point of a resistor divider connected between CSREF and CSCOMP tied to this pin sets the load line slope.
14	CSREF	Current Sense Reference Input. This pin must be connected to the opposite side of the output inductor.
15	CSFB	Non inverting Input of the Current Sense Amplifier. The combination of a resistor from the switch node to this pin and the feedback network from this pin to the CSCOMP pin sets the gain of the current sense amplifier.
16	CSCOMP	Current Sense Amplifier Output and Frequency Compensation Point.
17	GND	Analog and Digital Signal Ground.
18	PGND	Low Side Driver Power Ground. This pin should be connected close to the source of the lower MOSFET(s).
19	DRVL	Low Side Gate Drive Output.
20	PVCC	Power Supply Input/Output of Low Side Gate Driver.
21	SW	Current Return For High Side Gate Drive.
22	DRVH	High Side Gate Drive Output.
23	BST	High Side Bootstrap Supply. A capacitor from this pin to SW holds the bootstrapped voltage while the high side MOSFET is on.
24	VCC	Power Supply Input/Output of the Controller.
25 to 31	VID6 to VID0	Voltage Identification DAC Inputs. A 7 bit word (the VID Code) pro 0 8 Output.

ELECTRICAL CHARACTERISTICS (V_{CC} = PV_{CC} = 5.0 V, FBRTN = GND = PGND = 0 V, H = 5.0 V, L = 0 V, V_{VID} = V_{DAC} = 1.2 V, T_A = 40°C to 100°C, unless otherwise noted. (Note 1) Current entering a pin (sunk by the device) has a positive sign.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VOLTAGE CONTROL − Voltage Error Amplifier (VEAMP)						
FB, LLINE Voltage Range (Note 2)	V_{FB}, V_{LLINE}	Relative to CSREF = V_{DAC}	200		+200	mV
FB, LLINE Offset Voltage (Note 2)	V_{OSVEA}	Relative to CSREF = V_{DAC}	0.5		+0.5	mV
FB Bias Current	I_{FB}		1.0		+1.0	μA
LLINE Bias Current	I_{LL}		50		+50	nA
LLINE Positioning Accuracy	V_{FB} V_{DAC}					

ELECTRICAL CHARACTERISTICS (V_{CC} = PV_{CC} = 5.0 V, FBRTN = GND = PGND = 0 V, H = 5.0 V, L = 0 V, V_{VID} = V_{DAC} = 1.2 V, $T_{A, V}$

ELECTRICAL CHARACTERISTICS (V_{CC} = PV_{CC} = 5.0 V, FBRTN = GND = PGND = 0 V, H = 5.0 V, L = 0 V, V_{VID} = V_{DAC} = 1.2 V, T_A = 40°C to 100°C, unless otherwise noted. (Note 1) Current entering a pin (sunk by the device) has a positive sign.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
PULSE WIDTH MODULATOR − Clock Oscillator						
R_T Voltage	V_{RT}	R_T = 243 kΩ, V_{VID} = 1.2 V See also $V_{RT}(V_{VID})$ formula	1.08	1.2	1.35	V
PWM Clock Frequency Range (Note 2)	f_{CLK}	Operation of interest	0.3		3.0	MHz
RAMP GENERATOR						
RAMP Voltage	V_{RAMP}	EN = H, I_{RAMP} = 60 μA EN = L	0.9	1.0 V		

ELECTRICAL CHARACTERISTICS (V_{CC} = PV_{CC} = 5.0 V, FBRTN = GND = PGND = 0 V, H = 5.0 V, L = 0 V, V_{VID} = V_{DAC} = 1.2 V, T_A = 40°C to 100°C, unless otherwise noted. (Note 1) Current entering a pin (sunk by the device) has a positive sign.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
HIGH−SIDE MOSFET DRIVER						
Pullup Resistance, Sourcing Current Pulldown Resistance, Sinking Current		BST = PV_{CC}		2.0 1.0	3.3 2.8	Ω
Transition Times	tr_{DRVH}, tf_{DRVH}	BST = PV_{CC}, C_L = 3 nF, Figure 2		15 13	35 31	ns
Dead Delay Times	$tpdh_{DRVH}$	BST = PV_{CC}, Figure 2		10	45	ns
BST Quiescent Current		EN = L (Shutdown) EN = H, No Switching		5.0 200	15	μA
LOW−SIDE MOSFET DRIVER						
Pullup Resistance, Sourcing Current Pulldown Resistance, Sinking Current				1.8 0.9	3.0 2.7	Ω
Transition Times	tr_{DRVL}, tf_{DRVL}	C_L = 3 nF, Figure 2		15 14	35 35	ns
Propagation Delay Times	$tpdh_{DRVL}$	C_L = 3 nF, Figure 2		15	30	ns
SW Transition Timeout	t_{SWTO}	DRVH = L, SW = 2.5 V	150	250	450	ns
SW Off Threshold	V_{OFFSW}			2.2		V
PV_{CC} Quiescent Current		EN = L (Shutdown) EN = H, No Switching		14 200	50	μA

TYPICAL PERFORMANCE CHARACTERISTICS

V_{VID} = 1.5 V, T_A = 20°C to 100°C, unless otherwise noted.

TYPICAL PERFORMANCE CHARACTERISTICS

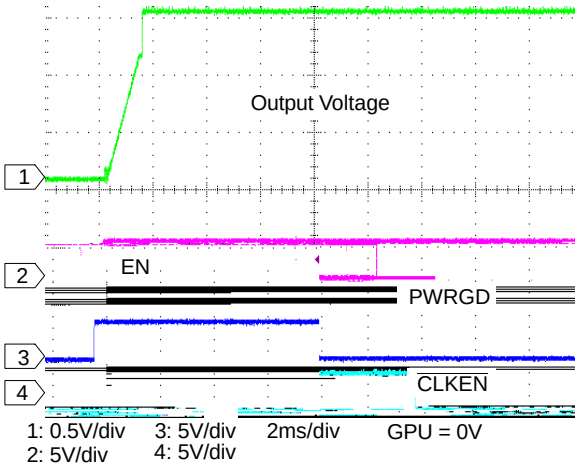


Figure 9. Startup Waveforms CPU Mode

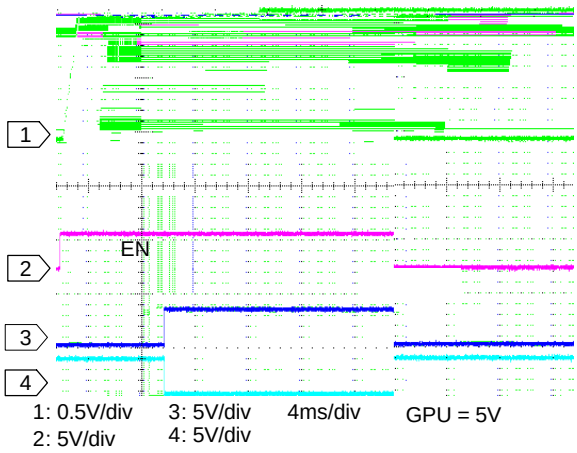


Figure 10. Startup Waveforms GPU Mode

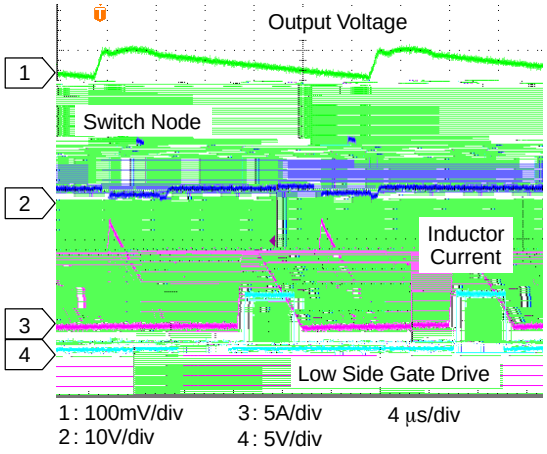


Figure 11. DCM Waveforms, 1 A Load Current

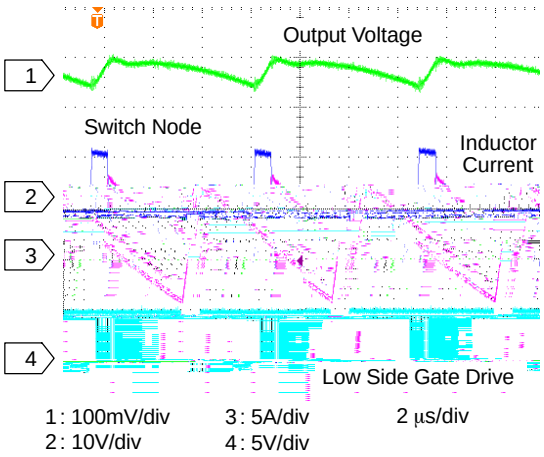


Figure 12. CCM Waveforms, 10 A Load Current

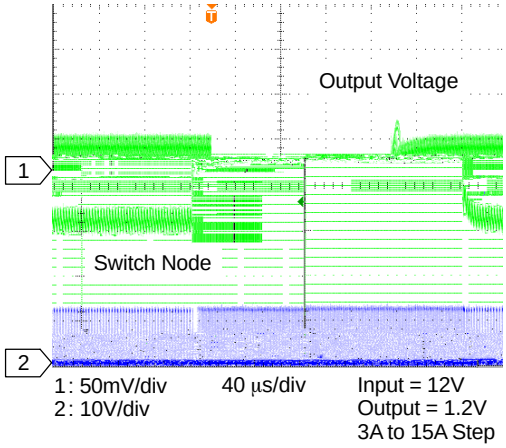


Figure 13. Load Transient

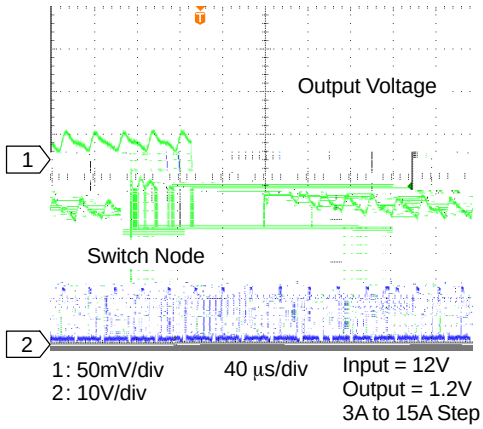


Figure 14. Load Transient

TYPICAL PERFORMANCE CHARACTERISTICS

THEORY OF OPERATION

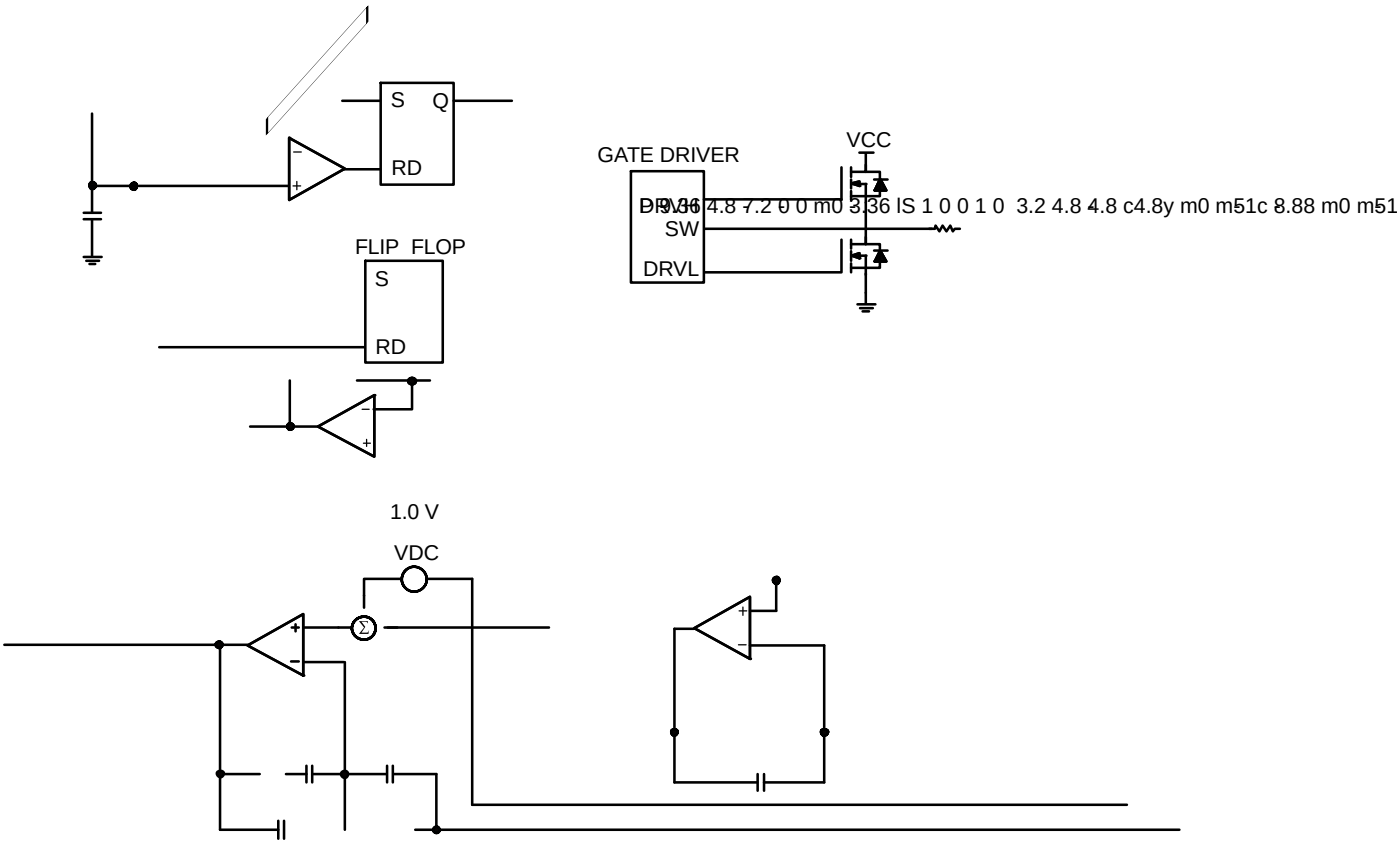
The ADP3211 is a Ramp Pulse Modulated (RPM) controller for synchronous buck Intel GMCH and CPU core power supply. The internal 7−bit VID DAC conforms to the Intel IMVP−6.5 specifications. The ADP3211 is a stable, high performance architecture that includes

- High speed response at the lowest possible switching frequency and minimal count of output decoupling capacitors
- Minimized thermal switching losses due to lower frequency operation
- High accuracy load line regulation
- High power conversion efficiency with a light load by automatically switching to DCM operation

Operation Modes

The ADP3211 runs in RPM mode for the purpose of fast transient response and high light load efficiency. During the following transients, the ADP3211 runs in PWM mode:

- Soft−Start
- Soft transient: the period of 110 μs following any VID change
- Current overload



a sense element, such as the low−side MOSFET. The current sense amplifier can be configured several ways, depending on system optimization objectives, and the current information can be obtained by:

- Output inductor ESR sensing without the use of a thermistor for the lowest cost
- Output inductor ESR sensing with the use of a thermistor that tracks inductor temperature to improve accuracy
- Discrete resistor sensing for the highest accuracy

At the positive input of the CSA, the CSREF pin is connected to the output voltage. At the negative input (that is, the CSFB pin of the CSA), signals from the sensing element (in the case of inductor DCR sensing, signals from the switch node side of the output inductors) are connected with a resistor. The feedback resistor between the CSCOMP and CSFB pins sets the gain of the current sense amplifier, and a filter capacitor is placed in parallel with this resistor. The current information is then given as the voltage difference between the CSCOMP and CSREF pins. This signal is used internally as a differential input for the current limit comparator.

An additional resistor divider connected between the CSCOMP and CSREF pins with the midpoint connected to the LLINE pin can be used to set the load line required by the GMCH specification. The current information to set the load line is then given as the voltage difference between the LLINE and CSREF pins. This configuration allows the load line slope to be set independent from the current limit threshold. If the current limit threshold and load line do not have to be set independently, the resistor divider between the CSCOMP and CSREF pins can be omitted and the CSCOMP pin can be connected directly to LLINE. To disable voltage positioning entirely (that is, to set no load line), LLINE should be tied to CSREF.

To provide the best accuracy for current sensing, the CSA has a low offset input voltage and the sensing gain is set by an external resistor ratio.

Active Impedance Control Mode

To control the dynamic output voltage droop as a function of the output current, the signal that is proportional to the total output current, converted from the voltage difference between LLINE and CSREF, can be scaled to be equal to the required droop voltage. This droop voltage is calculated by multiplying the droop impedance of the regulator by the output current. This value is used as the control voltage of the PWM regulator. The droop voltage is subtracted from the DAC reference output voltage, and the resulting voltage is used as the voltage positioning set−point. The arrangement results in an enhanced feed−forward response.

Voltage Control Mode

A high−gain bandwidth error amplifier is used for the voltage mode control loop. The non−inverting input voltage is set via the 7−bit VID DAC. The VID codes are listed in Table NO TAG. The non−inverting input voltage is offset by the droop voltage as a function of current, commonly known as active voltage positioning. The output of the error amplifier is the COMP pin, which sets the termination voltage of the internal PWM ramps.

At the negative input, the FB pin is tied to the output sense location using R_{FB}, a resistor for sensing and controlling the output voltage at the remote sensing point. The main loop compensation is incorporated in the feedback network connected between the FB and COMP pins.

Power−Good Monitoring

The power−good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open−drain output that can be pulled up through an external resistor to a voltage rail, not necessarily the same V_{CC} voltage

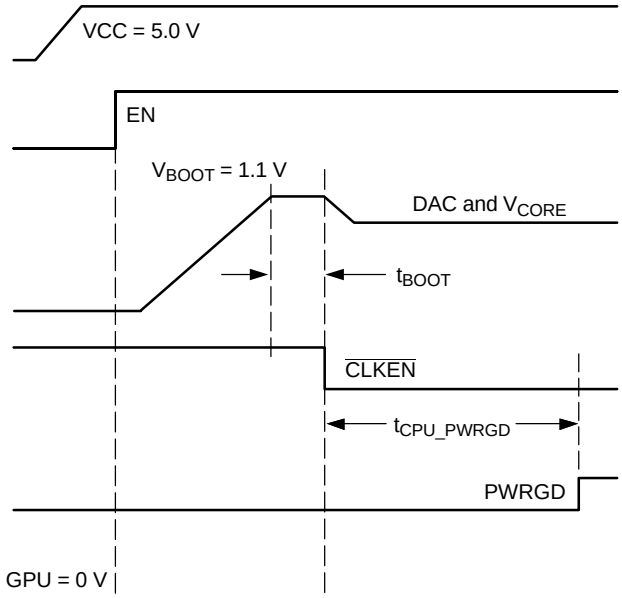


Figure 22. ADP3211 Powerup Sequence for CPU

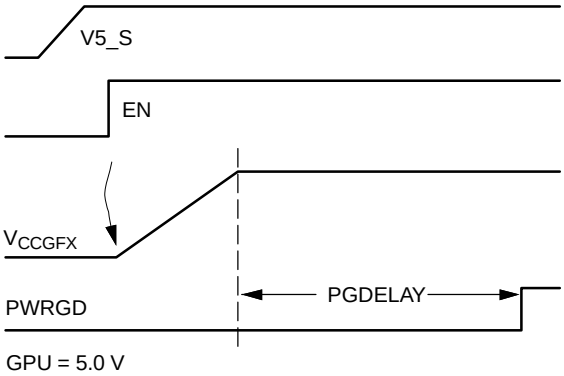


Figure 23. Powerup Sequence for GPU

VID Change and Soft Transient

With GPU connected to 5.0 V for GPU operation, when a VID input changes, the ADP3211 detects the change but ignores new code for a minimum of 400 ns. This delay is required to prevent the device from reacting to digital signal skew while the 7−bit VID input code is in transition. Additionally, the VID change triggers a PWRGD masking timer to prevent a PWRGD failure. Each VID change resets and re−triggers the internal PWRGD masking timer.

The ADP3211 provides a soft transient function to reduce inrush current during VID transitions. Reducing the inrush current helps decrease the acoustic noise generated by the MLCC input capacitors and inductors.

The soft transient feature is implemented internally. When a new VID code is detected, the ADP3211 steps sequentially through each VID voltage to the final VID voltage.

Current Limit, Short−Circuit, and Latchoff Protection

The ADP3211 has an adjustable current limit set by the R_{CLIM} resistor. The ADP3211 compares a programmable current limit set point to the voltage from the output of the current sense amplifier. The level of current limit is set with the resistor from the ILIM pin to CSCOMP. During operation, the voltage on ILIM is equal to the voltage on CSREF. The current through the external resistor connected between I_{LIM} and CSCOMP is then compared to the internal current limit current I_{cl}. If the current generated through this resistor into the ILIM pin (Ilim) exceeds the internal current limit threshold current (I_{cl}), the internal current limit amplifier controls the internal COMP voltage to maintain the average output current at the limit.

Normally, the ADP3211 operates in RPM mode. During a current overload, the ADP3211 switches to PWM mode.

With low impedance loads, the ADP3211 operates in a

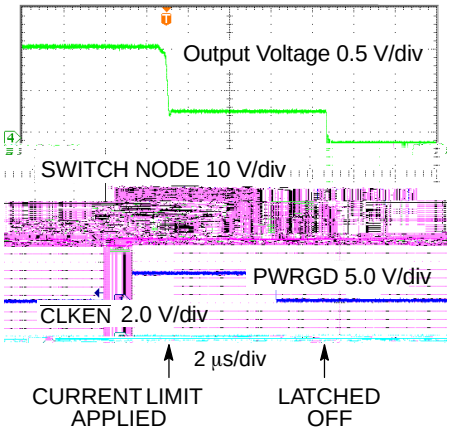


Figure 24. Current Overload

The latchoff function can be reset either by removing and reapplying V_{CC} or by briefly pulling the EN pin low.

During startup, when the output voltage is below 200 mV, a secondary current limit is active. This is necessary because the voltage swing of CSCOMP cannot extend below ground. This secondary current limit clamp controls the minimum internal COMP voltage to the PWM comparators to 1.5 V. This limits the voltage drop across the low−side MOSFETs through the current balance circuitry.

Light Load RPM DCM Operation

The ADP3211 operates in RPM mode. With higher loads, the ADP3211 operates in continuous conduction mode (CCM), and the upper and lower MOSFETs run synchronously and in complementary phase. See Figure 25 for the typical waveforms of the ADP3211 running in CCM with a 10 A load current.

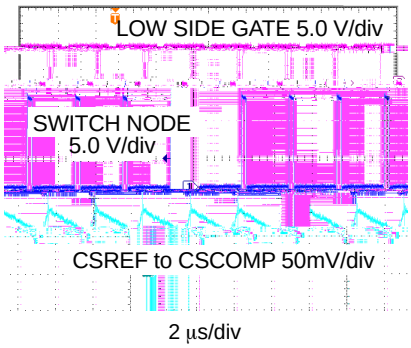


Figure 25. Single−Phase Waveforms in CCM

With lighter loads, the ADP3211 enters discontinuous conduction mode (DCM). Figure 26 shows a typical single−phase buck with one upper FET, one lower FET, an output inductor, an output capacitor, and a load resistor. Figure 27 shows the path of the inductor current with the upper FET on and the lower FET off. In Figure 28 the high−side FET is off and the low−side FET is on. In CCM, if one FET is on, its complementary FET must be off; however, in DCM, both high− and low−side FETs are off and no current flows into the inductor (see Figure 29). Figure 30 shows the inductor current and switch node voltage in DCM.

In DCM with a light load, the ADP3211 monitors the switch node voltage to determine when to turn off the low−side FET. Figure 31 shows a typical waveform in DCM with a 1 A load current. Between t1 and t2, the inductor current ramps down. The current flows through the source drain of the low−side FET and creates a voltage drop across the FET with a slightly negative switch node. As the inductor current ramps down to 0 A, the switch voltage approaches 0 V, as seen just before t2. When the switch voltage is approximately −4 mV, the low−side FET is turned off.

Figure 30 shows a small, dampened ringing at t2. This is caused by the LC created from capacitance on the switch node, including the CDS of the FETs and the output inductor. This ringing is normal.

The ADP3211 automatically goes into DCM with a liTh

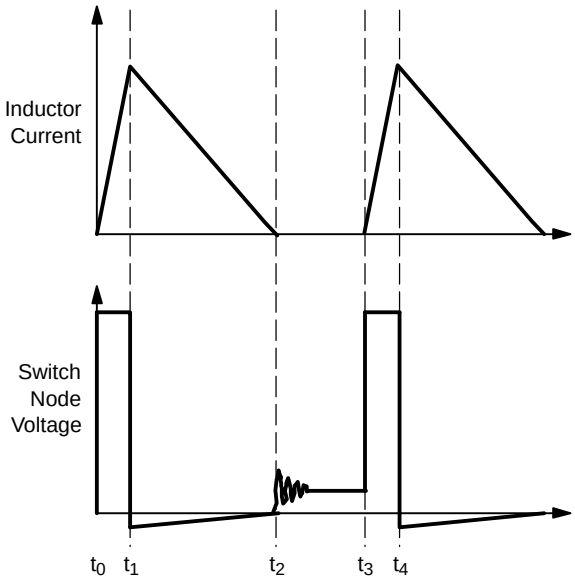


Figure 30. Inductor Current and Switch Node in DCM

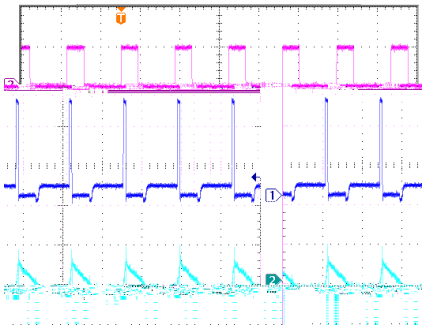


Figure 31. Single−

Table 1. VID Code Table

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output (V)
0	1 ref436.32 707.52 .48009						

Table 1. VID Code Table

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output (V)
1	0	1	0	0	1	0	0.4750
1	0	1	0	0	1	1	0.4625
1	0	1	0	1	0	0	0.4500
1	0	1	0	1	0	1	0.4375
1	0	1	0	1	1	0	0.4250
1	0	1	0	1	1	1	0.4125
1	0	1	1	0	0	0	0.4000
1	0	1	1	0	0	1	0.3875
1	0	1	1	0	1	0	0.3750
1	0	1	1	0	1	1	0.3625
1	0	1	1	1	0	0	0.3500
1	0	1	1	1	0	1	0.3375
1	0	1	1	1	1	0	0.3250
1	0	1	1	1	1	1	0.3125
1	1	0	0	0	0	0	0.3000
1	1	0	0	0	0	1	0.2875
1	1	0	0	0	1	0	0.2750
1	1	0	0	0	1	1	0.2625
1	1	0	0	1	0	0	0.2500
1	1	0	0	1	0	1	0.2375
1	1	0	0	1	1	0	0.2250
1	1	0	0	1	1	1	0.2125
1	1	0	1	0	0	0	0.2000
1	1	0	1	0	0	1	0.1875
1	1	0	1	0	1	0	0.1750
1	1	0	1	0	1	1	0.1625
1	1	0	1	1	0	0	0.1500
1	1	0	1	1	0	1	0.1375
1	1	0	1	1	1	0	0.1250
1	1	0	1	1	1	1	0.1125
1	1	1	0	0	0	0	0.1000
1	1	1	0	0	0	1	0.0875
1	1	1	0	0	1	0	0.0750
1	1	1	0	0	1	1	0.0625
1	1	1	0	1	0	0	0.0500
1	1	1	0	1	0	1	0.0375
1	1	1	0	1	1	0	0.0250
1	1	1	0	1	1	1	0.0125
1	1	1	1	0	0	0	0.0000
1	1	1	1	0	0	1	0.0000
1	1	1	1	0	1	0	0.0000
1	1	1	1	0	1	1	0.0000

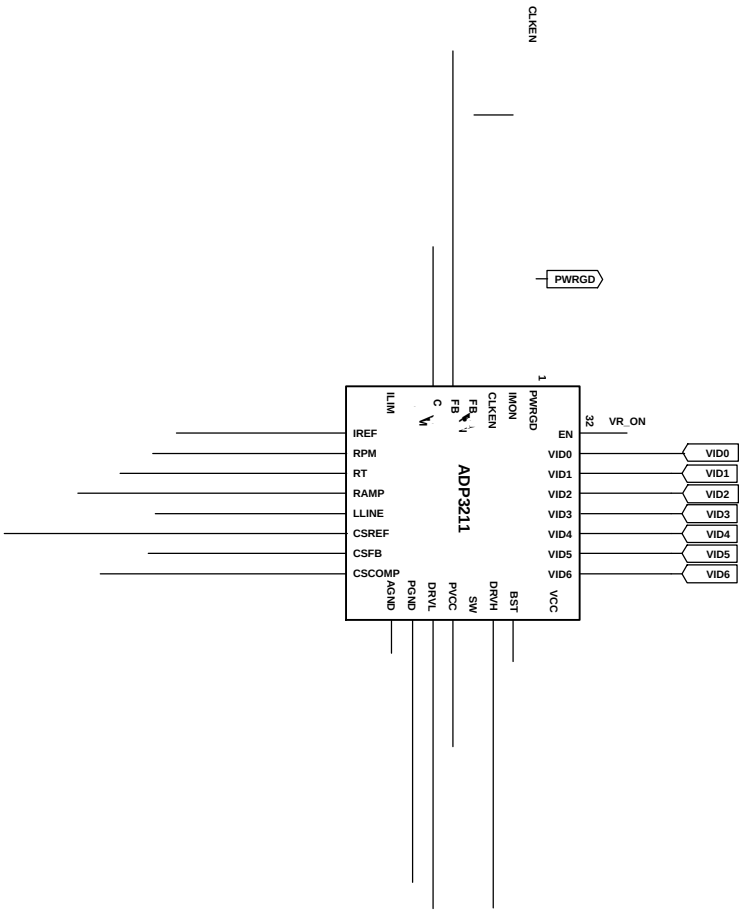


Figure 33. Typical Application Circuit

$$I_R = \frac{V_{VID} \times (1 - D_{MIN})}{f_{SW} \times L} \quad \text{(eq. 5)}$$

$$L \geq \frac{V_{VID} \times R_O \times (1 - D_{MIN})}{f_{SW}}$$

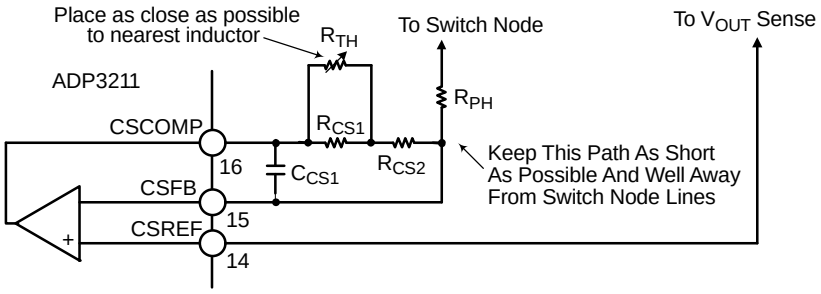


Figure 34. Temperature−Compensation Circuit Values

The following procedure and expressions yield values for R_{CS1}, R_{CS2}, and R_{TH} (the thermistor value at 25°C) for a given R_{CS} value.

1. Select an NTC to be used based on its type and value. Because the value needed is not yet determined, start with a thermistor with a value

$$C_{X(MIN)} \geq \left(\frac{L \times \Delta I_O}{\left(R_O + \frac{V_{OSMAX}}{\Delta I_O} \right) \times V_{VID}} - C_Z \right) \quad \text{(eq. 15)}$$

$$C_{X(MAX)} \leq \frac{L}{k^2 \times R_o{}^2} \times \frac{V_V}{V_{VID}} \times \left(\sqrt{1 + \left(t_v \frac{V_{VID}}{V_V} \times \frac{k \times R_o}{L} \right)^2} - 1 \right) - C_Z$$

$$\text{where } k = \ln\left(\frac{V_{ERR}}{V_V} \right) \quad \text{(eq. 16)}$$

To meet the conditions of these expressions and the transient response, the ESR of the bulk capacitor bank (R_X) should be less than two times the droop resistance, R_O. If the $C_{X(MIN)}$ is greater than $C_{X(MAX)}$, the system does not

about 120°C; therefore, the $R_{DS(SF)}$ per MOSFET should be less than 13.3 mΩ at room temperature, or 18.8 mΩ at high temperature.

Another important factor for the synchronous MOSFET is the input capacitance and feedback capacitance. The ratio of the feedback to input must be small (less than 10% is recommended) to prevent accidentally turning on the synchronous MOSFETs when the switch node goes high.

The high−side (main) MOSFET must be able to handle two main power dissipation components: conduction losses and switching losses. Switching loss is related to the time for the main MOSFET to turn on and off and to the current and voltage that are being switched. Basing the switching speed on the rise and fall times of the gate driver impedance and MOSFET input capacitance, the following expression provides an approximate value for the switching loss per main MOSFET:

$$P_{S(MF)} = 2 \times f_{SW} \times \frac{V_{DC} \times I_O}{n_{MF}} \times R_G \times n_{MF} \times C_{ISS} \quad \text{(eq. 21)}$$

where:
n_{MF} is the total number of main MOSFETs.
R_G is the total gate resistance.
C_{ISS} is the input capacitance of the main MOSFET.

The most effective way to reduce switching loss is to use lower gate capacitance devices.

The conduction loss of the main MOSFET is given by the following equation:

$$P_{C(MF)} = D \times \left[\left(\frac{I_O}{n_{MF}} \right)^2 + \frac{1}{12} \times \left(\frac{I_R}{n_{MF}} \right)^2 \right] \times R_{DS(MF)} \quad \text{(eq. 22)}$$

where $R_{DS(MF)}$ is the on resistance of the MOSFET.

Typically, a user wants the highest speed (low C_{ISS}) device for a main MOSFET, but such a device usually has higher on resistance. Therefore, the user must select a device that meets the total power dissipation (about 0.8 W to 1.0 W for an 8−lead SOIC) when combining the switching and conduction losses.

For example, an NTMFS4821N device can be selected as the main MOSFET (one in total; that is, n_{MF} = 1), with approximately C_{ISS} = 1400 pF (maximum) and $R_{DS(MF)}$ = 8.6 mΩ (maximum at T_J = 120°C), and an NTMFS4846N device can be selected as the synchronous MOSFET (two in total; that is, n_{SF} = 2), with $R_{DS(SF)}$ = 3.8 mΩ (maximum at T_J = 120°C). Solving for the power dissipation per MOSFET at I_O = 15 A and I_R = 5.0 A yields 178 mW for each synchronous MOSFET and 446 mW for each main MOSFET. A third synchronous MOSFET is an option to further increase the conversion efficiency and reduce thermal stress.

Finally, consider the power dissipation in the driver. This is best described in terms of the Q_G for the MOSFETs and is given by the following equation:

$$\left[\frac{f_{SW}}{2} \times (n_{MF} \times Q_{GMF} + n_{SF} \times Q_{GS\ aa\ 0\ 0\ 9\ 47\ 705.6A\ Tc()Tj/TT4\ 1\ Tf1.2\ 0\ TD(r} \right.$$

node when the high side MOSFET turns on. The switch node ringing could cause EMI system failures and increased stress on the power components and controller. The RC snubber should be placed as close as possible to the low side MOSFET. Typical values for the resistor range from 1 Ω to 10 Ω. Typical values for the capacitor range from 330 pF to 4.7 nF. The exact value of the RC snubber depends on the PCB layout and MOSFET selection. Some fine tuning must be done to find the best values. The equation below is used to find the starting values for the RC snubber.

$$R_{Snubber} = \frac{1}{2 \times \pi \times f_{Ringing} \times C_{OSS}} \quad \text{(eq. 27)}$$

$$C_{Snubber} = \frac{1}{\pi \times f_{Ringing} \times R_{Snubber}} \quad \text{(eq. 28)}$$

$$P_{Snubber} = C_{Snubber} \times V^2_{Input} \times f_{Switching} \quad \text{(eq. 29)}$$

Where $R_{Snubber}$ is the snubber resistor.
$C_{Snubber}$ is the snubber capacitor.
$f_{Ringing}$ is the frequency of the ringing on the switch node when the high side MOSFET turns on.
C_{OSS} is the low side MOSFET output capacitance at V_{Input}. This is taken from the low side MOSFET data sheet.
V_{input} is the input voltage.
$f_{Switching}$ is the switching frequency.
$P_{Snubber}$ is the power dissipated in $R_{Snubber}$.

Current Monitor

The ADP3211 has an output current monitor. The I_{MON} pin sources a current proportional to the total inductor current. A resistor, R_{MON}, from I_{MON} to FBRTN sets the gain of the output current monitor. A 0.1 μF is placed in parallel with R_{MON} to filter the inductor current ripple and high frequency load transients. Since the I_{MON} pin is connected directly to the CPU, it is clamped to prevent it from going above 1.15 V.

The I_{MON} pin current is equal to the R_{LIM} times a fixed gain of 10. R_{MON} can be found using the following equation:

$$R_{MON}$$

The expressions that follow compute the time constants for the poles and zeros in the system and are intended to yield an optimal starting point for the design; some adjustments may be necessary to account for PCB and component parasitic effects (see the Tuning Procedure for ADP3211 section):

$$R_E = R_O + A_D \times R_{DS} + \frac{R_{DCR} \times V_{RT}}{V_{VID}} + \frac{2 \times L \times (1 - D) \times V_{RT}}{C_X \times R_O \times V_{VID}} \quad \text{(eq. 35)}$$

$$T_A = C_X \times (R_O - R') + \frac{L_X}{R_O} \times \frac{R_O - R'}{R_X} \quad \text{(eq. 36)}$$

$$T_B = (R_X + R' - R_O) \times C_X \quad \text{(eq. 37)}$$

$$T_C = \frac{V_{RT} \times \left(L - \frac{A_D \times R_{DS}}{2 \times f_{SW}}\right)}{V_{VID} \times R_E} \quad \text{(eq. 38)}$$

$$T_D = \frac{C_X \times C_Z \times R_O{}^2}{C_X \times (R_O - R') + C_Z \times R_O} \quad \text{(eq. 39)}$$

where:
R' is the PCB resistance from the bulk capacitors to the ceramics and is approximately 0.4 mΩ (assuming an 8−layer motherboard).
R_{DS} is the total low−side MOSFET for on resistance.
A_D is 5.
V_{RT} is 1.25 V.
L_X is the ESL of the bulk capacitors (450 pH for the two Panasonic SP capacitors).

The compensation values can be calculated as follows:

$$C_A = \frac{R_O \times T_A}{R_E \times R_{FB}} \quad \text{(eq. 40)}$$

$$R_A = \frac{T_C}{C_A} \quad \text{(eq. 41)}$$

$$C_{FB} = \frac{T_B}{R_{FB}} \quad \text{(eq. 42)}$$

$$C_B = \frac{T_D}{R_A} \quad \text{(eq. 43)}$$

The standard values for these components are subject to the tuning procedure described in the Tuning Procedure for ADP3211 section.

C_{IN} Selection and Input Current D_I/D_T Reduction

In continuous inductor−current mode, the source current of the high−side MOSFET is approximately a square wave with a duty ratio equal to V_{OUT}/V_{IN}. To prevent large voltage transients, use a low ESR input capacitor sized for the maximum RMS current.

The maximum RMS capacitor current occurs at the lowest input voltage and is given by:

$$I_{CRMS} = D \times I_O \times \sqrt{\frac{1}{D} - 1} \quad \text{(eq. 44)}$$

$$I_{CRMS} = 0.15 \times 15\ A \times \sqrt{\frac{1}{0.15} - 1} = 5.36\ A$$

where I_O is the output current.

In a typical notebook system, the battery rail decoupling is achieved by using MLC capacitors or a mixture of MLC capacitors and bulk capacitors. In this example, the input capacitor bank is formed by four pieces of 10 μF, 25 V MLC capacitors, with a ripple current rating of about 1.5 A each.

TUNING PROCEDURE FOR ADP3211

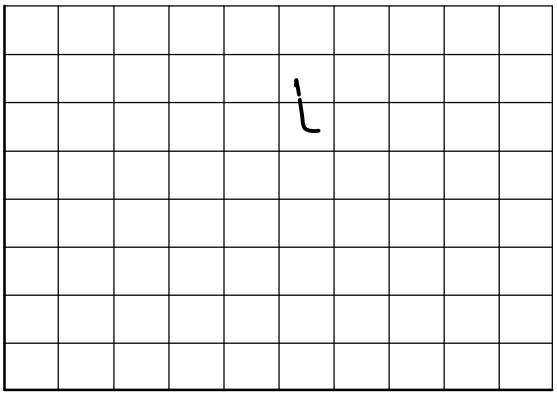
Set Up and Test the Circuit

1. Build a circuit based on the compensation values computed from the design spreadsheet.

7. Measure the output ripple with no load and with a full load with scope, making sure both are within the specifications.

Set the AC Load Line

1. Remove the dc load from the circuit and connect a dynamic load.
2. Connect the scope to the output voltage and set it to dc coupling mode with a time scale of 100 μs/div.
3. Set the dynamic load for a transient step of about 40 A at 1 kHz with 50% duty cycle.
4. Measure the output waveform (note that use of a dc offset on the scope may be necessary to see the waveform). Try to use a vertical scale of 100 mV/div or finer.
5. The resulting waveform will be similar to that shown in Figure 37. Use the horizontal cursors to measure V_{ACDRP} and V_{DCDRP}, as shown in Figure 37. Do not measure the undershoot or overshoot that occurs immediately after the step.



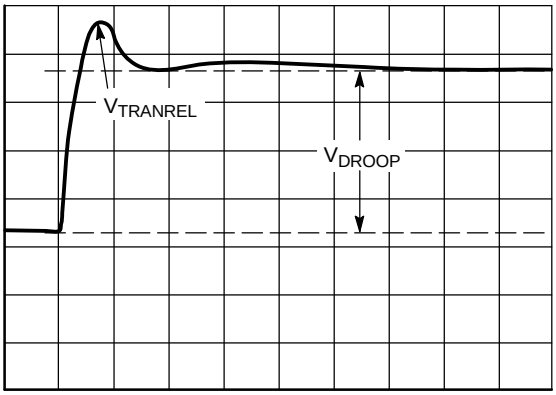


Figure 39. Transient Setting Waveform, Load Release

Layout and Component Placement

The following guidelines are recommended for optimal performance of a switching regulator in a PC system.

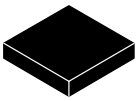
General Recommendations

1. For best results, use a PCB of four or more layers. This should provide the needed versatility for control circuitry interconnections with optimal placement; power planes for ground, input, and output; and wide interconnection traces in the rest

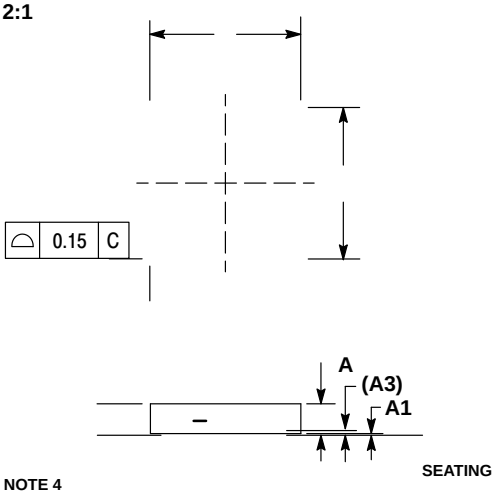
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

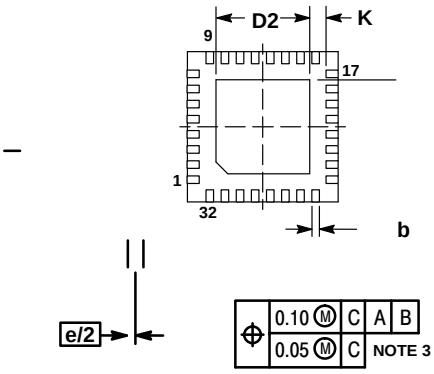
DATE 23 OCT 2013



SCALE 2:1

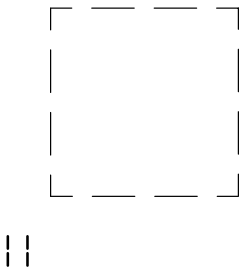


	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	2.95	3.25
E	5.00 BSC	
E2	2.95	3.25
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15



XXXXXXXX
XXXXXXXX
AWLYYWW▪
▪Free indicator, “G” or

RECOMMENDED



PITCH

DIMENSION: MILLIMETERS

DOCUMENT NUMBER:	98AON20032D	