ADP3212, NCP3218, NCP3218G

7-Bit, Programmable, 3-Phase, Mobile CPU Synchronous Buck Controller

The APD3212/NCP3218/NCP3218G is a highly efficient, multi−phase, synchronous buck switching regulator controller. With its integrated drivers, the APD3212/NCP3218/NCP3218G is optimized for converting the notebook battery voltage into the core supply voltage required by high performance Intel processors. An internal 7−bit DAC is used to read a VID code directly from the processor and to set the CPU core voltage to a value within the range of 0.3 V to 1.5 V. The APD3212/NCP3218/NCP3218G is programmable for 1−, 2−, or 3−phase operation. The output signals ensure interleaved 2− or 3−phase operation.

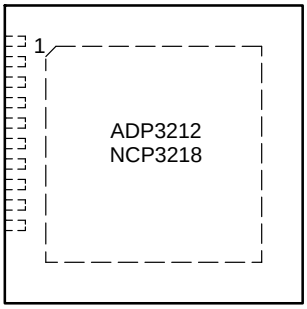
The APD3212/NCP3218/NCP3218G uses a multimode architecture run at a programmable switching frequency and optimized for efficiency depending on the output current requirement. The APD3212/NCP3218/NCP3218G switches between single− and multi−phase operation to maximize efficiency with all load conditions. The chip includes a programmable load line slope function to adjust the output voltage as a function of the load current so that the core voltage is always optimally positioned for a load transient. The APD3212/NCP3218/NCP3218G also provides accurate and reliable short−circuit protection, adjustable current limiting, and a delayed power−good output. The IC supports On−The−Fly (OTF) output voltage changes requested by the CPU.

The APD3212/NCP3218/NCP3218G are specified over the extended commercial temperature range of −40°C to 100°C. The ADP3212 is available in a 48−lead QFN 7x7mm 0.5mm pitch package. The NCP3218/NCP3218G is available in a 48−lead QFN 6x6mm 0.4mm pitch package. ADP3212/NCP3218 has 1.1 V Vboot Voltage, while NCP3218G has 987.5 mV Vboot Voltage. Except for the packages and Vboot Voltages, the APD3212/NCP3218/NCP3218G are identical. APD3212/NCP3218/NCP3218G are Halogen−Free, Pb−Free and RoHS compliant.

Features

- Single−Chip Solution
- Fully Compatible with the Intel IMVP−6.5™ Specifications
- Selectable 1−, 2−, or 3−Phase Operation with Up to 1 MHz per Phase Switching Frequency
- Phase 1 and Phase 2 Integrated MOSFET Drivers
- Input Voltage Range of 3.3 V to 22 V
- Guaranteed ±8 mV Worst−Case Differentially Sensed Core Voltage Error Over Temperature
- Automatic Power−Saving Mode Maximizes Efficiency with Light Load During Deeper Sleep Operation
- Active Current Balancing Between Output Phases
- Independent Current Limit and Load Line Setting Inputs for Additional Design Flexibility
- Built−In Power−Good Blanking Supports Voltage Identification (VID) On−The−Fly (OTF) Transients
- 7−Bit, Digitally Programmable DAC with 0.3 V to 1.5 V Output
- Short−Circuit Protection with Programmable Latchoff Delay
-

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
V_{CC}, PV_{CC1}, PV_{CC2}	−0.3 to +6.0	V
FBRTN, PGND1, PGND2	−0.3 to +0.3	V
BST1, BST2, DRVH1, DRVH2 DC t < 200 ns	 −0.3 to +28 −0.3 to +33	V
BST1 to PV_{CC}, BST2 to PV_{CC} DC t < 200 ns	 −0.3 to +22 −0.3 to +28	V
BST1 to SW1, BST2 to SW2	−0.3 to +6.0	V
SW1, SW2 DC t < 200 ns	 −1.0 to +22 −6.0 to +28	V
DRVH1 to SW1, DRVH2 to SW2	−0.3 to +6.0	V
DRVL1 to PGND1, DRVL2 to PGND2 DC t < 200 ns	 −0.3 to +6.0 −5.0 to +6.0	V
RAMP (in Shutdown)	−0.3 to +22	V
All Other Inputs and Outputs	−0.3 to +6.0	V
Storage Temperature Range	−65 to +150	°C
Operating Ambient Temperature Range	−40 to +100	°C
Operating Junction Temperature	125	°C
Thermal Impedance (θ_{JA}) 2−Layer Board	30.5	°C/W
Lead Temperature Soldering (10 sec) Infrared (15 sec)	 300 260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

PIN ASSIGNMENT

Pin No.	Mnemonic	Description
1	EN	Enable Input. Driving this pin low shuts down the chip, disables the driver outputs, pulls PWRGD and VRTT low, and pulls $\overline{\text{CLKEN}}$ high.
2	PWRGD	Power−Good Output. Open−drain output. A low logic state means that the output voltage is outside of the VID DAC defined range.
3	IMON	Current Monitor Output. This pin sources a current proportional to the output load current. A resistor to FBRTN sets the current monitor gain.
4	$\overline{\text{CLKEN}}$	Clock Enable Output. Open−drain output. A low logic state enables the CPU internal PLL clock to lock to the external clock.
5	FBRTN	Feedback Return Input/Output. This pin remotely senses the CPU core voltage. It is also used as the ground return for the VID DAC and the voltage error amplifier blocks.
6	FB	Voltage Error Amplifier Feedback Input. The inverting input of the voltage error amplifier.
7	COMP	Voltage Error Amplifier Output and Frequency Compensation Point.
8	$\overline{\text{TRDET}}$	Transient Detect Output. This pin is pulled low when a load release transient is detected. During repetitive load transients at high frequencies, this circuit optimally positions the maximum and minimum output voltage into a specified loadline window.
9	VARFREQ	Variable Frequency Enable Input. A high logic state enables the PWM clock frequency to vary with VID code.
10	VRTT	Voltage Regulator Thermal Throttling Output. Logic high state indicates that the voltage regulator temperature at the remote sensing point exceeded a set alarm threshold level.

PIN ASSIGNMENT

Pin No.	Mnemonic	Description
11	TTSNS	Thermal Throttling Sense and Crowbar Disable Input. A re

ELECTRICAL CHARACTERISTICS

V_{CC} = PV_{CC} = 5.0 V, FBRTN = PGND = GND = 0 V, H = 5.0 V, L = 0 V, EN = VARFREQ = H, DPRSLP = L, $\overline{PSI}$ = 1.05 V, V_{VID} = V_{DAC} = 1.2000 V, T_A = −40°C to 100°C, unless otherwise noted. (Note 1) Current entering a pin (sink current) has a positive sign.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VOLTAGE CONTROL **VOLTAGE ERROR AMPLIFIER (VEAMP)**						
FB, LLINE Voltage Range (Note 2)	V_{FB}, V_{LLINE}	Relative to CSREF = VDAC	−200		+200	mV
FB, LLINE Offset Voltage (Note 2)	V_{OSVEA}	Relative to CSREF = VDAC	−0.5		+0.5	mV
LLINE Bias Current	I_{LLINE}		−100		+100	nA
FB Bias Current	I_{FB}		−1.0		+1.0	μA
LLINE Positioning Accuracy	V_{FB} − V_{VID}	Measured on FB relative to V_{VID}, LLINE forced 80 mV below CSREF	−77.5	−80	−82.5	mV
COMP Voltage Range (Note 2)	V_{COMP}		0.85		4.0	V
COMP Current	I_{COMP}	COMP = 2.0 V, CSREF = VDAC FB forced 200 mV below CSREF FB forced 200 mV above CSREF		−0.75 6		mA
COMP Slew Rate	SR_{COMP}	C_{COMP} = 10 pF, CSREF = VDAC, Open loop configuration FB forced 200 mV below CSREF FB forced 200 mV above CSREF		15 −20		V/μs
Gain Bandwidth (Note 2)	GBW	Non−inverting unit gain configuration, R_{FB} = 1 kΩ		20		MHz
VID DAC VOLTAGE REFERENCE						
VDAC Voltage Range (Note 2)		See VID table	0		1.5	V
VDAC Accuracy	V_{FB} − V_{VID}	Measured on FB (includes offset), relative to V_{VID} V_{VID} = 1.2000 V to 1.5000 V, T = −40°C to 100°C V_{VID} = 0.3000 V to 1.1875 V, T = −40°C to 100°C	 −8.5 −7.5		 +8.5 +7.5	mV
VDAC Differential Non−linearity (Note 2)			−1.0		+1.0	LSB
VDAC Line Regulation	ΔV_{FB}	VCC = 4.75 V to 5.25 V		0.02		%
VDAC Boot Voltage (ADP3212, NCP3218)	V_{BOOTFB}	Measured during boot delay period		1.100		V
VDAC Boot Voltage (NCP3218G)	V_{BOOTFB}	Measured during boot delay period		987.5		mV
Soft−Start Delay (Note 2)	t_{DSS}	Measured from EN pos edge to FB = 50 mV		200		μs
Soft−Start Time	t_{SS}	Measured from FB = 50 mV to FB settles to 1.1 V within 5%		1.4		ms
Boot Delay	t_{BOOT}	Measured from FB settling to 1.1 V within 5% to $\overline{CLKEN}$ neg edge		60		μs
VDAC Slew Rate (Note 2)		Soft−Start Non−LSB VID step, DPRSLP = H, Slow C4 Entry/Exit Non−LSB VID step, DPRSLP = L, Fast C4 Exit LSB VID step, DVID transition		0.0625 0.25 1.0 0.4		LSB/μs
FBRTN Current	I_{FBRTN}			−90	−200	μA
VOLTAGE MONITORING and PROTECTION **POWER GOOD**						
CSREF Undervoltage Threshold	$V_{UVCSREF}$	Relative to nominal VDAC voltage	−240	−300	−360	mV
CSREF Overvoltage Threshold	$V_{OVCSREF}$	Relative to nominal VDAC voltage	150	200	250	mV
CSREF Crowbar Voltage Threshold	$V_{CBCSREF}$	Relative to FBRTN, V_{VID} > 1.1 V Relative to FBRTN, V_{VID} ≤ 1.1 V	1.5 1.3	1.55 1.35	1.6 1.4	V

1. All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).
2. Guaranteed by design or bench characterization, not production tested.
3. Based on bench characterization data.
4. Timing is referenced to the 90% and 10% points, unless otherwise noted.

ELECTRICAL CHARACTERISTICS

V_{CC} = PV_{CC} = 5.0 V, FBRTN = PGND = GND = 0 V, H = 5.0 V, L = 0 V, EN = VARFREQ = H, DPRSLP = L, $\overline{PSI}$ = 1.05 V, V_{VID} = V_{DAC} = 1.2000 V, T_A = −40°C to 100°C, unless otherwise noted. (Note 1) Current entering a pin (sink current) has a positive sign.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VOLTAGE MONITORING and PROTECTION POWER GOOD						
CSREF Reverse Voltage Threshold	$V_{RVCSREF}$	Relative to FBRTN, latchoff mode CSREF is falling CSREF is rising	−370	−300 −75	 −10	mV
PWRGD Low Voltage	V_{PWRGD}	$I_{PWRGD(SINK)}$ = 4 mA		85	250	mV

ELECTRICAL CHARACTERISTICS

V_{CC} = PV_{CC} = 5.0 V, FBRTN = PGND = GND = 0 V, H = 5.0 V, L = 0 V, EN = VARFREQ = H, DPRSLP = L, $\overline{PSI}$ = 1.05 V, V_{VID} = V_{DAC} = 1.2000 V, T_A = −40°C to 100°C, unless otherwise noted. (Note 1) Current entering a pin (sink current) has a positive sign.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
ZERO CURRENT SWITCHING COMPARATOR						
Masked Off−Time	$t_{OFFMSKD}$					

TYPICAL PERFORMANCE CHARACTERISTICS

V_{VID} = 1.5 V, T_A = 20°C to 100°C, unless otherwise noted.

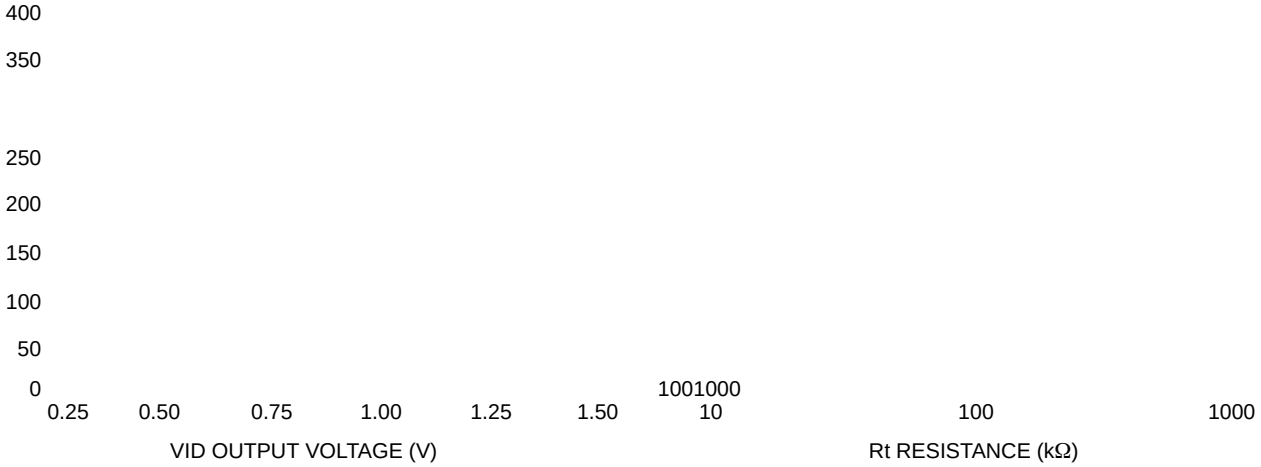
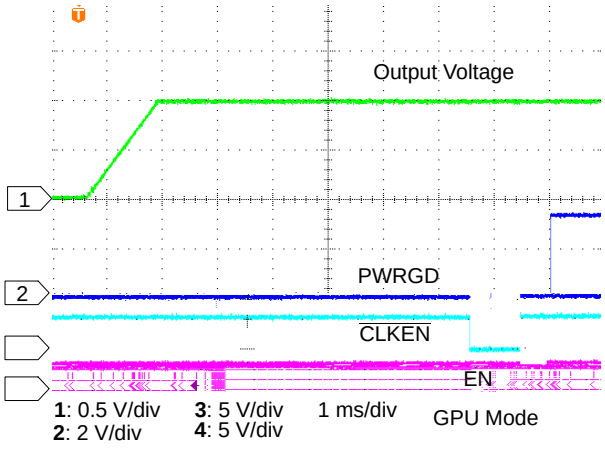
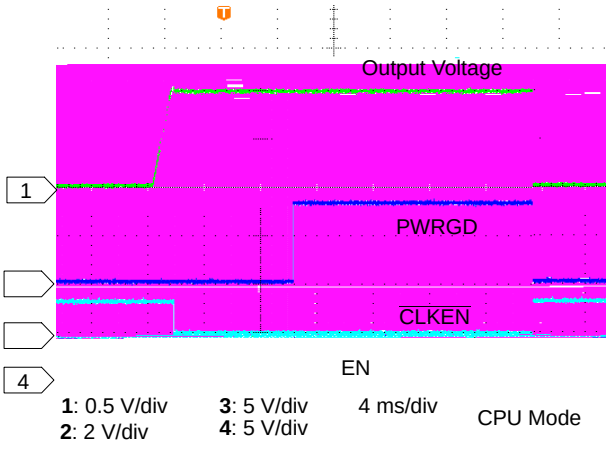
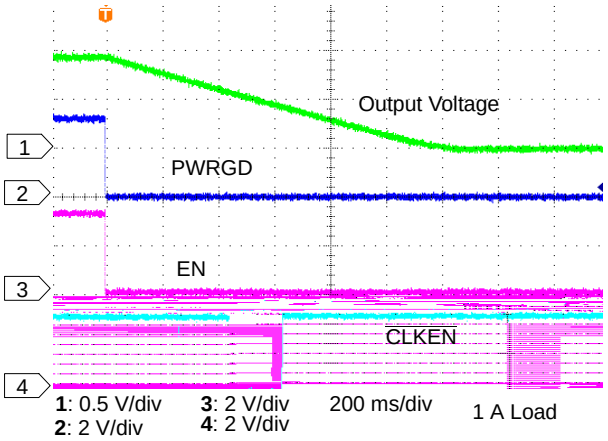


Figure 6. Switching Frequency vs. VID Output Voltage in PWM Mode

Figure 7. Per Phase Switching Frequency vs. RT Resistance







TYPICAL PERFORMANCE CHARACTERISTICS

V_{VID} = 1.5 V, T_A = 20°C to 100°C, unless otherwise noted.

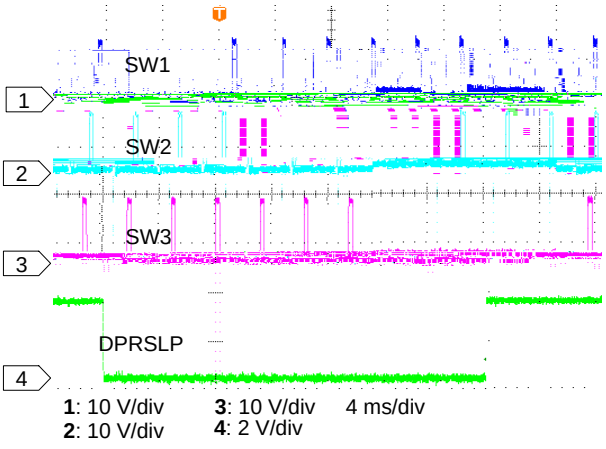


Figure 11. DPRSLP Transition with PSI = High

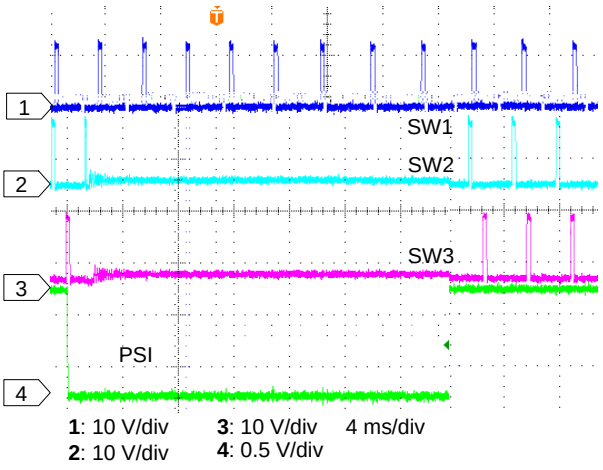


Figure 12. PSI Transition with DPRSLP = Low

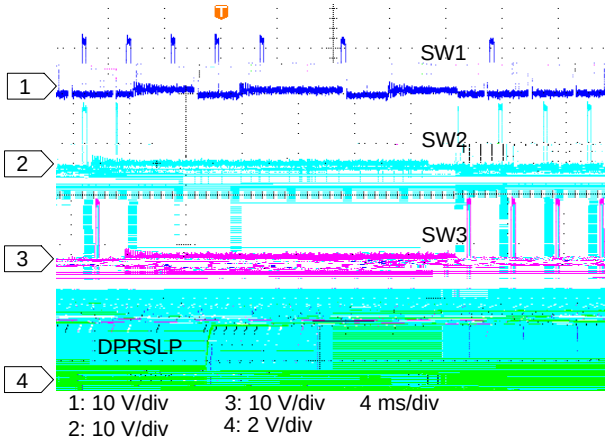


Figure 13. DPRSLP Transition with PSI = High

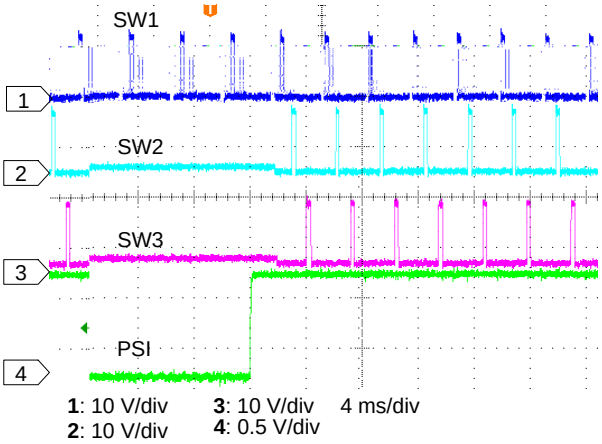


Figure 14. PSI Transition with DPRSLP = Low

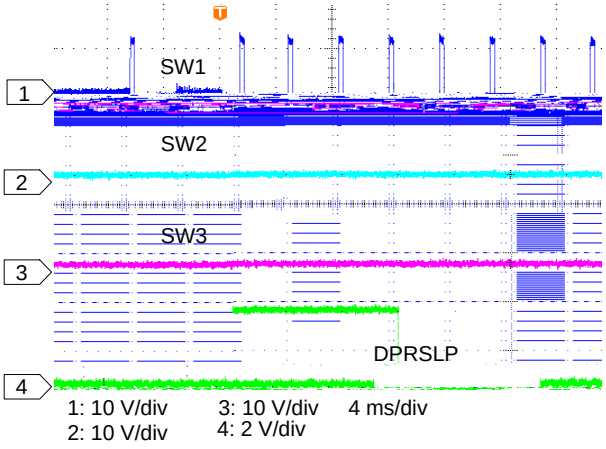


Figure 15. DPRSLP Transition with PSI = Low

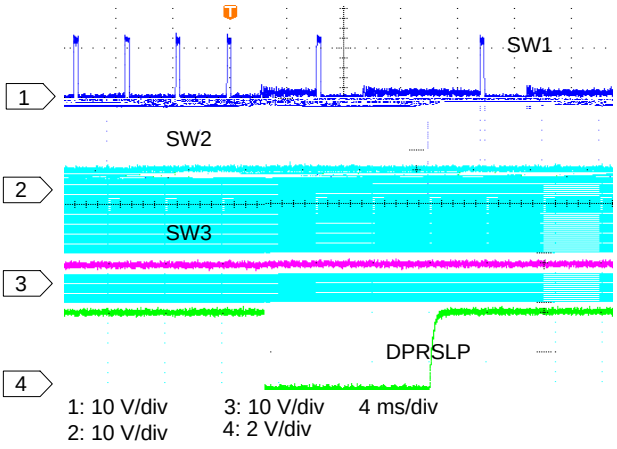


Figure 16. DPRSLP Transition with PSI = Low

Theory of Operation

The APD3212/NCP3218/NCP3218G combines multi−mode Pulse−Width Modulated (PWM) control and Ramp−Pulse Modulated (RPM) control with multi−phase logic outputs for use in single−, dual−phase, or triple−phase synchronous buck CPU core supply power converters. The internal 7−bit VID DAC conforms to the Intel IMVP−6.5 specifications.

Multi−phase operation is important for producing the high currents and low voltages demanded by today's microprocessors. Handling high currents in a single−phase converter would put too high of a thermal stress on system components such as the inductors and MOSFETs.

The multimode control of the APD3212/NCP3218/NCP3218G is a stable, high performance architecture that includes

- Current and thermal balance between phases.
- High speed response at the lowest possible switching frequency and minimal count of output decoupling capacitors.
- Minimized thermal switching losses due to lower frequency operation.
- High accuracy load line regulation.
- High current output by supporting 2−phase or 3−phase operation.
- Reduced output ripple due to multi−phase ripple cancellation.
- High power conversion efficiency with heavy and light loads.
- Increased immunity from noise introduced by PC board layout constraints.
- Ease of use due to independent component selection.
- Flexibility in design by allowing optimization for either low cost or high performance.

Number of Phases

The number of operational phases can be set by the user. Tying the PH1 pin to the GND pin forces the chip into single−phase operation. Tying PH0 to GND and PH1 to VCC forces the chip into 2−phase operation. Tying PH0 and PH1 to VCC forces the chip in 3−phase operation. PH0 and PH1 should be hard wired to VCC or GND. The APD3212/NCP3218/NCP3218G switches between single phase and multi−phase operation with $\overline{PSI}$ and DPRSLP to optimize power conversion efficiency. Table 1 summarizes PH0 and PH1.

Table 1. PHASE NUMBER CONFIGURATION

PH0	PH1	Number of Phases Configured
0	0	1
1	0	1 (GPU Mode)
0	1	2
1	1	3

In mulit−phase configuration, the timing relationship between the phases is determined by internal circuitry that monitors the PWM outputs. Because each phase is monitored independently, operation approaching 100% duty cycle is possible. In addition, more than one output can be active at a time, permitting overlapping phases.

Operation Modes

The number of phases can be static (see the Number of Phases section) or dynamically controlled by system signals to optimize the power conversion efficiency with heavy and light loads.

If APD3212/NCP3218/NCP3218G is configured for mulit−phase configuration, during a VID transient or with a heavy load condition (indicated by DPRSLP being low and $\overline{PSI}$ being high), the APD3212/NCP3218/NCP3218G runs in multi−phase, interleaved PWM mode to achieve minimal V_{CORE} output voltage ripple and the best transient performance possible. If the load becomes light (indicated by $\overline{PSI}$ being low or DPRSLP being high), APD3212/NCP3218/NCP3218G switches to single−phase mode to maximize the power conversion efficiency.

In addition to changing the number of phases, the APD3212/NCP3218/NCP3218G is also capable of dynamically changing the control method. In dual−phase operation, the APD3212/NCP3218/NCP3218G runs in PWM mode, where the switching frequency is controlled by the master clock. In single−phase operation (commanded by the DPRSLP high state), the APD3212/NCP3218/NCP3218G runs in RPM mode, where the switching frequency is controlled by the ripple voltage appearing on the COMP pin. In RPM mode, the DRVH1 pin is driven high each time the COMP pin voltage rises to a voltage limit set by the VID voltage and an external resistor connected between the RPM pin and GND. In RPM mode, the APD3212/NCP3218/NCP3218G turns off the low−side (synchronous rectifier) MOSFET when the inductor current drops to 0. Turning off the low−side MOSFETs at the zero current crossing prevents reversed inductor current build up and breaks synchronous operation of high− and low−side switches. Due to the asynchronous operation, the switching frequency becomes slower as the load current decreases, resulting in good power conversion efficiency with very light loads.

Table 2 summarizes how the APD3212/NCP3218/NCP3218G dynamically changes the number of active phases and transitions the operation mode bc.7 Tw [illegible]

Table 2. PHASE NUMBER AND OPERATION MODES

To increase the current in any given phase, users should make RSWFB for that phase larger (that is, RSWFB = 100 Ω for the hottest phase and do not change it during balance optimization). Increasing RSWFB to 150 Ω makes a substantial increase in phase current. Increase each RSWFB value by small amounts to achieve thermal balance starting with the coolest phase.

If adjusting current balance between phases is not needed, RSWFB should be 100 Ω for all phases.

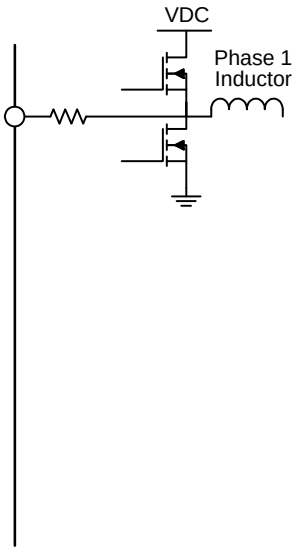


Figure 19. Current Balance Resistors

When a VID input changes, the APD3212/NCP3218/NCP3218G detects the change but ignores new code for a minimum of 400 ns. This delay is required to prevent the device from reacting to digital signal skew while the 7−bit VID input code is in transition. Additionally, the VID change triggers a PWRGD masking timer to prevent a PWRGD failure. Each VID change resets and retriggers the internal PWRGD masking timer.

As listed in Table 3, during a VID transient, the APD3212/NCP3218/NCP3218G forces PWM mode regardless of the state of the system input signals. For example, this means that if the chip is configured as a dual−phase controller but is running in single−phase mode due to a light load condition, a current overload event causes the chip to switch to dual−phase mode to share the excessive load until the delayed current limit latchoff cycle terminates.

In user−set single−phase mode, the APD3212/NCP3218/NCP3218G usually runs in RPM mode. When a VID transition occurs, however, the APD3212/NCP3218/NCP3218G switches to dual−phase PWM mode.

Light Load RPM DCM Operation

In single−phase normal mode, DPRSLP is pulled low and the APD3208 operates in Continuous Conduction Mode (CCM) over the entire load range. The upper and lower MOSFETs run synchronously and in complementary phase. See Figure 21 for the typical waveforms of the

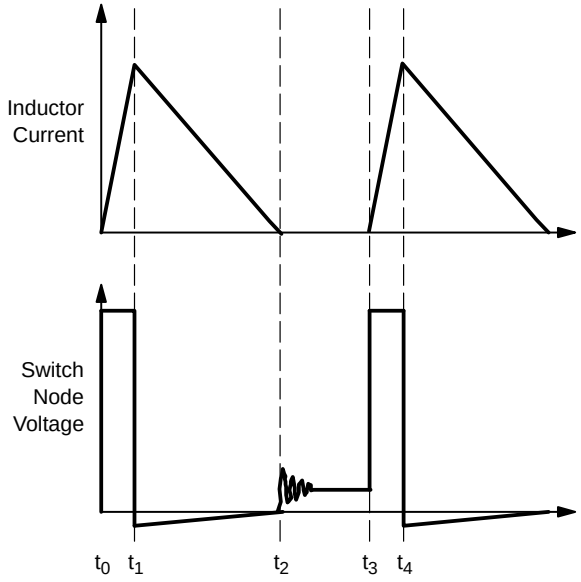


Figure 26. Inductor Current and Switch Node in DCM

Figure 27. Single−

Table 3. VID CODE TABLE (continued)

VID6

Figure 29. Typical Dual−

Application Information

The design parameters for a typical IMVP−6.5−compliant CPU core VR application are as follows:

- Maximum input voltage (V_{INMAX}) = 19 V
- Minimum input voltage (V_{INMIN}) = 8.0 V
- Output voltage by VID setting (V_{VID}) = 1.05 V
- Maximum output current (I_O) = 52 A
- Droop resistance (R_O) = 1.9 mΩ
- Nominal output voltage at 40 A load (V_{OFL}) = 0.9512 V
- Static output voltage drop from no load to full load (ΔV) = V_{ONL} − V_{OFL} = 1.05 V − 0.9512 V = 98 mV
- Maximum output current step (ΔI_O) = 52 A
- Number of phases (n) = 2
- Switching frequency per phase (f_{SW}) = 300 kHz
- Duty cycle at maximum input voltage (D_{MAX}) = 0.13 V
- Duty cycle at minimum input voltage (D_{MIN}) = 0.055 V

Setting the Clock Frequency for PWM

In PWM operation, the APD3212/NCP3218/NCP3218G uses a fixed−frequency control architecture. The frequency is set by an external timing resistor (RT). The clock frequency and the number of phases determine the switching frequency per phase, which relates directly to the switching losses and the sizes of the inductors and input and output capacitors. For a dual−phase design, a clock frequency of 600 kHz sets the switching frequency to 300 kHz per phase. This selection represents the trade−off between the switching losses and the minimum sizes of the output filter components. To achieve a 600 kHz oscillator frequency at a VID voltage of 1.2 V, RT must be 181 kΩ. Alternatively, the value for RT can be calculated by using the following equation:

$$R_T = \frac{V_{VID} + 1.0\ V}{2 \times n \times f_{SW} \times 9\ pF} - 16\ k\Omega \qquad \text{(eq. 1)}$$

where:

9 pF and 16 kΩ are internal IC component values.
V_{VID} is the VID voltage in volts.
n is the number of phases.
f_{SW} is the switching frequency in hertz for each phase.

For good initial accuracy and frequency stability, it is recommended to use a 1% resistor.

When VARFREQ pin is connected to ground, the switching frequency does not change with VID. The value for RT can be calculated by using the following equation.

$$R_T = \frac{1.0\ V}{n \times 2 \times f_{SW} \times 9\ pF} - 16\ k\Omega \qquad \text{(eq. 2)}$$

Setting the Switching Frequency for RPM Operation of Phase 1

During the RPM operation of Phase 1, the APD3212/NCP3218/NCP3218G runs in pseudoconstant frequency if the load current is high enough for continuous current mode. While in DCM, the switching frequency is reduced with the load current in a linear manner.

To save power with light loads, lower switching frequency is usually preferred during RPM operation. However, the V_{CORE} ripple specification of IMVP−6.5 sets a limitation for the lowest switching frequency. Therefore, depending on the inductor and output capacitors, the switching frequency in RPM can be equal to, greater than, or less than its counterpart in PWM.

A resistor from RPM to GND sets the pseudo constant frequency as following:

$$R_{RPM} = \frac{2 \times R_T}{V_{VID} + 1.0\ V} \times \frac{A_R \times (1 - D) \times V_{VID}}{R_R \times C_R \times f_{SW}} - 0.5\ k\Omega \qquad \text{(eq. 3)}$$

where:

A_R is the internal ramp amplifier gain.
C_R is the internal ramp capacitor value.
R_R is an external resistor on the RAMPADJ pin to set the internal ramp magnitude.

Soft Start and Current Limit Latch−Off Delay Times

Inductor Selection

The choice of inductance determines the ripple current of the inductor. Less inductance results in more ripple current, which increases the output ripple voltage and the conduction losses in the MOSFETs. However, this allows the use of smaller−size inductors, and for a specified peak−to−peak transient deviation, it allows less total output capacitance. Conversely, a higher inductance results in lower ripple current and reduced conduction losses, but it requires larger−size inductors and more output capacitance for the same peak−to−peak transient deviation. For a multi−phase converter, the practical value for peak−to−peak inductor ripple current is less than 50% of the maximum dc current of that inductor. Equation 4 shows the relationship between the inductance, oscillator frequency, and peak−to−peak ripple current. Equation 5 can be used to determine the minimum inductance based on a given output ripple voltage.

$$I_R = \frac{V_{VID} \times (1 - D_{MIN})}{f_{SW} \times L} \qquad \text{(eq. 4)}$$

L

The following procedure and expressions yield values for R_{CS1}, R_{CS2}, and R_{TH} (the thermistor value at 25°C) for a given R_{CS} value.

1. Select an NTC to be used based on its type and value. Because the value needed is not yet determined, start with a thermistor with a value close to R_{CS} and an NTC with an initial tolerance of better than 5%.
2. Find the relative resistance value of the NTC at two temperatures. The appropriate temperatures will depend on the type of NTC, but 50°C and 90°C have been shown to work well for most types of NTCs. The resistance values are called A (A is $R_{TH}(50°C)/R_{TH}(25°C)$) and B (B is $R_{TH}(90°C)/R_{TH}(25°C)$). Note that the relative value of the NTC is always 1 at 25°C.
3. Find the relative value of R_{CS} required for each of the two temperatures. The relative value of R_{CS} is based on the percentage of change needed, which is initially assumed to be 0.39%/°C in this example.
   The relative values are called r_1 (r_1 is $1/(1+ TC \times (T_1 - 25))$) and r_2 (r_2 is $1/(1 + TC \times (T_2 - 25))$), where TC is 0.0039, T_1 is 50°C, and T_2 is 90°C.
4. Compute the relative values for r_{CS1}, r_{CS2}, and r_{TH}

To meet the conditions of these expressions and the transient response, the ESR of the bulk capacitor bank (R_X

The most effective way to reduce switching loss is to use lower gate capacitance devices.

The conduction loss of the main MOSFET is given by the following equation:

$$P_{C(MF)} = D \times \left[\left(\frac{I_O}{n_{MF}} \right)^2 + \frac{1}{12} \times \left(\frac{n \times I_R}{n_{MF}} \right)^2 \right] \times R_{DS(MF)} \quad \text{(eq. 16)}$$

where $R_{DS(MF)}$ is the on resistance of the MOSFET.

Typically, a user wants the highest speed (low C_{ISS}) device for a main MOSFET, but such a device usually has higher on resistance. Therefore, the user must select a device that meets the total power dissipation (about 0.8 W to 1.0 W for an 8−lead SOIC) when combining the switching and conduction losses.

For example, an IRF7821 device can be selected as the main MOSFET (four in total; that is, n_{MF} = 4), with approximately
C_{ISS} = 1010 pF (maximum) and $R_{DS(MF)}$ = 18 mΩ (maximum at T_J = 120°C), and an IR7832 device can be selected as the synchronous MOSFET (four in total; that is, n_{SF} = 4), with
$R_{DS(SF)}$ = 6.7 mΩ (maximum at T_J = 120°C). Solving for the power dissipation per MOSFET at I_O = 40 A and I_R = 9.0 A yields 630 mW for each synchronous MOSFET and 590 mW for each main MOSFET. A third synchronous MOSFET is an option to further increase the conversion efficiency and reduce thermal stress.

Finally, consider the power dissipation in the driver for each phase. This is best described in terms of the Q_G for the MOSFETs and is given by the following equation:

$$P_{DRV} = \left[\frac{f_{SW}}{2 \times n} \times (n_{MF} \times Q_{GMF} + n_{SF} \times Q_{GSF}) + I_{CC} \right] \times VCC \quad \text{(eq. 17)}$$

where Q_{GMF} is the total gate charge for each main MOSFET, and Q_{GSF} is the total gate charge for each synchronous MOSFET.

The previous equation also shows the standby dissipation (I_{CC} times the VCC) of the driver.

Ramp Resistor Selection

The ramp resistor (R_R) is used to set the size of the internal PWM ramp. The value of this resistor is chosen to provide the best combination of thermal balance, stability, and transient response. Use the following expression to determine a starting value:

$$R_R = \frac{A_R \times L}{3 \times A_D \times R_{DS} \times C_R} \quad \text{(eq. 18)}$$

$$R_R = \frac{0.5 \times 360\ \text{nH}}{3 \times 5 \times 5.2\ \text{m}\Omega \times 5\ \text{pF}} = 462\ \text{k}\Omega$$

where:

A_R is the internal ramp amplifier gain.
A_D is the current balancing amplifier gain.
R_{DS} is the total low−side MOSFET on resistance.
C_R is the internal ramp capacitor value.

Another consideration in the selection of R_R is the size of the internal ramp voltage (see Equation 19). For stability and noise immunity, keep the ramp size larger than 0.5 V. Taking this into consideration, the value of R_R in this example is selected as 280 kΩ.

The internal ramp voltage magnitude can be calculated as follows:

$$V_R = \frac{A_R \times (1 - D) \times V_{VID}}{R_R \times C_R \times f_{SW}} \quad \text{(eq. 19)}$$

$$V_R = \frac{0.5 \times (1 - 0.061) \times 1.150\ \text{V}}{462\ \text{k}\Omega \times 5\ \text{pF} \times 280\ \text{kHz}} = 0.83\ \text{V}$$

The size of the internal ramp can be increased or decreased. If it is increased, stability and transient response improves but thermal balance degrades. Conversely, if the ramp size is decreased, thermal balance improves but stability and transient response degrade. In the denominator of Equation 18, the factor of 3 sets the minimum ramp size that produces an optimal combination of good stability, transient response, and thermal balance.

Current Limit Setpoint

To select the current limit setpoint, the resistor value for R_{CLIM} must be determined. The current limit threshold for the APD3212/NCP3218/NCP3218G is set with R_{CLIM}. R_{CLIM} can be found using the following equation:

$$R_{LIM} = \frac{I_{LIM} \times R_O}{60\ \mu\text{A}} \quad \text{(eq. 20)}$$

where:

R_{LIM} is the current limit resistor.
R_O is the output load line.
I_{LIM} is the current limit setpoint.

When the APD3212/NCP3218/NCP3218G is configured for 3 phase operation, the equation above is used to set the current limit. When the APD3212/NCP3218/NCP3218G switches from 3 phase to 1 phase operation by $\overline{\text{PSI}}$ or DPRSLP signal, the current is single phase is one third of the current limit in 3 phase.

When the APD3212/NCP3218/NCP3218G is configured for 2 phase operation, the equation above is used to set the current limit. When the APD3212/NCP3218/NCP3218G switches from 2 phase to 1 phase operation by $\overline{\text{PSI}}$ or DPRSLP signal, the current is single phase is one half of the current limit in 2 phase.

When the APD3212/NCP3218/NCP3218G is configured for 1 phase operation, the equation above is used to set the current limit.

Current Monitor

The APD3212/NCP3218/NCP3218G has output current monitor. The IMON pin sources a current proportional to the total inductor current. A resistor, R_{MON}, from IMON to FBRTN sets the gain of the output current monitor. A 0.1 μF is placed in parallel with R_{MON} to filter the inductor current

The compensation values can be calculated as follows:

$$C_A = \frac{n \times R_O \times T_A}{R_E \times R_B} \quad \text{(eq. 31)}$$

$$R_A = \frac{T_C}{C_A}$$

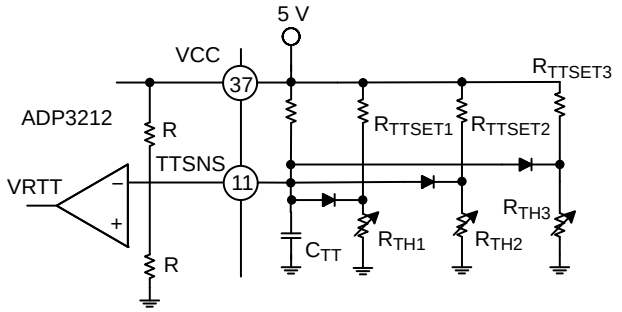


Figure 34. Multiple−Point Thermal Monitoring

The number of hot spots monitored is not limited. The alarm temperature of each hot spot can be individually set by using different values for R_{TTSET1}, R_{TTSET2}, ... R_{TTSETn}.

Tuning Procedure for APD3212/NCP3218/NCP3218G

Set Up and Test the Circuit

1. Build a circuit based on the compensation values computed from the design spreadsheet.
2. Connect a dc load to the circuit.
3. Turn on the APD3212/NCP3218/NCP3218G and verify that it operates properly.
4. Check for jitter with no load and full load conditions.

Set the DC Load Line

1. Measure the output voltage with no load (V_{NL}) and verify that this voltage is within the specified tolerance range.
2. Measure the output voltage with a full load when the device is cold (V_{FLCOLD}). Allow the board to run for ~10 minutes with a full load and then measure the output when the device is hot (V_{FLHOT}). If the difference between the two measured voltages is more than a few millivolts, adjust R_{CS2} using Equation 40.

$$R_{CS2(NEW)} = R_{CS2(OLD)} \times \frac{V_{NL} - V_{FLCOLD}}{V_{NL} - V_{FLHOT}} \quad \text{(eq. 40)}$$

3. Repeat Step 2 until no adjustment of R_{CS2} is needed.
4. Compare the output voltage with no load to that with a full load using 5 A steps. Compute the load line slope for each change and then find the average to determine the overall load line slope (R_{OMEAS}).
5. If the difference between R_{OMEAS} and R_O is more than 0.05 mΩ, use the following equation to adjust the R_{PH} values:

$$R_{PH(NEW)} = R_{PH(OLD)} \times \frac{R_{OMEAS}}{R_O} \quad \text{(eq. 41)}$$

6. Repeat Steps 4 and 5 until no adjustment of R_{PH} is needed. Once this is achieved, do not change R_{PH}, R_{CS1}, R_{CS2}, or R_{TH} for the rest of the procedure.
7. Measure the output ripple with no load and with a full load with scope, making sure both are within the specifications.

Set the AC Load Line

1. Remove the dc load from the circuit and connect a dynamic load.
2. Connect the scope to the output voltage and set it to dc coupling mode with a time scale of 100 μs/div.
3. Set the dynamic load for a transient step of about 40 A at 1 kHz with 50% duty cycle.
4. Measure the output waveform (note that use of a dc offset on the scope may be necessary to see the waveform). Try to use a vertical scale of 100 mV/div or finer.
5. The resulting waveform will be similar to that shown in Figure 35. Use the horizontal cursors to measure V_{ACDRP} and V_{DCDRP}, as shown in Figure 35. Do not measure the undershoot or overshoot that occurs immediately after the step.

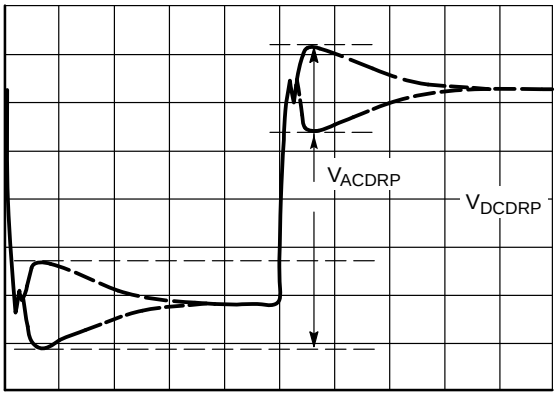


Figure 35. AC Load Line Waveform

dynamic loads have an excessive overshoot at powerup if a minimum current is incorrectly set (this is an issue if a VTT tool is in use).

Set the Initial Transient

1. With the dynamic load set at its maximum step size, expand the scope time scale to 2 μs/div to 5 μs/div. This results in a waveform that may have two overshoots and one minor undershoot before achieving the final desired value after V_{DROOP} (see Figure 36).

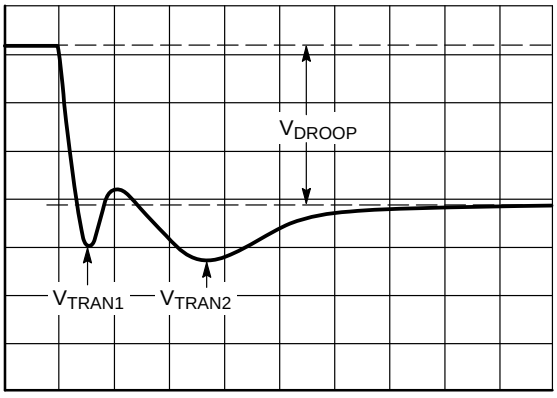


Figure 36. Transient Setting Waveform, Load Step

2. If both overshoots are larger than desired, try the following adjustments in the order shown.

a. Increase the resistance of the ramp resistor (R_{RAMP}) by 25%.

b. For V_{TRAN1}, increase C_B or increase the switching frequency.

c. For V_{TRAN2}, increase R_A by 25% and decrease C_A by 25%.

If these adjustments do not change the response, it is because the system is limited by the output decoupling. Check the output response and the switching nodes each time a change is made to ensure that the output decoupling is stable.

3. For load release (see Figure 37), if $V_{TRANREL}$ is larger than the value specified by IMVP−6.5, a greater percentage of output capacitance is needed. Either increase the capacitance directly or decrease the inductor values. (If inductors are changed, however, it will be necessary to redesign the circuit using the information from the spreadsheet and to repeat all tuning guide procedures).

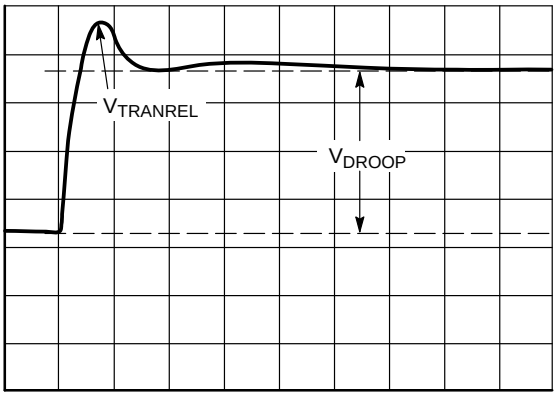


Figure 37. Transient Setting Waveform, Load Release

Layout and Component Placement

The following guidelines are recommended for optimal performance of a switching regulator in a PC system.

General Recommendations

1. For best results, use a PCB of four or more layers. This should provide the needed versatility for control circuitry interconnections with optimal placement; power planes for ground, input, and output; and wide interconnection traces in the rest of the power delivery current paths. Keep in mind that each square unit of 1 oz copper trace has a resistance of ~0.53 mΩ at room temperature.
2. When high currents must be routed between PCB layers, vias should be used liberally to create several parallel current paths so that the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.
3. If critical signal lines (including the output voltage sense lines of the APD3212/NCP3218/ NCP3218G) must cross through power circuitry, it is best if a signal ground plane can be interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of increasing signal ground noise.
4. An analog ground plane should be used around and under the APD3212/NCP3218/NCP3218G for referencing the components associated with the controller. This plane should be tied to the nearest ground of the output decoupling capacitor, but should not be tied to any other power circuitry to prevent power currents from flowing into the plane.

5. The components around the APD3212/NCP3218/ NCP3218G should be located close to the controller with short traces. The most important traces to keep short and away from other traces are