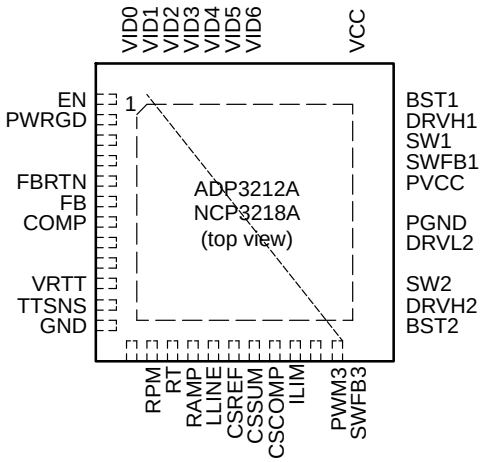
PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
V_{CC}, PV_{CC1}, PV_{CC2}	−0.3 to +6.0	V
FBRTN, PGND1, PGND2	−0.3 to +0.3	V
BST1, BST2, DRVH1, DRVH2 DC t < 200 ns	 −0.3 to +28 −0.3 to +33	V
BST1 to PV_{CC}, BST2 to PV_{CC} DC t < 200 ns	 −0.3 to +22 −0.3 to +28	V
BST1 to SW1, BST2 to SW2	−0.3 to +6.0	V
SW1, SW2 DC t < 200 ns	 −1.0 to +22 −6.0 to +28	V

PIN ASSIGNMENT

Pin No.	Mnemonic	Description

ELECTRICAL CHARACTERISTICS
V_{CC} = PV_{CC}

ELECTRICAL CHARACTERISTICS

V_{CC} = PV_{CC} = 5.0 V, FBRTN = PGND = GND = 0 V, H = 5.0 V, L = 0 V, EN = VARFREQ = H, DPRSLP = L, $\overline{PSI}$ = 1.05 V, V_{VID} = V_{DAC} = 1.2000 V, T_A = −40°C to 100°C, unless otherwise noted. (Note 1) Current entering a pin (sink current) has a positive sign.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VOLTAGE MONITORING and PROTECTION − POWER GOOD						
CSREF Crowbar Voltage Threshold	$V_{CBCSREF}$	Relative to FBRTN	1.5	1.55	1.6	V
CSREF Reverse Voltage Threshold	$V_{RVCSREF}$	Relative to FBRTN, latchoff mode CSREF is falling CSREF is rising	 −350	 −300 −75	 −10	mV
PWRGD Low Voltage	V_{PWRGD}	$I_{PWRGD(SINK)}$ = 4 mA		85	250	mV
PWRGD High, Leakage Current	I_{PWRGD}	V_{PWRDG} = 5.0 V			1.0	μA
PWRGD Startup Delay	$T_{SSPWRGD}$	Measured from $\overline{CLKEN}$ neg edge to PWRGD pos edge		9.0		ms
PWRGD Latchoff Delay	$T_{LOFFPWRGD}$	Measured from Out−off−Good−Window event to Latchoff (switching stops)		9.0		μs
PWRGD Propagation Delay (Note 3)	$T_{PDPWRGD}$	Measured from Out−off−Good−Window event to PWRGD neg edge		200		ns
Crowbar Latchoff Delay (Note 2)	T_{LOFFCB}	Measured from Crowbar event to latchoff (switching stops)		200		ns
PWRGD Masking Time		Triggered by any VID change or OCP event		100		μs
CSREF Soft−Stop Resistance		EN = L or latchoff condition		70		Ω
CURRENT CONTROL − CURRENT−SENSE AMPLIFIER (CSAMP)						
CSSUM, CSREF Common−Mode Range (Note 2)		Voltage range of interest	0		2.0	V
CSSUM, CSREF Offset Voltage	V_{OSCSA}	CSREF – CSSUM, T_A = 25°C T_A = −10°C to 85°C T_A = −40°C to 85°C	−0.5 −1.7 −1.9		+0.5 +1.7 +1.9	mV
CSSUM Bias Current	I_{BCSSUM}		−50		+50	nA
CSREF Bias Current	I_{BCSREF}		−2.0		+2.0	μA
CSCOMP Voltage Range (Note 2)		Voltage range of interest	0.05		2.0	V
CSCOMP Current	$I_{CSCOMPsource}$	CSSUM forced 200 mV below CSREF		−750		μA
	$I_{CSCOMPsink}$	CSSUM forced 200 mV above CSREF		1.0		mA
CSCOMP Slew Rate (Note 2)		C_{CSCOMP} = 10 pF, CSREF = VDAC, Open loop configuration CSSUM forced 200 mV below CSREF CSSUM forced 200 mV above CSREF		 20 −20		V/μs
Gain Bandwidth (Note 2)	GBW_{CSA}	Non−inverting unit gain configuration R_{FB} = 1 kΩ		20		MHz
CURRENT MONITORING and PROTECTION CURRENT REFERENCE						
I_{REF} Voltage	V_{REF}	R_{REF} = 80 kΩ to set I_{REF} = 20 μA	1.55	1.6	1.65	V
CURRENT LIMITER (OCP)						
Current Limit (OCP) Threshold	V_{LIMTH}	Measured from CSCOMP to CSREF, R_{LIM} = 1.5 kΩ, 3−ph configuration, $\overline{PSI}$ = H 3−ph configuration, $\overline{PSI}$ = L 2−ph configuration, $\overline{PSI}$ = H 2−ph configuration, $\overline{PSI}$ = L 1−ph configuration	 −80 −22 −80 −35 −75	 −90 −30 −90 −45 −90	 −100 −38 −100 −55 −105	mV
Current Limit Latchoff Delay		Measured from OCP event to PWRGD de−assertion		150		μs

1. All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).
2. Guaranteed by design or bench characterization, not production tested.
3. Based on bench characterization data.
4. Timing is referenced to the 90% and 10% points, unless otherwise noted.

ELECTRICAL CHARACTERISTICS

V_{CC} = PV_{CC} = 5.0 V, FBRTN = PGND = GND = 0 V, H = 5.0 V, L = 0 V, EN = VARFREQ = H, DPRSLP = L, $\overline{PSI}$ = 1.05 V, V_{VID} = V_{DAC} = 1.2000 V, T_A = −40°C to 100°C, unless otherwise noted. (Note 1) Current entering a pin (sink current) has a positive sign.

Parameter	Symbol	Conditions	Min	Typ	Max	Units

TEST CIRCUITS

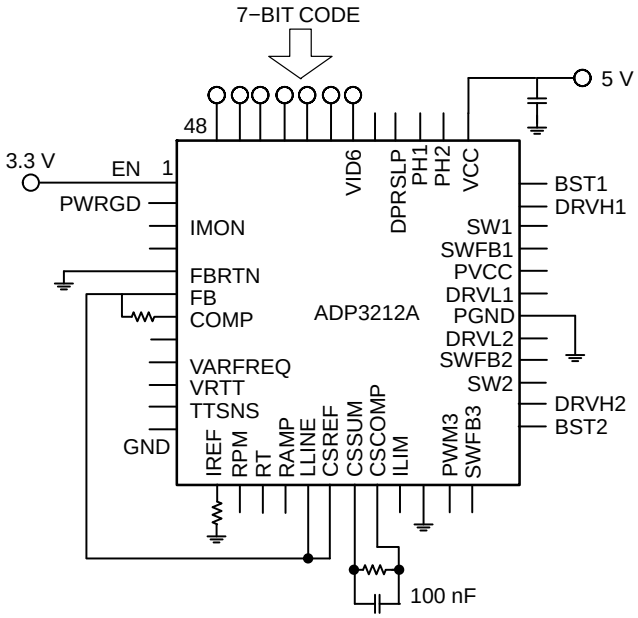


Figure 3. Closed−Loop Output Voltage Accuracy

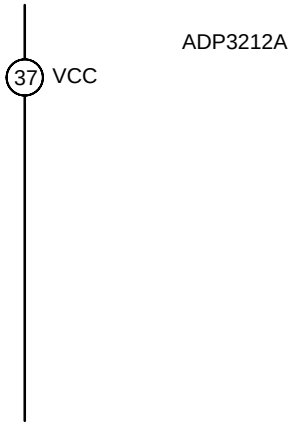


Figure 4. Current Sense Amplifier, V_{OS}

Figure 5. Positioning Accuracy

Theory of Operation

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– –
–
– – –
–
–

Table 2. PHASE NUMBER AND OPERATION MODES (Note 1)

–

Differential Sensing of Output Voltage

– – Δ

– ±

μ

Output Current Sensing

–

-
-
-

Ω

Ω

Ω

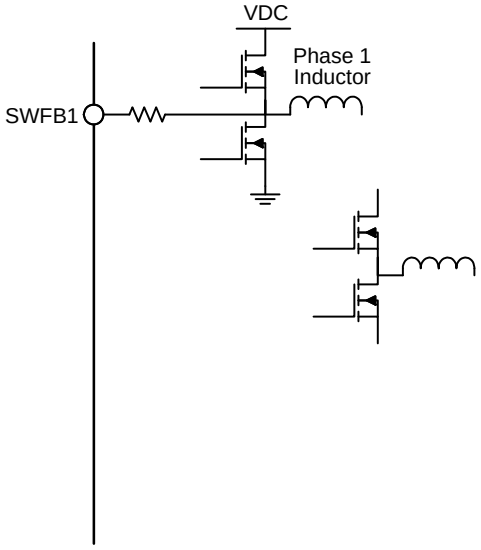

Figure 19. Current Balance Resistors

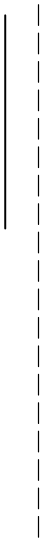

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Table 3. VID CODE TABLE (continued)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output (V)
0	1	0	0	0	0	0	1.1000 V
0	1	0	0	0	0	1	

Table 3. VID CODE TABLE (continued)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output (V)
1	0	1	0	0	0	1	0.4875 V
1	0	1	0	0	1	0	0.4750 V
1	0	1	0	0	1	1	0.4625 V
1	0	1	0	1	0	0	0.4500 V
1	0	1	0	1	0	1	0.4375 V
1	0	1	0	1	1	0	0.4250 V
1	0	1	0	1	1	1	0.4125 V
1	0	1	1	0	0	0	0.4000 V
1	0	1	1	0	0	1	0.3875 V
1	0	1	1	0	1	0	0.3750 V
1	0	1	1	0	1	1	0.3625 V
1	0	1	1	1	0	0	0.3500 V
1	0	1	1	1	0	1	0.3375 V

1100000001000c(1)TjET59.811 50TjET59.811 538.4490.1f59.811 563.414 49.323 .907486.5BT8 0 0 8 131.4142 554.910498.6(0)TjET1 34 551.3

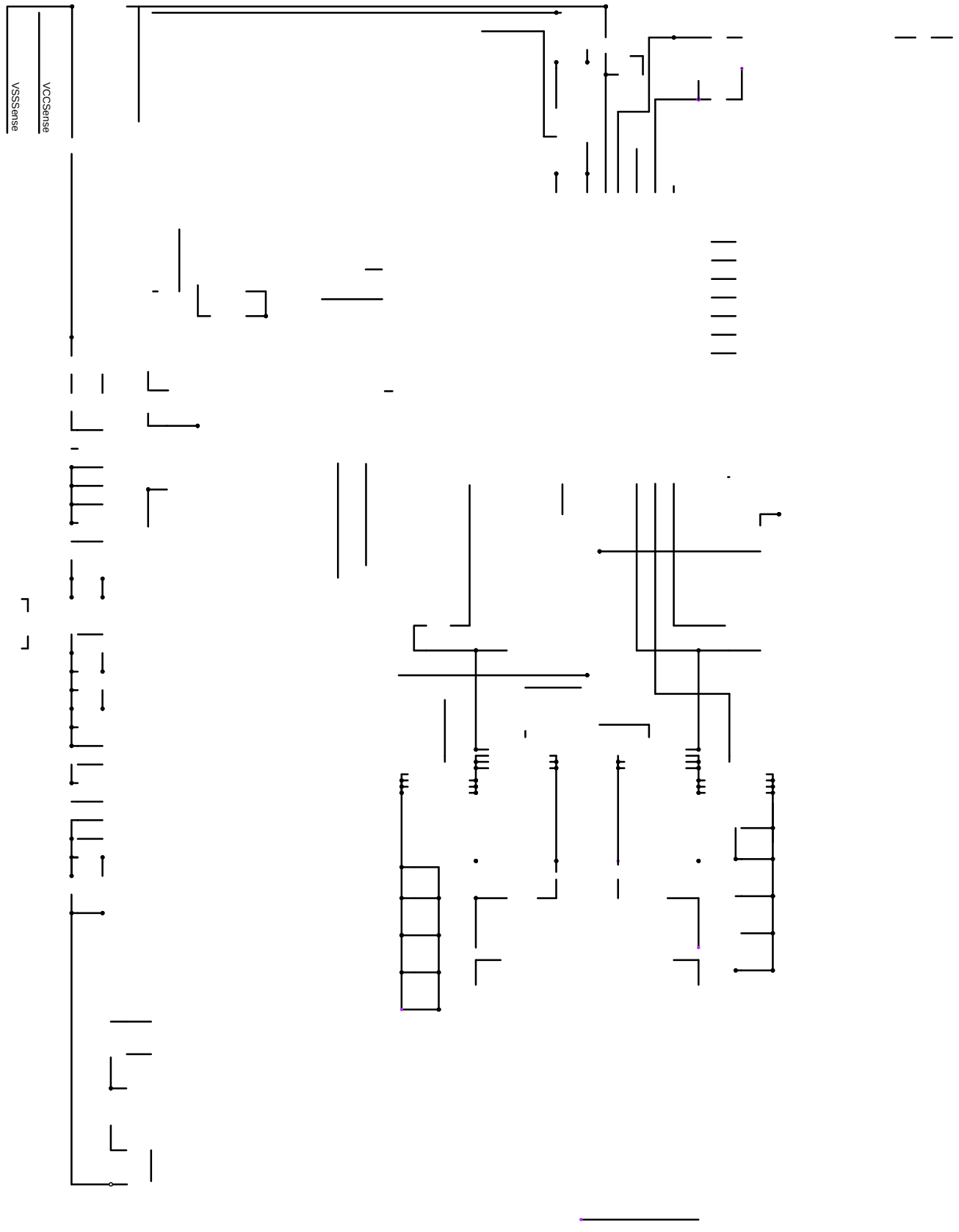

Figure 29. Typical Dual−Phase Application Circuit

Application Information

– –

-
-
-
-
- Ω
-
-
- Δ – –
- Δ
-
- f
-
-

Setting the Clock Frequency for PWM

–

–

–

Ω

$R_T = V_{VID}$

$$R_O = \frac{R_{CS}}{R_{PH(x)}} \times R_{SENSE} \quad \text{(eq. 6)}$$

$$C_{CS} = \frac{L}{R_{SENSE} \times R_{CS}} \quad \text{(eq. 7)}$$

Ω

Selecting a Standard Inductor

Ω
Ω

$$C_{CS} = \frac{330\ \text{nH}}{0.8\ \text{m}\Omega \times 200\ \text{k}\Omega} = 2.1\ \text{nF}$$

Power Inductor Manufacturers

–

Ω

Ω

- –
- –
- –
- –

$$R_{PH(x)} \geq \frac{0.8\ \text{m}\Omega}{2.1\ \text{m}\Omega} \times 220\ \text{k}\Omega = 83.8\ \text{k}\Omega$$

Ω

Inductor DCR Temperature Correction

Output Droop Resistance

–

°

–

μ –

μ

μ

$$C_{X(MIN)} \geq \left\{ \frac{330\ nH \times 27.9\ A}{2 \times \left(2.1\ m\Omega + \frac{10\ mV}{27.9\ A}\right) \times 1.4375\ V} - 300\ \mu F \right\} = 1.0\ mF$$

$$C_{X(MAX)} \leq \frac{330\ nH \times 220\ mV}{2 \times 3.1^2 \times (2.1\ m\Omega)^2 \times 1.4375\ V} \times$$

(

$P_{C(MF)} = D \times$

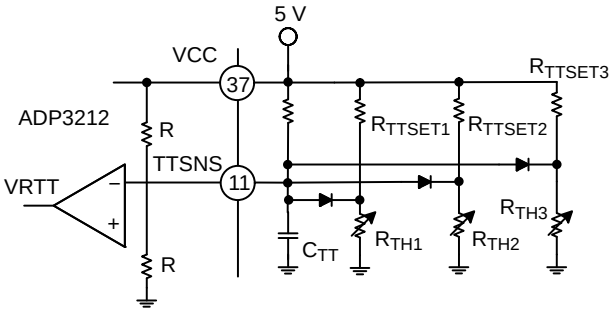

Figure 34. Multiple−Point Thermal Monitoring

Tuning Procedure for APD3212A/NCP3218A

Set Up and Test the Circuit

Set the DC Load Line

$$R_{CS2(NEW)} = R_{CS2(OLD)} \times \frac{V_{NL} - V_{FLCOLD}}{V_{NL} - V_{FLHOT}} \quad \text{(eq. 40)}$$

Set the Initial Transient

μ

μ

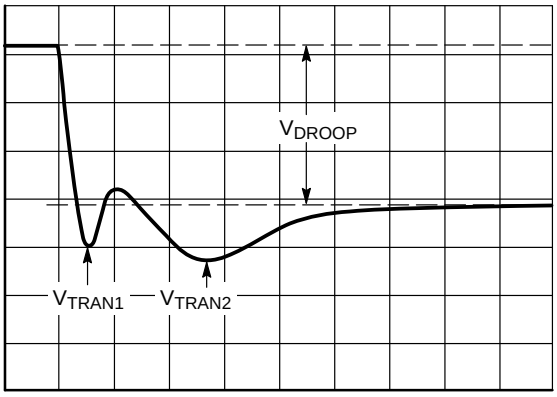

Figure 36. Transient Setting Waveform, Load Step

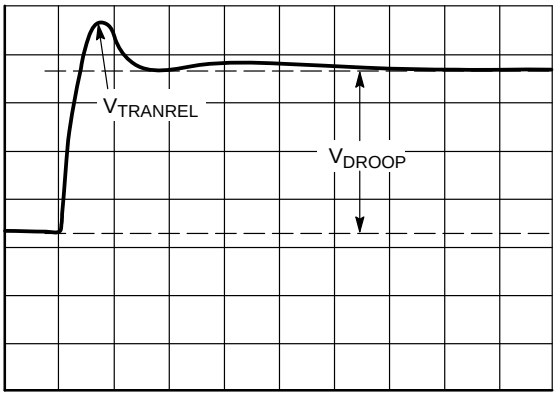

Figure 37. Transient Setting Waveform, Load Release

Layout and Component Placement

General Recommendations

Ω

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