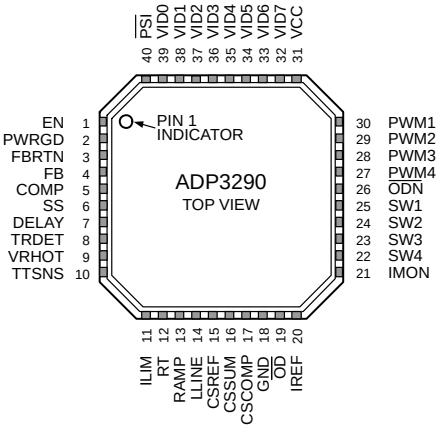
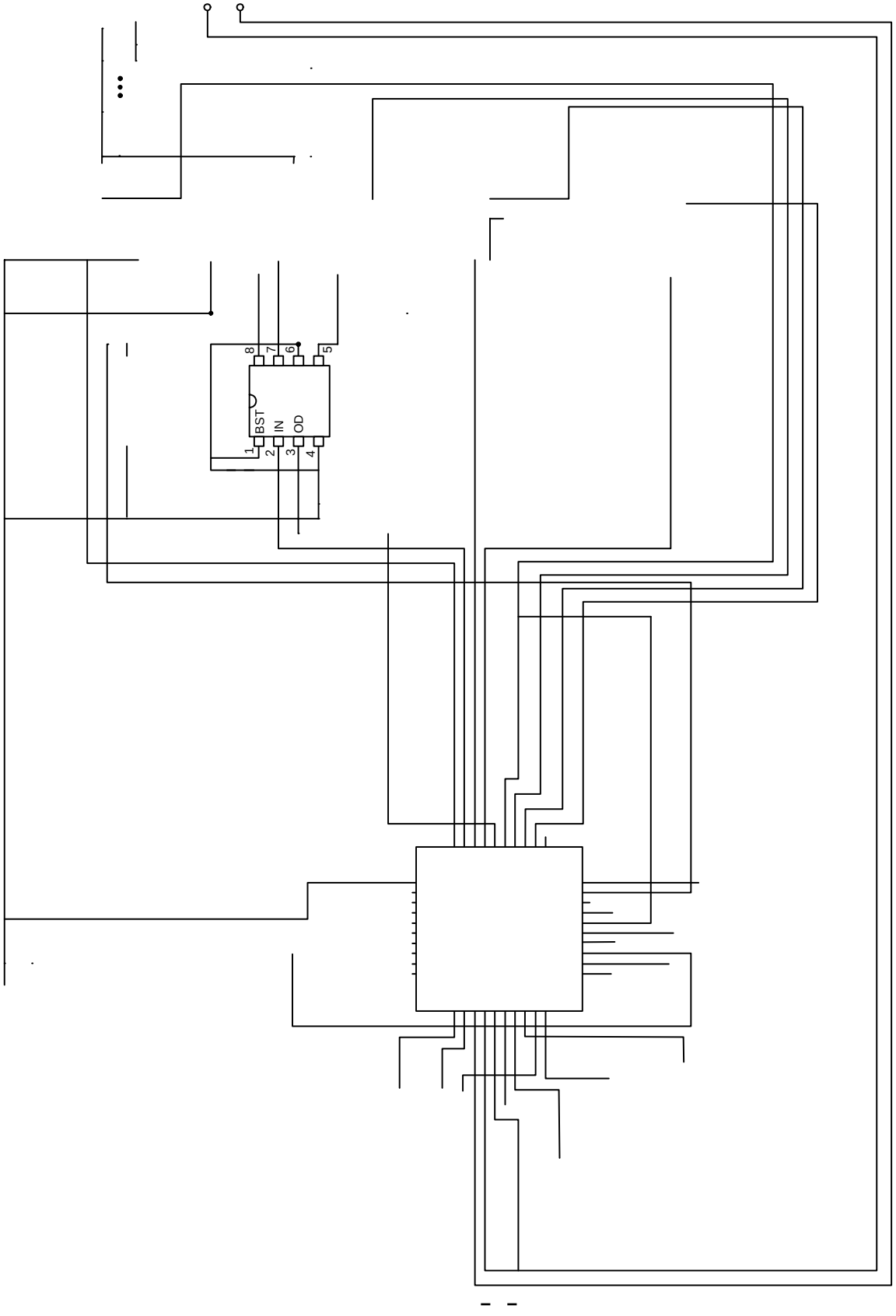
- ±7 mV Worse−Case Differential Sensing Error
- Logic−Level PWM Outputs for Interface to External High Power Drivers
- Fast−Enhanced PWM FlexMode™ for Excellent Load Transient Performance
- TRDET to Improve Load Release
- Active Current Balancing Between All Output Phases
- Built−In Power−Good/Crowbar Blanking Supports Dynamic VID Code Changes
- Digitally Programmable 0.5 V to 1.6 V Output Supports VR11.1 Specification
- Programmable Overcurrent Protection with Programmable Latchoff Delay
- This is a Pb−Free Device



- Desktop PC Power Supplies for:
  - Next Generation Intel® Processors
  - VRM Modules


8
7
6
5
BST
IN
OD
1
2
3
4

Supply Voltage	V_{CC}	−0.3 to +6	V
FBRTN	V_{FBRTN}	−0.3 to +0.3	V
PWM3 to PWM4, Rampadj		−0.3 to V_{CC} +0.3	V
SW1 to SW4		−5 to +25	V
SW1 to SW4 <200 ns		−10 to +25	V
All other Inputs and Outputs		−0.3 to V_{CC} +0.3	V
Storage Temperature Range			

1	EN	Power Supply Enable Input. Pulling this pin to GND disables the PWM outputs and pulls the PWRGD output low.
2	PWRGD	Power−Good Output. Open−drain output that signals when the output voltage is outside of the proper operating range.
3	FBRTN	Feedback Return. VID DAC and error amplifier input for remote sensing of the output voltage.
4	FB	Feedback Input. Error amplifier reference for remote sensing of the output voltage. An external resistor between this pin and the output voltage sets the no−load offset point.
5	COMP	

(V_{CC} = 12 V, FBRTN = GND, T_A = 0°C to 85°C unless otherwise noted) (Note 1)

(V_{CC} = 12 V, FBRTN = GND, T_A = 0°C to 85°C unless otherwise noted) (Note 1)

cont.						
TTSNS VRHOT Threshold Voltage			715	760	805	mV
TTSNS Hysteresis				50		mV
VRHOT Output Low Voltage	$V_{OL(VRHOT)}$	$I_{VRHOT(SINK)}$ = −4 mA, TTSNS = 5.0 V		150	300	

The ADP3290 combines a multi−mode, fixed frequency PWM control with multiphase logic outputs for use in 2−, 3−, or 4−phase synchronous buck CPU core supply power converters. The internal VID DAC is designed to interface with Intel 8−bit VRD/VRM 11.1 and compatible CPUs. Multiphase operation is important for producing the high currents and low voltages demanded by today’s microprocessors. Handling the high currents in a single−phase converter places high thermal

The clock frequency of the ADP3290 is set with an external resistor connected from the RT pin to ground. The frequency follows the graph in Figure 3. To determine the frequency per phase, the clock is divided by the number of phases in use. If all phases are in use, divide by 4. If PWM4 is tied to V_{CC}, divide by 3. If PWM4 and PWM3 are tied to V_{CC}, divide by 2.

NOTE: Single−Phase operation is also possible; contact ON Semiconductor for more details.

The ADP3290 combines differential sensing with a high accuracy VID DAC and reference, and a low offset error amplifier. This maintains a worst−case specification of ±7.0 mV differential sensing error over its full operating output voltage and with tighter accuracy over a 0 °C to 60 °C temperature range. The output voltage is sensed between the FB pin and FBRTN pin. FB is connected through a resistor to the regulation point, usually the remote sense pin of the microprocessor. FBRTN is connected directly to the remote sense ground point. The internal VID DAC and precision reference are referenced to FBRTN, which has a minimal current of 125 A to allow accurate remote sensing. The internal error amplifier compares the output of the DAC to the FB pin to regulate the output voltage.

The ADP3290 provides a dedicated current sense amplifier (CSA) to monitor the total output current for proper voltage positioning versus load current, for the I_{MON} output, and for current limit detection. Sensing the load current at the output gives the total real−time current being delivered to the load, which is an inherently more accurate method than peak current detection or sampling the current across a sense element such as the low−side MOSFET. This amplifier can be configured several ways, depending on the objectives of the system, as follows:

- Output inductor DCR sensing without a thermistor for lowest cost.
- Output inductor DCR sensing with a thermistor for improved accuracy with tracking of inductor temperature.
- Sense resistors for highest accuracy measurements.

The positive input of the CSA is connected to the CSREF pin, which is connected to the average output voltage. The inputs to the amplifier are summed together through resistors from the sensing element, such as the switch node side of the output inductors, to the inverting input CSSUM. The feedback resistor between CSCOMP and CSSUM sets the gain of the amplifier and a filter capacitor is placed in parallel with this resistor. The gain of the amplifier is programmable by adjusting the input summing resistor.

An additional resistor divider connected between CSREF and CSCOMP (with the midpoint connected to LLINE) can be used to set the load line required by the microprocessor. The current information is then given as CSREF − LLINE. This difference signal is used internally to offset the VID DAC for voltage positioning. The difference between CSREF and CSCOMP is then used as a differential input for the current limit comparator. This allows the load line to be set independently of the current limit threshold. In the event that the current limit threshold and load line are not independent, the resistor divider between CSREF and CSCOMP can be removed and the CSCOMP pin can be directly connected to LLINE. To disable voltage positioning entirely (that is, no load line) connect LLINE to CSREF.

To provide the best accuracy for sensing current, the CSA is designed to have a low offset input voltage. Also, the sensing gain is determined by external resistors to make it extremely accurate.

For controlling the dynamic output voltage droop as a function of output current, a signal proportional to the total output current at the LLINE pin can be scaled to equal the regulator droop impedance multiplied by the output current. This droop voltage is then used to set the input control voltage to the system. The droop voltage is subtracted from the DAC reference input voltage to tell the error amplifier where the output voltage should be. This allows enhanced feed−forward response.

The ADP3290 has individual inputs (SW1 to SW4) for each phase that are used for monitoring the current of each phase. This information is combined with an internal ramp to create a current balancing feedback system that has been optimized for initial current balance accuracy and dynamic thermal balancing during operation. This current balance information is independent of the average output current information used for positioning as described in the Load Line Setting section.

The magnitude of the internal ramp can be set to optimize the transient response of the system. It also monitors the supply voltage for feed−forward control for changes in the supply. A resistor connected from the power input voltage to the RAMP pin determines the slope of the internal PWM ramp.

External resistors can be placed in series with individual phases to create an intentional current imbalance if desired, such as when one phase has better cooling and can support higher currents. Resistor R_{SW1} through R_{SW4} can be used for adjusting thermal balance. It is best to have the ability to add these resistors during the initial design, therefore, ensure that placeholders are provided in the layout.

To increase the current in any given phase, enlarge R_{SW} for that phase (make R_{SW} = 0 for the hottest phase and do not change it during balancing). Increasing R_{SW} by 1 k can make an increase in phase current. Increase each R_{SW} value by small amounts to achieve balance, starting with the coolest phase first.

A high gain, bandwidth voltage mode error amplifier is used for the voltage mode control loop. The control input voltage to the positive input is set via the VID logic according to the voltages listed.

This voltage is also offset by the droop voltage for active positioning of the output voltage as a function of current, commonly known as active voltage positioning. The output of the amplifier is the COMP pin, which sets the termination voltage for the internal PWM ramps.

The negative input (FB) is tied to the output sense location with Resistor R_B and is used for sensing and controlling the output voltage at this point. A current source from the FB pin flowing through R_B is used for setting the no load offset voltage from the VID voltage. The no load voltage is negative with respect to the VID DAC. The main loop compensation is incorporated into the feedback network between FB and COMP.

The ADP3290 incorporates enhanced transient response for both load steps and load release. For load steps, it senses the error amp to determine if a load step has occurred and sequences the proper number of phases on to ramp up the output current.

For load release, it also senses the error amp and uses the load release information to trigger the TRDET pin, which is then used to adjust the feedback for optimal positioning especially during high frequency load steps.

Additional information is used during load transients to ensure proper sequencing and balancing of phases during high frequency load steps as well as minimizing stress on the components such as the input filter and MOSFETs.

The delay times for the startup timing sequence are set with a capacitor from the DELAY pin to ground. In UVLO, or when EN is logic low, the DELAY pin is held at ground. After the UVLO and EN signals are asserted, the first delay time (TD1 in Figure 5) is initiated. A 15 A current flows out of the DELAY pin to charge C_{DLY}. A comparator monitors the DELAY voltage with a threshold of 1.7 V. The delay time is therefore set by the 15 A charging a capacitor from 0 V to 1.7 V. This DELAY pin is used for multiple delay timings (TD1, TD3, and TD5) during the startup sequence. Also, DELAY is used for timing the current limit latchoff, as explained in the Current Limit, Short−Circuit, and Latchoff Protection section.

The soft−start times for the output voltage are set with a capacitor from the SS pin to ground. After TD1 and the phase detection cycle have been completed, the SS time (TD2 in Figure 5) starts. The SS pin is disconnected from GND, and the capacitor is charged up to the 1.1 V boot voltage by the SS amplifier, which has a limited output current of 15 A. The voltage at the FB pin follows the ramping voltage on the SS pin, limiting the inrush current during startup. The soft−start time depends on the value of the boot voltage and C_{SS}.

Once the SS voltage is within 100 mV of the boot voltage, the boot voltage delay time (TD3 in Figure 5) is started. The end of the boot voltage delay time signals the beginning of the second soft−start time (TD4 in Figure 5). The SS voltage now changes from the boot voltage to the programmed VID DAC voltage (either higher or lower) using the SS amplifier with the limited 15 A output current. The voltage of the FB pin follows the ramping voltage of the SS pin, limiting the inrush current during the transition from the boot voltage to the final DAC voltage. The second soft−start time depends on the boot voltage, the programmed VID DAC voltage, and C_{SS}.

Once TD5 has finished, the SS pin is then used to limit the slew−rate of DVID steps. The current source is changed to 75 A and the DVID slew−rate becomes 5 X the soft−start slew−rate. Typically, the SS slew−rate is 2 mV/ S, so the DVID becomes 10 mV/ S.

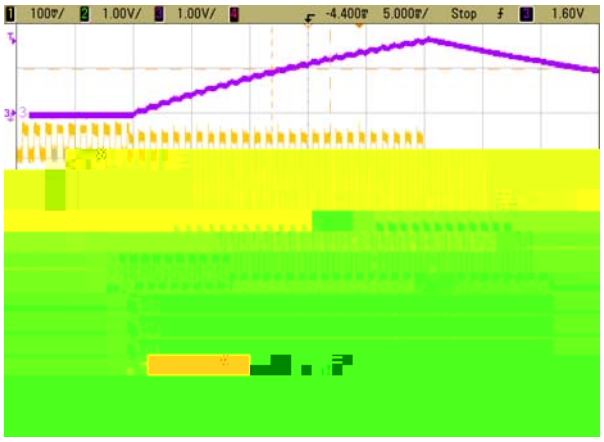
The ADP3290 compares a programmable current limit set point to the voltage from the output of the current sense amplifier. The level of current limit is set with the resistor from the I_{LIM} pin to CSCOMP. During operation, the voltage on I_{LIM} is equal to the voltage on CSREF. The current through the external resistor connected between I_{LIM} and CSCOMP is then compared to the internal current limit current I_{cl}. If the current generated through this register into the I_{LIM} pin(I_{LIM}) exceeds the internal current limit threshold current (I_{cl}), the internal current limit amplifier controls the internal COMP voltage to maintain the average output at the limit.

If the limit is reached and TD5 in Figure 5 has completed, a latchoff delay time starts, and the controller shuts down if the fault is not removed. The current limit delay time shares the DELAY pin timing capacitor with the startup sequence timing. However, during current limit, the DELAY pin current is reduced to 3.75 A. A comparator monitors the DELAY voltage and shuts off the controller when the voltage reaches 1.7 V. Therefore, the current limit latchoff delay time is set by the current of 3.75 A, charging the delay capacitor from 0 V to 1.7 V. This delay is four times longer than the delay time during the startup sequence.

The current limit delay time starts only after the TD5 is complete. If there is a current limit during startup, the ADP3290 goes through TD1 to TD5, and then starts the latchoff time. Because the controller continues to cycle the phases during the latchoff delay time, the controller returns to normal operation and the DELAY capacitor is reset to GND if the short is removed before the 1.7 V threshold is reached.

The latchoff function can be reset by either removing and reapplying the supply voltage to the ADP3290, or by toggling the EN pin low for a short time. To disable the short circuit latchoff function, an external resistor should be placed in parallel with C_{DLY}. This prevents the DELAY capacitor from charging up to the 1.7 V threshold. The addition of this resistor causes a slight increase in the delay times.

During startup, when the output voltage is below 200 mV, a secondary current limit is active. This is necessary because the voltage swing of CSCOMP cannot go below ground. This secondary current limit controls the internal COMP voltage to the PWM comparators to 1.5 V. This limits the voltage drop across the low−side MOSFETs through the current balance circuitry. An inherent per−phase current limit protects individual phases if one or more phases stop functioning because of a faulty component. This limit is based on the maximum normal mode COMP voltage. Typical overcurrent latchoff waveforms are shown in Figure 7.



The I_{MON} pin is used to output an analog voltage representing the total output current being delivered to the load. It outputs an accurate current that is directly proportional to the current set by the I_{LIM} resistor. This current is then run through a parallel RC connected from the I_{MON} pin to the FBRTN pin to generate an accurately scaled and filtered voltage per the VR11.1 specification. The size of the resistor is used to set the I_{MON} scaling.

If the I_{MON}

UVLO or EN is less than their respective thresholds, the ADP3290 is disabled. This holds the PWM outputs at ground, shorts the DELAY capacitor to ground, and the forces PWRGD and $\overline{OD}$ signals low.

In the application circuit, the $\overline{OD}$ pin should be connected to the $\overline{OD}$ input of the external driver for the phase that is always on while the $\overline{ODN}$ pin should be connected to the $\overline{OD}$ input on the external drivers of the phases that are shut off during low−power operation. Grounding $\overline{OD}$ and $\overline{ODN}$ disable the drivers such that both DRVH and DRVL are grounded. This feature is important in preventing the discharge of the output capacitors when the controller is shut off. If the driver outputs are not disabled, a negative voltage can be generated during output due to the high current discharge of the output capacitors through the inductors.

The ADP3290 includes a thermal monitoring circuit to detect when a point on the VR has exceeded a user−defined temperature. The thermal monitoring circuit requires an NTC thermistor to be placed between TTSNS and GND.

A fixed current of 120 A is sourced out of the TTSNS pin

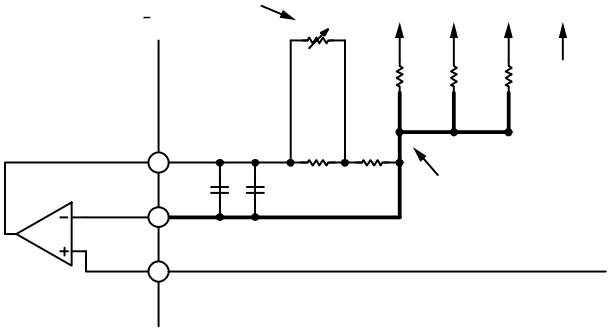
1.09375	0	1	0	1	0	0	1	1
1.08750	0	1	0	1	0	1	0	0
1.08125	0	1	0	1	0	1	0	1
1.07500	0	1	0	1	0	1	1	0
1.06875	0	1	0	1	0	1	1	1
1.06250	0	1	0	1	1	0	0	0
1.05625	0	1	0	1	1	0	0	1
1.05000	0	1	0	1	1	0	1	0
1.04375	0	1	0	1	1	0	1	1
1.03750	0	1	0	1	1	1	0	0
1.03125	0	1	0	1	1	1	0	1
1.02500	0	1	0	1	1	1	1	0
1.01875	0	1	0	1	1	1	1	1
1.01250	0	1	1	0	0	0	0	0
1.00625	0	1	1	0	0	0	0	1
1.00000	0	1	1	0	0	0	1	0
0.99375	0	1	1	0	0	0	1	1
0.98750	0	1	1	0	0	1	0	0
0.98125	0	1	1	0	0	1	0	1
0.97500	0	1	1	0	0	1	1	0
0.96875	0	1	1	0	0	1	1	1
0.96250	0	1	1	0	1	0	0	0
0.95625	0	1	1	0	1	0	0	1
0.95000	0	1	1	0	1	0	1	0
0.94375	0	1	1	0	1	0	1	1
0.93750	0	1	1	0	1	1	0	0
0.93125	0	1	1	0	1	1	0	1
0.92500	0	1	1	0	1	1	1	0
0.91875	0	1	1	0	1	1	1	1
0.91250	0	1	1	1	0	0	0	0
0.90625	0	1	1	1	0	0	0	1
0.90000	0	1	1	1	0	0	1	0
0.89375	0	1	1	1	0	0	1	1
0.88750	0	1	1	1	0	1	0	0
0.88125	0	1	1	1	0	1	0	1
0.87500	0	1	1	1	0	1	1	0
0.86875	0	1	1	1	0	1	1	1
0.86250	0	1	1	1	1	0	0	0
0.85625	0	1	1	1	1	0	0	1
0.85000	0	1	1	1	1	0	1	0
0.84375	0	1	1	1	1	0	1	1
0.83750	0	1	1	1	1	1	0	0
0.83125	0	1	1	1	1	1	0	1
0.82500	0	1	1	1	1	1	1	0
0.81875	0	1	1	1	1	1	1	1
0.81250	1	0	0	0	0	0	0	0
0.80625	1	0	0	0	0	0	0	1
0.80000	1	0	0	0	0	0	1	0
0.79375	1	0	0	0	0	0	1	1
0.78750	1	0	0	0	0	1	0	0

The design parameters for a typical Intel VRD 11.1 compliant CPU application are as follows:

-

The smallest possible inductor should be used to minimize the number of output capacitors. For this example, choosing a 220 nH inductor is a good starting point and gives a calculated ripple current of 12.5 A. The inductor should not saturate at the peak current of 38.7 A and should be able to handle the sum of the power dissipation caused by the average current of 32.5 A in the winding and core loss.

Another important factor in the inductor design is the dc resistance (DCR), which is used for measuring the phase currents. A large DCR can cause excessive power losses, though too small a value can lead to increased measurement error. A good rule is to have the DCR (R_L) be about 1 to 1.5



Here, I_{LIM} is the current limit current, which is the maximum signal level that the CSA responds to.

It is best to select the resistor values to minimize their values to reduce the noise and parasitic susceptibility of the feedback path.

By combining Equation 14 with Equation 15 and selecting minimum values for the resistors, the following equations result:

$$R_{LL2} = \frac{I_{LIM} \times R_O}{50\ \ A} \qquad \text{(eq. 16)}$$

$$R_{LL1} = \left(\frac{R_{CSA}}{R_O} - 1 \right) \times R_{LL2} \qquad \text{(eq. 17)}$$

Another useful feature for some VR applications is the ability to select different load lines. Figure 11 shows an optional MOSFET switch that allows this feature. Here, design for $R_{CSA} = R_{O(MAX)}$ (selected with Q_{LL} on) and then use Equation 14 to set $R_O = R_{O(MIN)}$ (selected with Q_{LL}

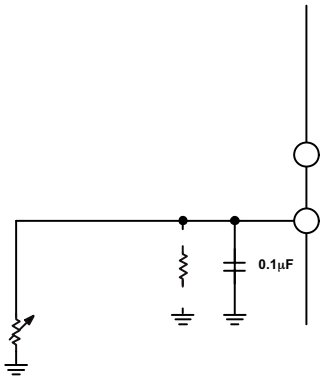
To select the current limit setpoint, first find the resistor value for R_{LIM}. The current limit threshold for the ADP3290 is set with a constant current source (I_{ILIM} = 4/3*I_{REF}) flowing out of the I_{LIM} pin, which sets up a voltage (V_{LIM}) across R_{LIM}. Thus, increasing R_{LIM} now increases the current limit. R_{LIM} can be found using:

$$R_{LIM} = \frac{V_{LIM}}{I_{ILIM}} = \frac{I_{LIM} \times R_{CS} \times DCR}{\frac{4}{3} \times V_{REF} \times R_{PH}} \times R_{REF} \qquad \text{(eq. 33)}$$

Here, I_{LIM} is the peak average current limit for the supply output. The peak average current is the dc current limit plus the output ripple current. In this example, choose I_{LIM_DC} =150 A (130% * TDC) and having a ripple current of 10 A gives an I

$$T_C = \frac{V_{RT} \times \left(L - \frac{A_D \times R_{DS}}{2 \times f_{SW}} \right)}{V_{VID} \times} \quad \text{(eq. 41)}$$

The thermistor is used on the TTSENSE input of the ADP3290 for monitoring the temperature of the VR. A constant current of 123 A is sourced out of this pin and runs through a thermistor network such as the one shown in Figure 14.



A voltage is generated from this current through the thermistor and sensed inside the IC. When the voltage reaches 1.105V, the VRFAN output gets set. When the voltage reaches 0.81 V, the VRHOT gets set. This corresponds to $R_{TTSENSE}$ values of 8.98 k for VRFAN and 6.58 k for VRHOT.

These values correspond to a thermistor temperature of ~100°C and ~110°C when using the same type of 100 k NTC thermistor used in the current sense amplifier.

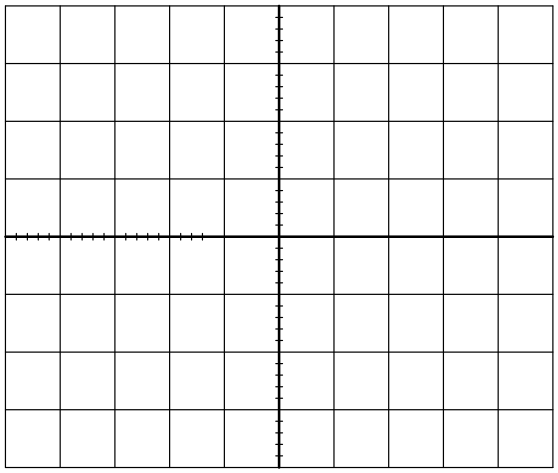
An additional fixed resistor in parallel with the thermistor allows tuning of the trip point temperatures to match the hottest temperature in the VR, when the thermistor itself is directly sensing a proportionately lower temperature. Setting this resistor value is best accomplished with a variable resistor during thermal validation and then fixing this value for the final design.

Additionally, a 0.1 F capacitor should be used for filtering noise.

3. Measure the output voltage at no load (V_{NL}). Verify that it is within tolerance.
4. Measure the output voltage at full load cold (V_{FLCOLD}). Let the board sit for ~10 minutes at full load, and then measure the output (V_{FLHOT}).

19. If both overshoots are larger than desired, try making the adjustments using the following suggestions:
    - Make the ramp resistor larger by 25% (R_{RAMP})
    - For V_{TRAN1}, increase C_B or increase the switching frequency
    - For V_{TRAN2}, increase R_A and decrease C_A by 25%

    If these adjustments do not change the response, the design is limited by the output decoupling. Check the output response every time a change is made, and check the switching nodes to ensure that the response is still stable.
20. For load release (see Figure 18), if $V_{TRANREL}$ is larger than the allowed overshoot, there is not enough output capacitance. Either more capacitance is needed, or the inductor values need to be made smaller. When changing inductors, start the design again using a spreadsheet and this tuning procedure.



to the air. Make a mirror image of any pad being used to heatsink the MOSFETs on the opposite side of the PCB to achieve the best thermal dissipation in the air around the board. To further improve thermal performance, use the largest possible pad area.

The output power path should also be routed to encompass a short distance. The output power path is formed by the current path through the inductor, the output capacitors, and the load.

For best EMI containment, a solid power ground plane should be used as one of the inner layers extending fully under all the power components.

The output voltage is sensed and regulated between the FB pin and the FBRTN pin, which connect to the signal ground at the load. To avoid differential mode noise pickup in the sensed signal, the loop area should be small. Thus, the FB trace and FBRTN trace should be routed adjacent to each other on top of the power ground plane back to the controller.

The feedback traces from the switch nodes should be connected as close as possible to the inductor. The CSREF signal should be connected to the output voltage at the nearest inductor to the controller.

LFCSP40 6x6, 0.5P
CASE 932AC
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