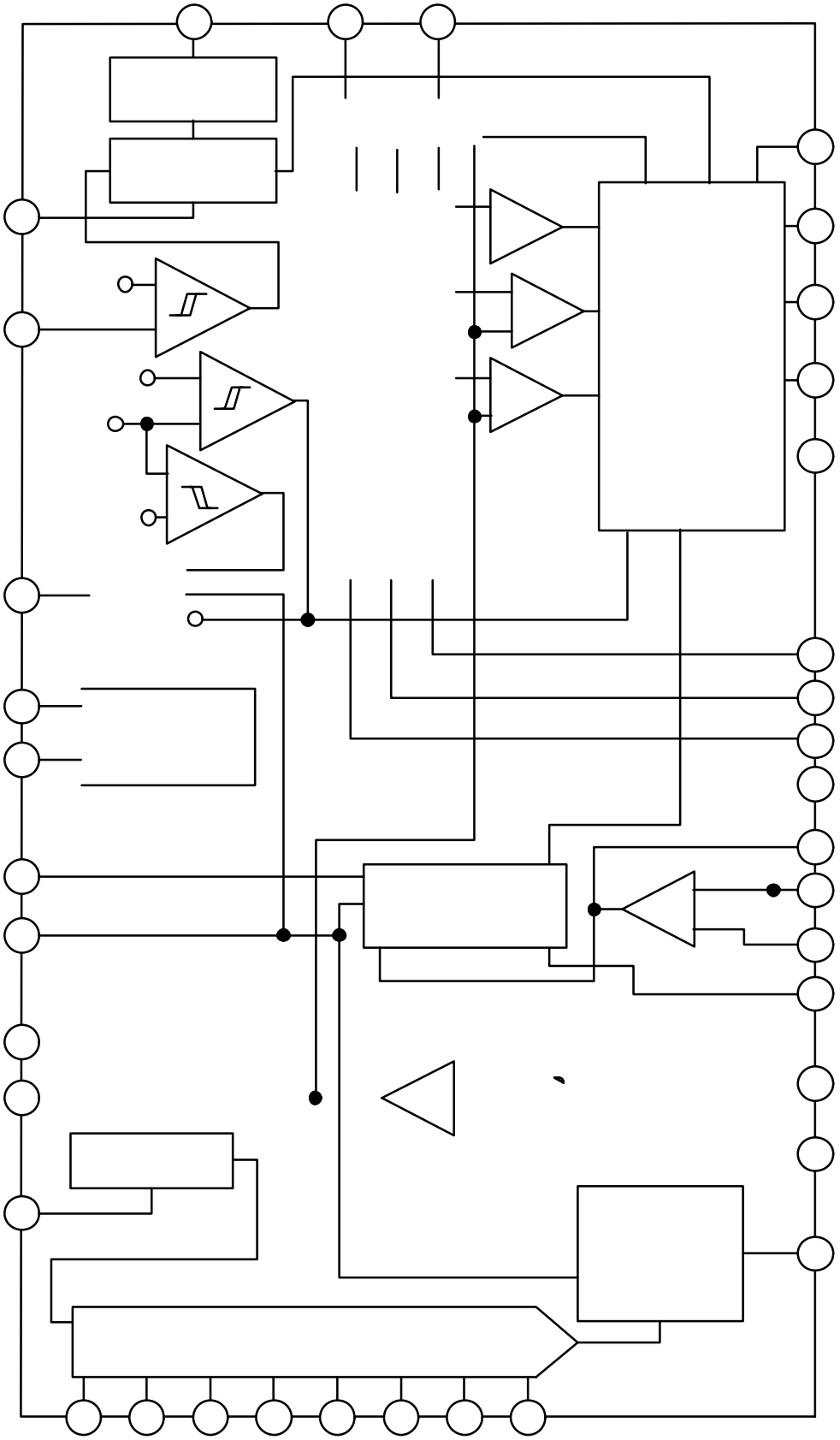

Figure 1. Simplified Block Diagram

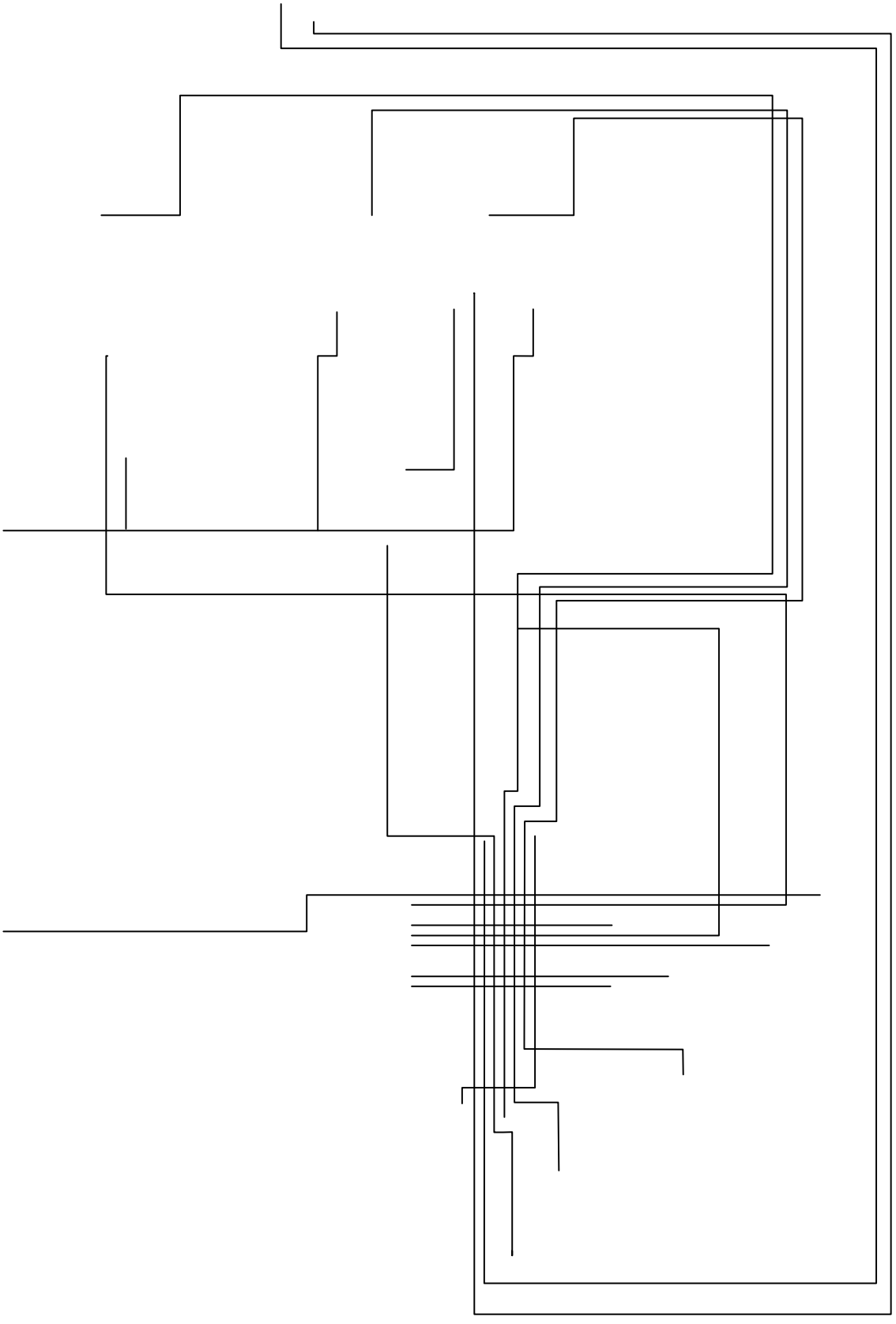

Figure 2. Application Schematic − 3−Phase Operation

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +6	V
FBRTN	V_{FBRTN}	−0.3 to +0.3	V
PWM3 to PWM3, Rampadj		−0.3 to V_{CC} +0.3	V
SW1 to SW3		−5 to +25	V
SW1 to SW3 <200 ns		−10 to +25	V
All other Inputs and Outputs		−0.3 to V_{CC} +0.3	V
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Ambient Temperature Range	T_A	0 to 85	°C
Operating Junction Temperature	T_J	125	°C
Thermal Impedance	θ_{JA}	100	°C/W
Lead Temperature Soldering (10 sec) Infrared (15 sec)		 300 260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

PIN ASSIGNMENT

Pin No.	Mnemonic	Description
1	EN	Power Supply Enable Input. Pulling this pin to GND disables the PWM outputs and pulls the PWRGD output low.
2	PWRGD	Power−Good Output. Open−drain output that signals when the output voltage is outside of the proper operating range.
3	FBRTN	Feedback Return. VID DAC and error amplifier input for remote sensing of the output voltage.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, FBRTN = GND, T_A = 0°C to 85°

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, FBRTN = GND, T_A = 0°C to 85°C unless otherwise noted) (Note 1)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Current Sense Amplifier						
Offset Voltage	$V_{OS(CSA)}$	CSSUM - CSREF, CSREF = 0.8V ~1.6V, Temperature Range: 0 °C to 60 °C	−0.5		+0.5	mV
Input Bias Current	$I_{BIAS(CSSUM)}$	Temperature Range: 0 °C to 60 °C	−7.5		+7.5	nA
Gain Bandwidth Product	$GBW_{(CSA)}$	CSSUM = CSCOMP		10		MHz
Slew Rate		C_{CSCOMP} = 10 pF		10		V/μs
Input Common−Mode Range		CSSUM and CSREF	0		3.5	V
Output Voltage Range			0.05		3.5	V
Output Current	I_{CSCOMP}			500		μA

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, FBRTN = GND, T_A = 0°C to 85°C unless otherwise noted) (Note 1)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Thermal Throttling Control						
VRHOT Output Low Voltage	$V_{OL(VRHOT)}$	$I_{VRHOT(SINK)}$ = −4 mA, TTSNS = 5 V		150	300	mV
Power−Good Comparator						
Undervoltage Threshold	$V_{PWRGD(UV)}$	Relative to nominal DAC output	−400	−350	−300	mV
Overvoltage Threshold	$V_{PWRGD(OV)}$	Relative to nominal DAC output	100	150	200	mV
Output Low Voltage	$V_{OL(PWRGD)}$	$I_{PWRGD(SINK)}$ = −4 mA		150	300	mV
Power−Good Delay Time During Soft−Start		C_{DELAY} = 10 nF		2.0		ms
VID Code Changing			100	250		μs
VID Code Static				200		ns
Crowbar Trip Point	$V_{CB(CSREF)}$	Relative to nominal DAC output	100	150	200	mV
Crowbar Reset Threshold		Relative to FBRTN	305	360	415	mV
Crowbar Delay Time VID Code Changing	$t_{CROWBAR}$	Overvoltage to PWM going low	100	250		μs
VID Code Static				400		ns
PWM OUTPUTS Output Low Voltage	$V_{OL(PWM)}$	$I_{PWM(SINK)}$ = −400 μA		160	500	mV
Output High Voltage	$V_{OH(PWM)}$	$I_{PWM(SOURCE)}$ = 400 μA	4.0	5.0		V
Supply						
V_{CC}	V_{CC}	V_{SYSTEM} = 12 V, R_{SHUNT} = 340 Ω	4.65	5.0	5.55	V
DC Supply Current	I_{VCC}	V_{SYSTEM} = 13.2 V, R_{SHUNT} = 340 Ω			25	mA
Shunt Turn−On Current				6.5		mA
Shunt Turn−On Threshold Voltage	V_{SYSTEM}	V_{SYSTEM} rising		6		V
Shunt Turn−Off Voltage		V_{SYSTEM} falling		4.1		V

1. All limits at temperature extremes are guaranteed via correction using standard quality control (SQC).
2. Guaranteed by characterization, not tested in production.
3. Guaranteed by design, not tested in production.

TYPICAL CHARACTERISTICS

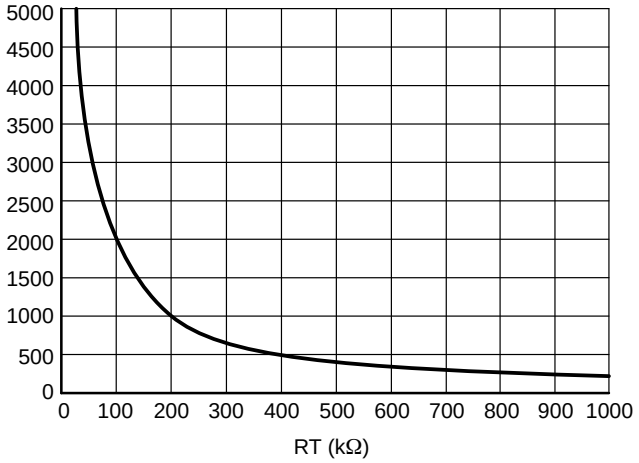

Figure 3. Oscillator Frequency vs. RT

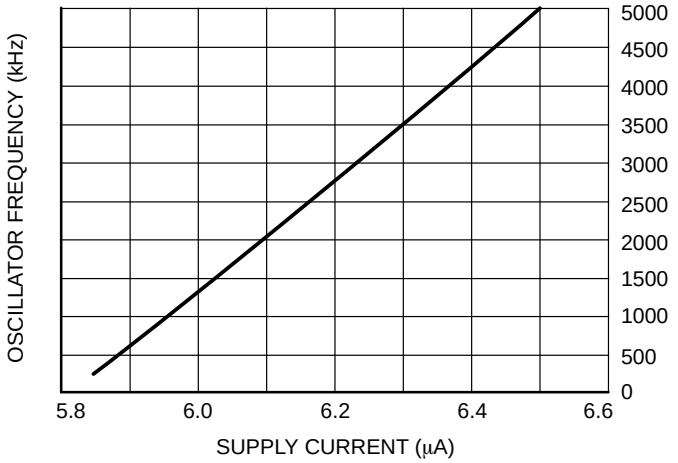

Figure 4. Oscillator Frequency vs. Supply Current

Theory of Operation

The ADP3293 combines a multi−mode, fixed frequency PWM control with multiphase logic outputs for use in 2− or 3−phase synchronous buck CPU core supply power converters. The internal VID DAC is designed to interface with Intel 8−bit VRD/VRM 11.1 and compatible CPUs. Multiphase operation is important for producing the high currents and low voltages demanded by today's microprocessors. Handling the high currents in a single−phase converter places high thermal demands on the components in the system, such as the inductors and MOSFETs.

The multi−mode control of the ADP3293 ensures a stable, high performance topology for the following:

- Balancing currents and thermals between phases for both static and dynamic operation
- High speed response at the lowest possible switching frequency and output decoupling
- FEPWM and TRDET functions for improved load step and load release transient response
- Minimizing thermal switching losses by using lower frequency operation
- Tight load line regulation and accuracy
- Reduced output ripple due to multiphase cancellation
- PC board layout noise immunity
- Ease of use and design due to independent component selection
- Flexibility in operation for tailoring design to low cost or high performance

Startup Sequence

The ADP3293 follows the VR11.1 startup sequence shown in Figure 5. After both the EN and UVLO conditions are met, the DELAY pin goes through one cycle (TD1). After this cycle, the internal oscillator is enabled. The first four clock cycles are blanked from the PWM outputs and used for phase detection as explained in the Phase Detection Sequence section. Then, the soft−start ramp is enabled (TD2),

Master Clock Frequency

The clock frequency of the ADP3293 is set with an external

Voltage Control Mode

A high gain, bandwidth voltage mode error amplifier is used for the voltage mode control loop. The control input voltage to the positive input is set via the VID logic according to the voltages listed.

This voltage is also offset by the droop voltage for active positioning of the output voltage as a function of current, commonly known as active voltage positioning. The output of the amplifier is the COMP pin, which sets the termination voltage for the internal PWM ramps.

The negative input (FB) is tied to the output sense location with Resistor R_B and is used for sensing and controlling the output voltage at this point. A current source from the FB pin flowing through R_B is used for setting the no load offset voltage from the VID voltage. The no load voltage is negative with respect to the VID DAC. The main loop compensation is incorporated into the feedback network between FB and COMP.

Fast Enhanced Transient Modes

The ADP3293 incorporates enhanced transient response for both load steps and load release. For load steps, it senses the error amp to determine if a load step has occurred and sequences the proper number of phases on to ramp up the output current.

For load release, it also senses the error amp and uses the load release information to trigger the TRDET pin, which is then used to adjust the feedback for optimal positioning especially during high frequency load steps.

Additional information is used during load transients to ensure proper sequencing and balancing of phases during high frequency load steps as well as minimizing stress on the components such as the input filter and MOSFETs.

Delay Timer

The delay times for the startup timing sequence are set with a capacitor from the DELAY pin to ground. In UVLO, or when EN is logic low, the DELAY pin is held at ground. After the UVLO and EN signals are asserted, the first delay time (TD1 in Figure 5) is initiated. A 15 μA current flows out of the DELAY pin to charge C_{DLY}. A comparator monitors the DELAY voltage with a threshold of 1.7 V. The delay time is therefore set by the 15 μA charging a capacitor from 0 V to 1.7 V. This DELAY pin is used for multiple delay timings (TD1, TD3, and TD5) during the startup sequence. Also, DELAY is used for timing the current limit latchoff, as explained in the Current Limit section.

Soft−Start

The soft−start times for the output voltage are set with a capacitor from the SS pin to ground. After TD1 and the phase detection cycle have been completed, the SS time (TD2 in Figure 5) starts. The SS pin is disconnected from GND, and the capacitor is charged up to the 1.1 V boot voltage by the SS amplifier, which has a limited output current of 15 μA. The voltage at the FB pin follows the ramping voltage on the SS pin, limiting the inrush current during startup. The soft−start time depends on the value of the boot voltage and C_{SS}.

Once the SS voltage is within 100 mV of the boot voltage, the boot voltage delay time (TD3 in Figure 5) is started. The end of the boot voltage delay time signals the beginning of the second soft−start time (TD4 in Figure 5). The SS voltage now changes from the boot voltage to the programmed VID DAC voltage (either higher or lower) using the SS amplifier with the limited 15 μA output current. The voltage of the FB pin follows the ramping voltage of the SS pin, limiting the inrush current during the transition from the boot voltage to the final DAC voltage. The second soft−start time depends on the boot voltage, the programmed VID DAC voltage, and C_{SS}.

Once TD5 has finished, the SS pin is then used to limit the slew−rate of DVID steps. The current source is changed to 75 μA and the DVID slew−rate becomes 5 X the soft−start slew−rate. Typically, the SS slew−rate is 2 mV/μS, so the DVID becomes 10 mV/μS.

If EN is taken low or if V_{CC} drops below UVLO, DELAY and SS are reset to ground to be ready for another soft−start cycle.

Current Limit, Short−Circuit, and Latchoff Protection

The ADP3293 compares a programmable current limit set point to the voltage from the output of the current sense amplifier. The level of current limit is set with the resistor from the ILIM pin to CSCOMP. During operation, the voltage on ILIM is equal to the voltage on CSREF. The current through the external resistor connected between ILIM and CSCOMP is then compared to the internal current limit current I_{cl}. If the current generated through this register into the ILM pin(Ilim) exceeds the internal current limit threshold current (I_{cl}), the internal current limit amplifier controls the internal COMP voltage to maintain the average output at the limit.

If the limit is reached and TD5 in Figure 5 has completed, a latchoff delay time starts, and the controller shuts down if the fault is not removed. The current limit delay time shares the DELAY pin timing capacitor with the startup sequence timing. However, during current limit, the DELAY pin current is reduced to 3.75 μA. A comparator monitors the DELAY voltage and shuts off the controller when the voltage reaches 1.7 V. Therefore, the current limit latchoff delay time is set by the current of 3.75 μA, charging the delay capacitor from 0 V to 1.7 V. This delay is four times longer than the delay time during the startup sequence.

The current limit delay time starts only after the TD5 is complete. If there is a current limit during startup, the ADP3293 goes through TD1 to TD5, and then starts the latchoff time. Because the controller continues to cycle the phases during the latchoff delay time, the controller returns to normal operation and the DELAY capacitor is reset to GND if the short is removed before the 1.7 V threshold is reached.

The latchoff function can be reset by either removing and reapplying the supply voltage to the ADP3293, or by toggling the EN pin low for a short time. To disable the short circuit latchoff function, an external resistor should be placed in parallel with C_{DLY}. This prevents the DELAY capacitor from charging up to the 1.7 V threshold. The addition of this resistor causes a slight increase in the delay times.

During

Power State Indicator

The $\overline{\text{PSI}}$ pin is used as an input to determine the operating power state of the load. If this pin is pulled low, the controller knows the load is in a low power state and it takes the $\overline{\text{ODN}}$ signal low, which can be used to disable phases for increased efficiency.

The sequencing into and out of low−power operation is maintained to minimize output voltage deviations as well as providing full−power load transients immediately following exit from a low−power state.

One additional feature of the ADP3293 is the internal current limit threshold is changed when $\overline{\text{PSI}}$ is pulled low. The current limit threshold is reduced by 1/N such that the same per phase average current limit is maintained to protect the components in the system.

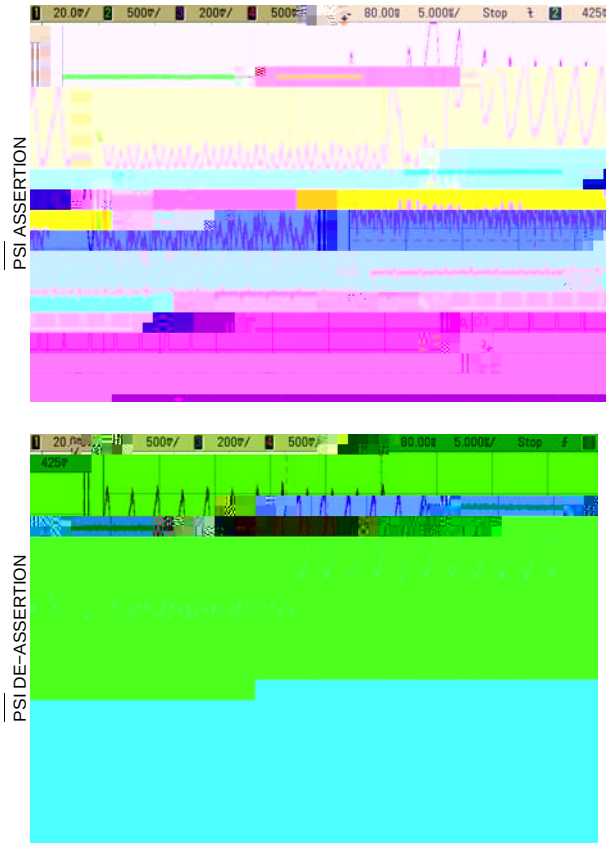

Figure 7. $\overline{\text{PSI}}$ Mode Transition Waveform (Io = 25A)
1-Vo, 2-$\overline{\text{PSI}}$, 3-COMP, 4-TRDET, D0~D2-PWM1~3

Output Crowbar

To protect the load and output components of the supply, the PWM outputs are driven low, which turns on the low−side MOSFETs when the output voltage exceeds the upper crowbar threshold. This crowbar action stops once the output voltage falls below the release threshold of approximately 375 mV.

Turning on the low−side MOSFETs pulls down the output as the reverse current builds up in the inductors. If the output overvoltage is due to a short in the high−side MOSFET, this action current limits the input supply or blows its fuse, protecting the microprocessor from being destroyed.

Output Enable and UVLO

For the ADP3293 to begin switching, the input supply current to the controller must be higher than the UVLO threshold and the EN pin must be higher than its 0.8 V threshold. This initiates a system startup sequence. If either UVLO or EN is less than their respective thresholds, the ADP3293 is disabled. This holds the PWM outputs at ground, shorts the DELAY capacitor to ground, and the forces PWRGD and $\overline{\text{OD}}$ signals low.

In the application circuit, the $\overline{\text{OD}}$ pin should be connected to the $\overline{\text{OD}}$ input of the external driver for the phase that is always on while the $\overline{\text{ODN}}$ pin should be connected to the $\overline{\text{OD}}$ input on the external drivers of the phases that are shut off during low−power operation. Grounding $\overline{\text{OD}}$ and $\overline{\text{ODN}}$ disable the drivers such that both DRVH and DRVL are grounded. This feature is important in preventing the discharge of the output capacitors when the controller is shut off. If the driver outputs are not disabled, a negative voltage can be generated during output due to the high current discharge of the output capacitors through the inductors.

Thermal Monitoring

The ADP3293 includes a thermal monitoring circuit to detect when a point on the VR has exceeded a user−defined temperature. The thermal monitoring circuit requires an NTC thermistor to be placed between TTSNS and GND.

A fixed current of 120 μA is sourced out of the TTSNS pin and into the thermistor. The current source is internally limited to 5.0 V. An internal circuit compares the TTSNS voltage to a 0.81 V threshold, and outputs an w[OTJfSTJ/TT5 1 Tf4..2(

Ouasr prgh cu a gnalOuentin Crs exocrrent ThBecausehe TTSNS pilt

VR11.1 VID Codes

OUTPUT(V)	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
1.02500	0	1	0	1	1	1	1	0
1.01875	0	1	0	1	1	1	1	1
1.01250	0	1	1	0	0	0	0	0
1.00625	0	1	1	0	0	0	0	1
1.00000	0	1	1	0	0	0	1	0
0.99375	0	1	1	0	0	0	1	1
0.98750	0	1	1	0	0	1	0	0
0.98125	0	1	1	0	0	1	0	1
0.97500	0	1	1	0	0	1	1	0
0.96875	0	1	1	0	0	1	1	1
0.96250	0	1	1	0	1	0	0	0
0.95625	0	1	1	0	1	0	0	1
0.95000	0	1	1	0	1	0	1	0
0.94375	0	1	1	0	1	0	1	1
0.93750	0	1	1	0	1	1	0	0
0.93125	0	1	1	0	1	1	0	1
0.92500	0	1	1	0	1	1	1	0
0.91875	0	1	1	0	1	1	1	1
0.91250	0	1	1	1	0	0	0	0
0.90625	0	1	1	1	0	0	0	1
0.90000	0	1	1	1	0	0	1	0
0.89375	0	1	1	1	0	0	1	1
0.88750	0	1	1	1	0	1	0	0
0.88125	0	1	1	1	0	1	0	1
0.87500	0	1	1	1	0	1	1	0
0.86875	0	1	1	1	0	1	1	1
0.86250	0	1	1	1	1	0	0	0
0.85625	0	1	1	1	1	0	0	1
0.85000	0	1	1	1	1	0	1	0
0.84375	0	1	1	1	1	0	1	1
0.83750	0	1	1	1	1	1	0	0
0.83125	0	1	1	1	1	1	0	1
0.82500	0	1	1	1	1	1	1	0
0.81875	0	1	1	1	1	1	1	1
0.81250	1	0	0	0	0	0	0	0
0.80625	1	0	0	0	0	0	0	1
0.80000	1	0	0	0	0	0	1	0
0.79375	1	0	0	0	0	0	1	1
0.78750	1	0	0	0	0	1	0	0
0.78125	1	0	0	0	0	1	0	1
0.77500	1	0	0	0	0	1	1	0
0.76875	1	0	0	0	0	1	1	1
0.76250	1	0	0	0	1	0	0	0
0.75625	1	0	0	0	1	0	0	1
0.75000	1	0	0	0	1	0	1	0
0.74375	1	0	0	0	1	0	1	1
0.73750	1	0	0	0	1	1	0	0

Application Information

The design parameters for a typical Intel VRD 11.1 compliant CPU application are as follows:

- Input voltage (V_{IN}) = 12 V
- VID setting voltage (V_{VID}) = 1.400 V
- Duty cycle (D) = 0.117
- Nominal output voltage at no load (V_{ONL}) = 1.381 V
- Nominal output voltage at 85 A load (V_{OFL}) = 1.296 V
- Static output voltage drop based on a 1.0 mΩ load line (R_O) from no load to full load (V_D) = $V_{ONL} - V_{OFL}$ = 1.381 V − 1.296 V = 85 mV
- Maximum output current (I_O) = 100 A
- Maximum output current step (ΔI_O) = 85 A

The smallest possible inductor should be used to minimize the number of output capacitors. For this example, choosing a 220 nH inductor is a good starting point and gives a calculated ripple current of 12.5 A. The inductor should not saturate at the peak current of 39.6 A and should be able to handle the sum of the power dissipation caused by the average current of 34.6 A in the winding and core loss.

Another important factor in the inductor design is the dc resistance (DCR), which is used for measuring the phase currents. A large DCR can cause excessive power losses, though too small a value can lead to increased measurement error. A good rule is to have the DCR (R_L) be about 1 to 1.5 times the droop resistance (R_O). This example uses an inductor with a DCR of 0.57 mΩ.

Designing an Inductor

Once the inductance and DCR are known, the next step is to either design an inductor or to find a standard inductor that comes as close as possible to meeting the overall design goals. It is also important to have the inductance and DCR tolerance specified to control the accuracy of the system. Reasonable tolerances most manufacturers can meet are 15% inductance and 7% DCR at room temperature. The first decision in designing the inductor is choosing the

$$C_{X(MIN)} \geq \left(\frac{220\ nH \times 85\ A}{3 \times \left(1.0\ m\Omega + \frac{50\ mV}{85\ A}\right) \times 1.4\ V} - 396\ \mu F \right) = 2.407mF$$

$$C_{X(MAX)} \leq \frac{220\ nH \times 1.1\ V}{3 \times 5.39^2 \times \left(1.0\ m\Omega\right)^2 \times 1.4\ V} \times$$

$$\left(1 + \left(233.75\ \mu s \times 1.4\ V \times 3 \times 5.39 \times 1.0\ m\Omega \right. \right.$$

impedance and MOSFET input capacitance, Equation 24 provides an approximate value for the switching loss per main MOSFET, where n_{MF} is the total number of main MOSFETs.

$$P_{S(MF)} = 2 \times f_{SW} \times \frac{V_{CC} \times I_O}{n_{MF}} \times R_G \times \frac{n_{MF}}{n} \times C_{ISS} \quad \text{(eq. 24)}$$

where R_G is the total gate resistance (2 Ω for the ADP3120A and about 1 Ω for typical high speed switching MOSFETs, making R_G = 3 Ω), and C_{ISS} is the input capacitance of the main MOSFET. Adding more main MOSFETs (n_{MF}) does not help the switching loss per MOSFET because the additional gate capacitance slows switching. Use lower gate capacitance devices to reduce switching loss.

The conduction loss of the main MOSFET is given by the following, where $R_{DS(MF)}$ is the on resistance of the MOSFET:

$$P_{C(MF)} = D \times \left[\left(\frac{I_O}{n_{MF}} \right)^2 + \frac{1}{12} \times \left(\frac{n \times I_R}{n_{MF}} \right)^2 \right] \times R_{DS(MF)} \quad \text{(eq. 25)}$$

Typically, for main MOSFETs, the highest speed (low C_{ISS}) device is preferred, but these usually have higher on resistance. Select a device that meets the total power dissipation (about 1.5 W for a single D−PAK) when combining the switching and conduction losses.

For this example, an BSC100N03L is selected as the main MOSFET (six total; n_{MF} = 3), with C_{ISS} = 1000 pF (maximum) and $R_{DS(MF)}$ = 11 mΩ (maximum at T_J = 120°C). An IPD09N03L is selected as the synchronous MOSFET (six total; n_{SF} = 6), with C_{ISS} = 1600 pF (maximum) and $R_{DS(SF)}$ = 10.5 mΩ (maximum at T_J = 120°C). The synchronous MOSFET C_{ISS} is less than 3000 pF, satisfying this requirement.

Solving for the power dissipation per MOSFET at I_O = 100 A and I_R = 7.5 A yields 1.9 W for each synchronous MOSFET and 2.0 W for each main MOSFET.

Finally, consider the power dissipation in the driver for each phase. This is best expressed as Q_G for the MOSFETs and is given by Equation 26, where Q_{GMF} is the total gate charge for each main MOSFET and Q_{GSF} is the total gate charge for each synchronous MOSFET.

$$P_{DRV} = \left[\frac{f_{SW}}{2 \times n} \times \left(n_{MF} \times Q_{GMF} + n_{SF} \times Q_{GSF} \right) + I_{CC} \right] \times V_{CC} \quad \text{(eq. 26)}$$

Also shown is the standby dissipation factor ($I_{CC} \times V_{CC}$) of the driver. For the ADP3120A, the maximum dissipation should be less than 400 mW. In this example, with I_{CC} = 7 mA, Q_{GMF} = 13 nC, and Q_{GSF} = 15 nC, there is 200 mW in each driver, which is below the 400 mW dissipation limit. See the ADP3120A data sheet1 Tf.2268 0 05.0583 91.

In this example, the overall ramp signal is 1.05 V. If the ramp size is smaller than 0.5 V, increase the ramp size to be at least 0.5 V by decreasing the ramp resistor for noise immunity.

Current Limit Setpoint

To select the current limit setpoint, first find the resistor value for R_{LIM}. The current limit threshold for the ADP3293 is set with a constant current source (I_{ILIM} = 4/3*I_{REF}) flowing out of the ILIM pin, which sets up a voltage (V_{LIM}) across R_{LIM}. Thus, increasing R_{LIM} now increases the current limit. R_{LIM} can be found using:

$$R_{LIM} = \frac{V_{LIM}}{I_{ILIM}} = \frac{I_{LIM} \times R_{CS} \times DCR}{\frac{4}{3} \times V_{REF} \times R_{PH}}$$

First, compute the time constants for all the poles and zeros in the system using Equation 36 to Equation 40.

$$R_E = n \times R_O + A_D \times R_{DS} + \frac{R_L \times V_{RT}}{V_{VID}} + \frac{2 \times L \times (1 - n \times D) \times V_{RT}}{n \times C_X \times R_O \times V_{VID}}$$

$$R_E = 3 \times 1\ m\Omega + 5 \times 5.25\ m\Omega + \frac{0.57\ m\Omega \times 1.05\ V}{1.4\ V} + \frac{2 \times 220\ nH \times (1 - 0.35) \times 1.05\ V}{3 \times 3.36\ mF \times 1\ m\Omega \times 1.4\ V} = 50.96\ m\Omega$$

(eq. 36)

$$T_A = C_X \times \left(R_O - R^1\right) + \frac{L_X}{R_O} \times \frac{R_O - R^1}{R_X} = 3.36\ mF \times \left(1\ m\Omega - 0.5\ m\Omega\right) + \frac{330\ pH}{1\ m\Omega} \times \frac{1\ m\Omega - 0.5\ m\Omega}{0.83\ m\Omega} = 1.88\ \mu s$$

(eq. 37)

$$T_B = \left(R_X + R^1 - R_O\right) \times C_X = \left(0.83\ m\Omega + 0.5\ m\Omega - 1\ m\Omega\right) \times 3.36\ mf = 1109\ ns$$

(eq. 38)

$$T_C = \frac{V_{RT} \times \left(L - \frac{A_D \times R_{DS}}{2 \times f_{SW}}\right)}{V_{VID} \times R_E} = \frac{1.05\ V \times \left(220\ nH - \frac{5 \times 5.25\ m\Omega}{2 \times 450\ kHz}\right)}{1.4\ V \times 50.96\ m\Omega} = 2.81\ \mu s$$

(eq. 39)

$$T_D = \frac{C_X \times C_Z \times R_O^2}{C_X \times \left(R_O - R^1\right) + C_Z \times R_O} = \frac{3.36\ mF \times 396\ \mu F \times \left(1\ m\Omega\right)^2}{3.36\ mF \times \left(1\ m\Omega - 0.5\ m\Omega\right.}$$

(eq. 40)

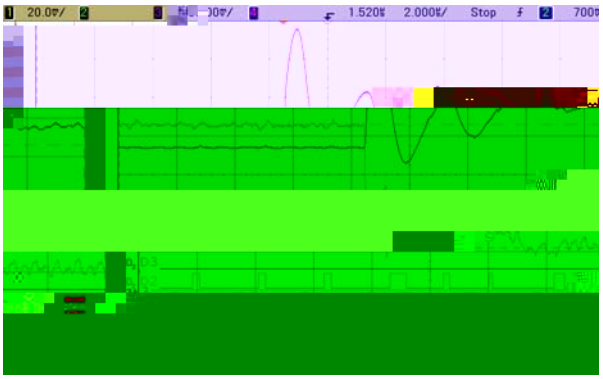

Figure 10. Typical Transient Response for Design Example Load Step

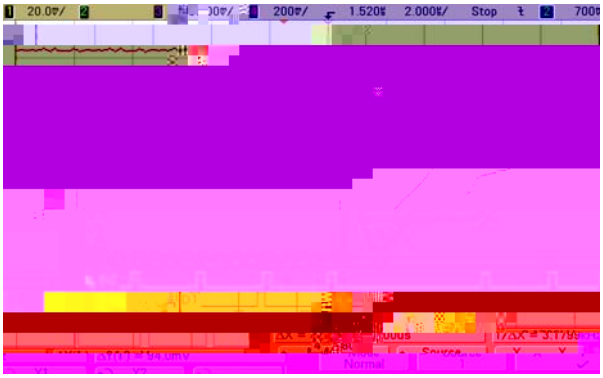

Figure 11. Typical Transient Response for Design Example Load Release
1-Vo, 3-COMP, 4-TRDET, D0~D2-PWM1~3

C_{IN} Selection and Input Current di/dt Reduction

In continuous inductor current mode, the source current of the high-side MOSFET is approximately a square wave with a duty ratio equal to n × V_{OUT}/V_{IN} and an amplitude of one-nth the maximum output current. To prevent large voltage transients, a low ESR input capacitor, sized for the maximum rms current, must be used. The maximum rms capacitor current is given by:

$$I_{CRMS} = D \times I_O \times \sqrt{\frac{1}{N \times D} - 1}$$

$$I_{CRMS} = 0.117 \times 100\ A \times \sqrt{\frac{1}{3 \times 0.117} - 1} = 15.9\ A$$

(eq. 45)

The capacitor manufacturer's ripple−current ratings are often based on only 2000 hours of life. As a result, it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors can be placed in parallel to meet size or height requirements in the design. In this example, the input capacitor bank is formed by three 680 μF, 16 V aluminum electrolytic capacitors and twelve 4.7 μF ceramic capacitors.

To reduce the input current di/dt to a level below the recommended maximum of 0.1 A/μs, an additional small inductor (L > 370 nH at 18 A) should be

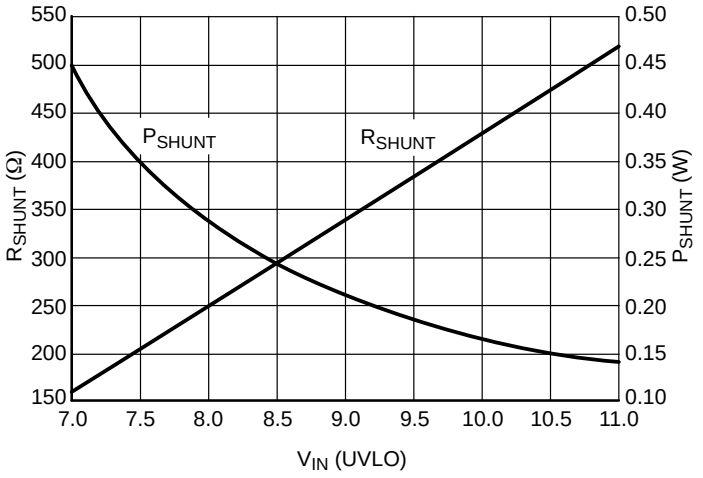

Figure 13. Typical Shunt Resistor Value and Power Dissipation for Different UVLO Voltage

The maximum power dissipated is calculated using Equation 46.

$$P_{MAX} = \frac{\left(V_{IN(MAX)} - V_{CC(MIN)}\right)^2}{R_{SHUNT}} \quad \text{(eq. 46)}$$

where:

$V_{IN(MAX)}$ is the maximum voltage from the 12 V input supply (if the 12 V input supply is 12 V ± 5%, $V_{IN(MAX)}$ = 12.6 V; if the 12 V input supply is 12 V ± 10%, $V_{IN(MAX)}$ = 13.2 V). $V_{CC(MIN)}$ is the minimum V_{CC} voltage of the ADP3293. This is specified as 4.75 V. R_{SHUNT} is the shunt resistor value.

The CECC standard specification for power rating in surface mount resistors is: 0603 = 0.1 W, 0805 = 0.125 W, 1206 = 0.25 W.

Tuning the ADP3293

1. Build a circuit based on the compensation values computed from the design spreadsheet.

AC Load Line Setting

11. Remove the dc load from the circuit and hook up the dynamic load.
12. Hook up the scope to the output voltage and set it

Because the ADP3293 turns off all of the phases (switches inductors to ground), no ripple voltage is present during load release. Therefore, the user does not have to add headroom for ripple. This allows load release $V_{TRANREL}$ to be larger than V_{TRAN1} by the amount of ripple, and still meet specifications.

If V_{TRAN1} and $V_{TRANREL}$ are less than the desired final droop, this implies that capacitors can be removed. When removing capacitors, also check the output ripple voltage to make sure it is still within specifications.

Layout and Component Placement

The following guidelines are recommended for optimal performance of a switching regulator in a PC system.

General Requirements

For good results, a PCB with at least four layers is recommended. This provides the needed versatility for control circuitry interconnections with optimal placement, power planes for ground, input and output power, and wide interconnection traces in the remainder of the power delivery current paths. Keep in mind that each square unit of 1 ounce copper trace has a resistance of ~0.53 mΩ at room temperature.

Whenever high currents must be routed between PCB layers, use vias liberally to create several parallel current paths, so the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.

If critical signal lines (including the output voltage sense lines of the ADP3293) must cross through power circuitry, it is best to interpose a signal ground plane between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of making signal ground a bit noisier.

An analog ground plane should be used around and under the ADP3293 as a reference for the components associated with the controller. This plane should be tied to the nearest output decoupling capacitor ground and should not be tied to any other power circuitry to prevent power currents from flowing into it.

The components around the ADP3293 should be located close to the controller with short traces. The most important traces to keep short and away from other traces are the FB pin and CSSUM pin. The output capacitors should be connected as close as possible to the load (or connector), for example, a microprocessor core, that receives the power. If the load is distributed, the capacitors should also be distributed and generally be in proportion to where the load tends to be more dynamic.

Avoid crossing any signal lines over the switching power path loop described in the Power Circuitry Recommendations sections.

Power Circuitry Recommendations

The switching power path should be routed on the PCB to encompass the shortest possible length to minimize radiated switching noise energy (EMI) and conduction losses in the board. Failure to take proper precautions often results in EMI problems for the entire PC system and noise−related operational problems in the power converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors and the power MOSFETs, including all interconnecting PCB traces and planes. Using short and wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which can cause high energy ringing; and it accommodates the high current demand with minimal voltage loss.

When a power dissipating component, for example, a power MOSFET, is soldered to a PCB, it is recommended to liberally use the vias, both directly on the mounting pad and immediately surrounding it. Two important reasons for this are improved current rating through the vias and improved thermal performance from vias extended to the opposite side of the PCB, where a plane can more readily transfer the heat to the air. Make a mirror image of any pad being used to heatsink the MOSFETs on the opposite side of the PCB to achieve the best thermal dissipation in the air around the board. To further improve thermal performance, use the largest possible pad area.

The output power path should also be routed to encompass a short distance. The output power path is formed by the current path through the inductor, the output capacitors, and the load.

For best EMI containment, a solid power ground plane should be used as one of the inner layers extending fully under all the power components.

Signal Circuitry Recommendations

The output voltage is sensed and regulated between the FB pin and the FBRTN pin, which connect to the signal ground at the load. To avoid differential mode noise pickup in the sensed signal, the loop area should be small. Thus, the FB trace and FBRTN trace should be routed adjacent to each other on top of the power ground plane back to the controller.

The feedback traces from the switch nodes should be connected as close as possible to the inductor. The CSREF signal should be connected to the output voltage at the nearest inductor to the controller.

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