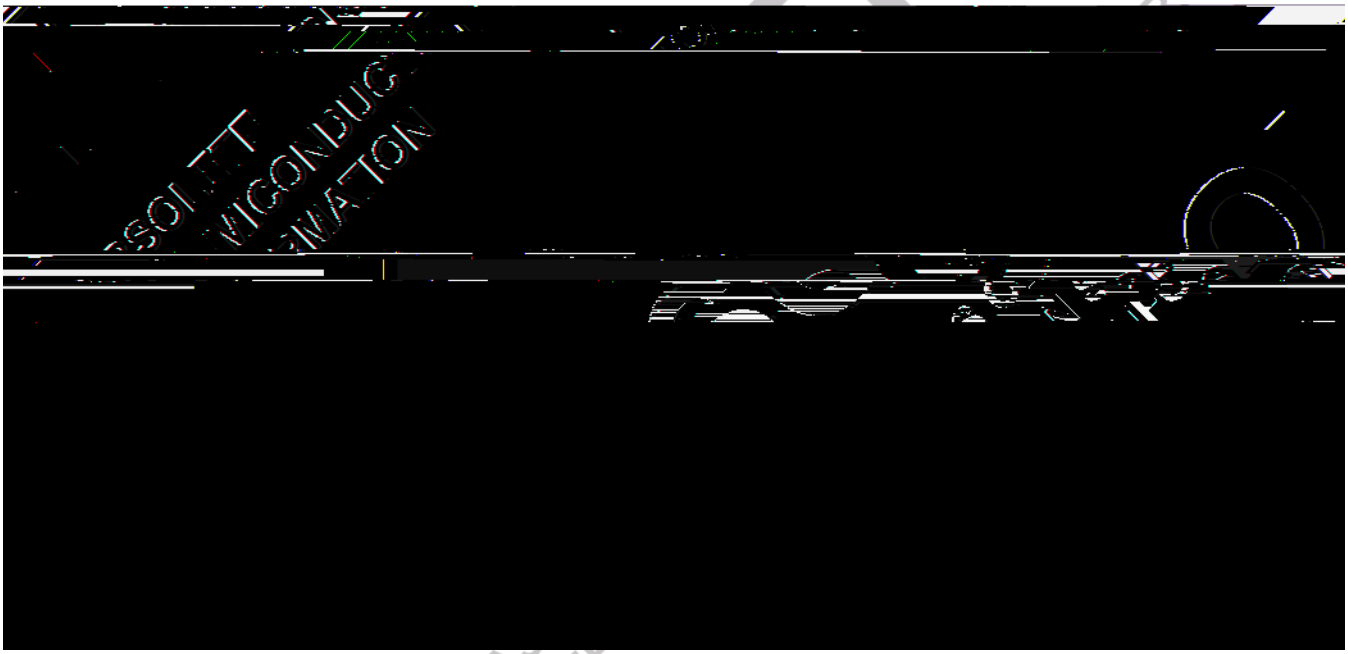
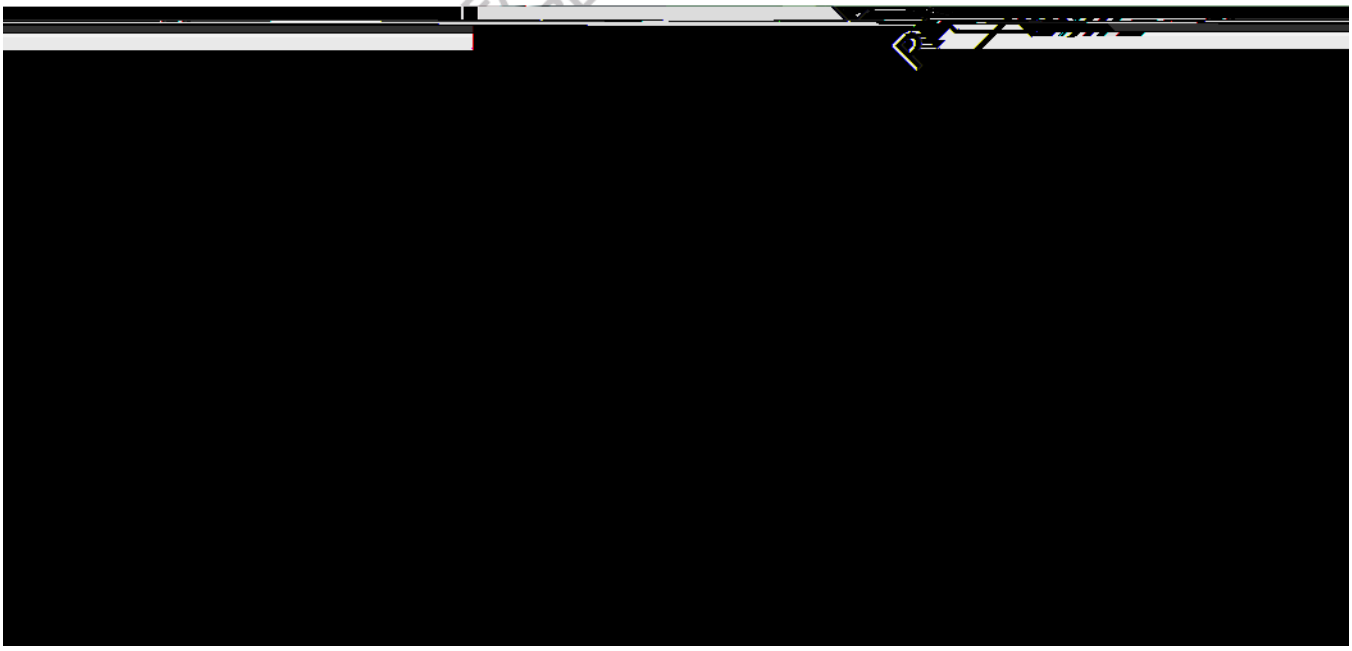
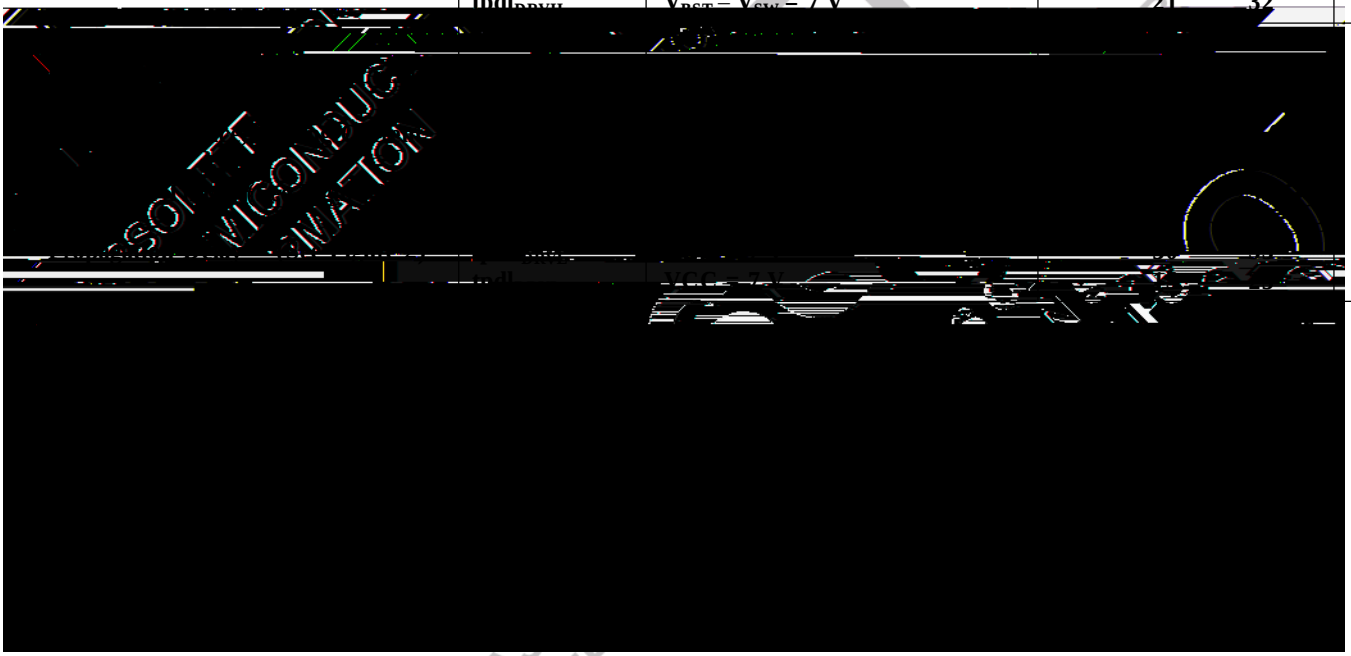
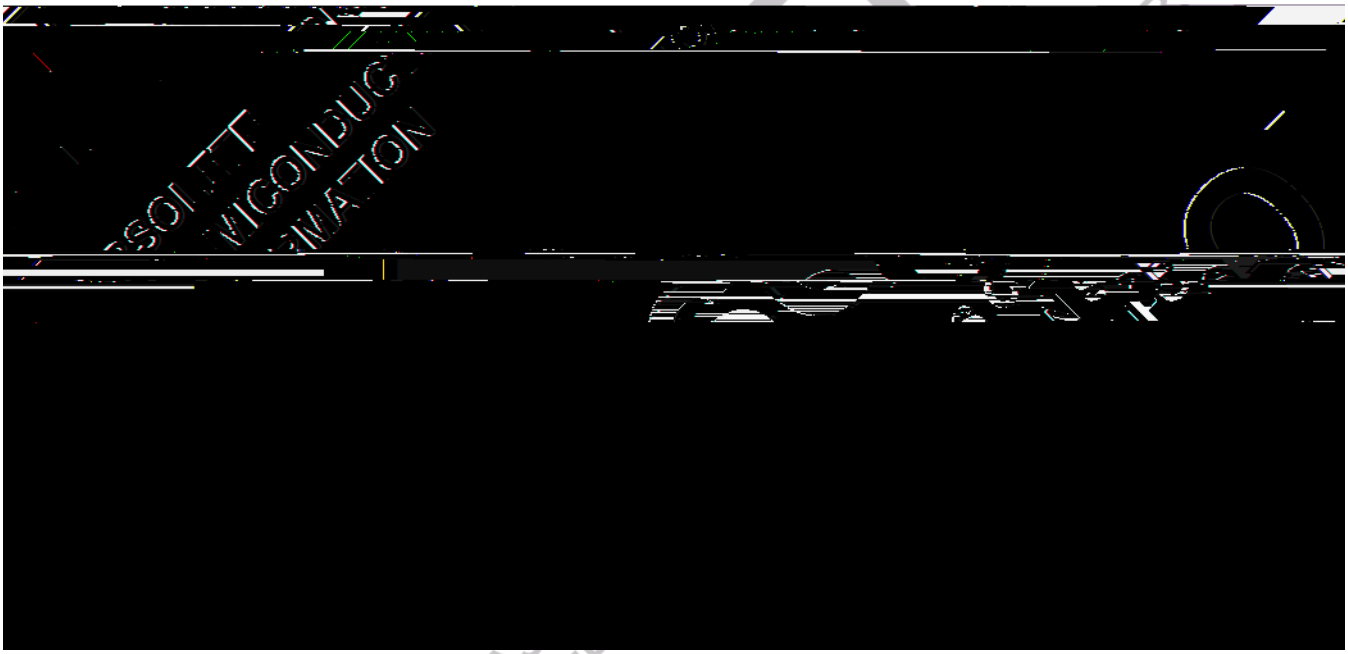


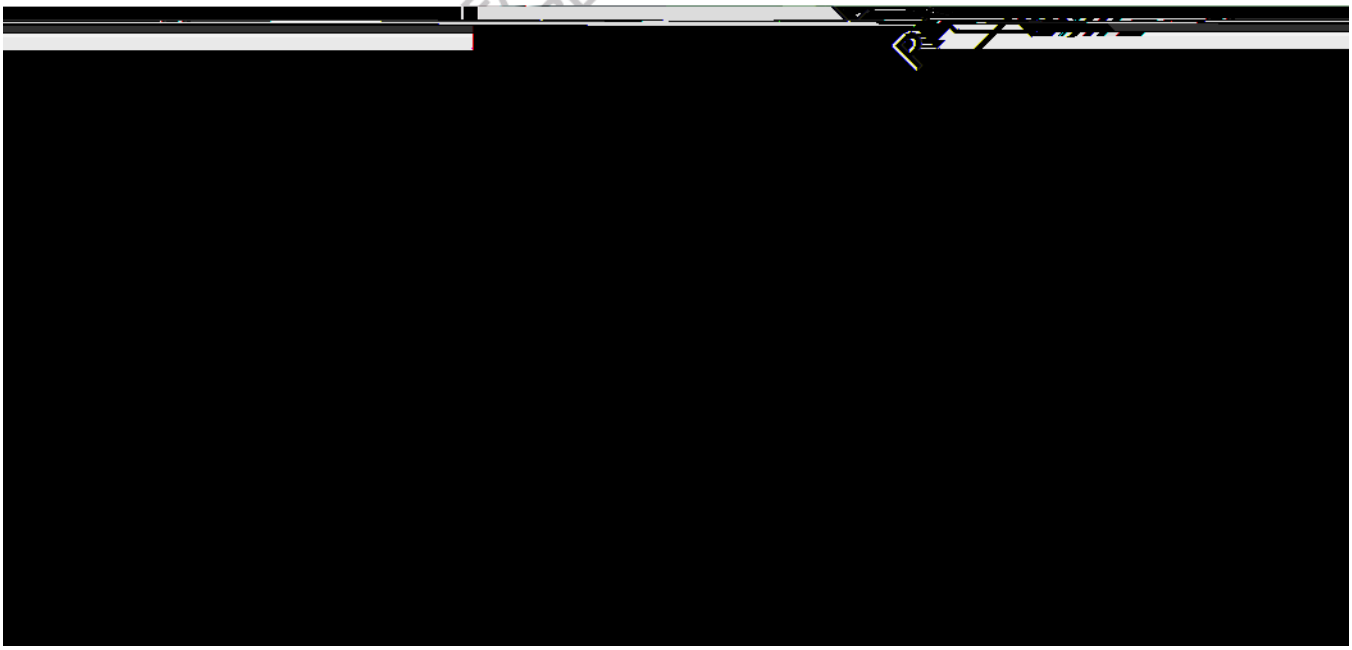


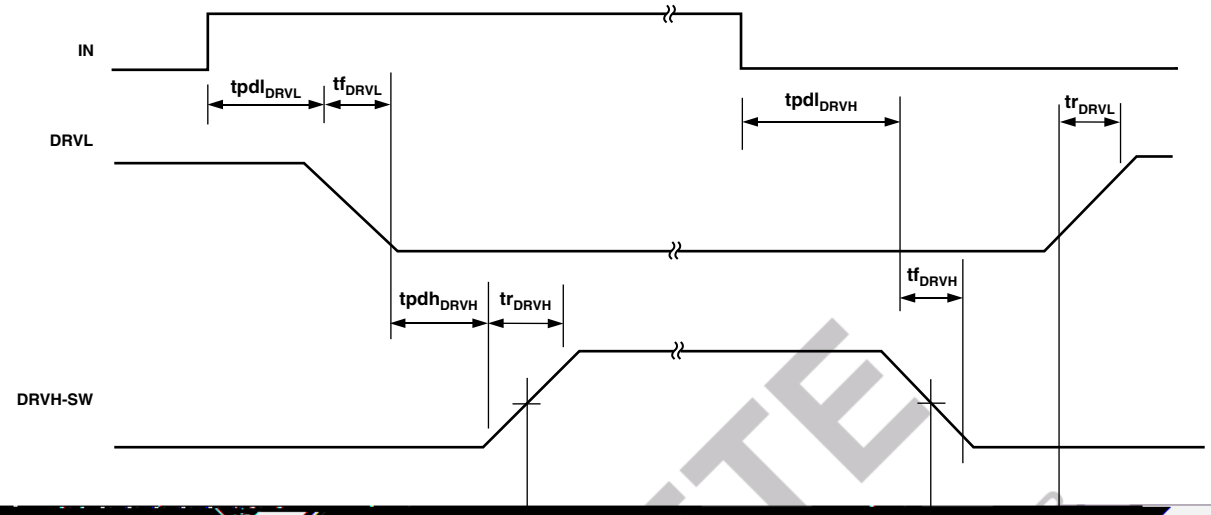
ADP3414—SPECIFICATIONS[1] (T_A = 0°C to 70°C, VCC = 7 V, BST = 4 V to 26 V, unless otherwise noted.)

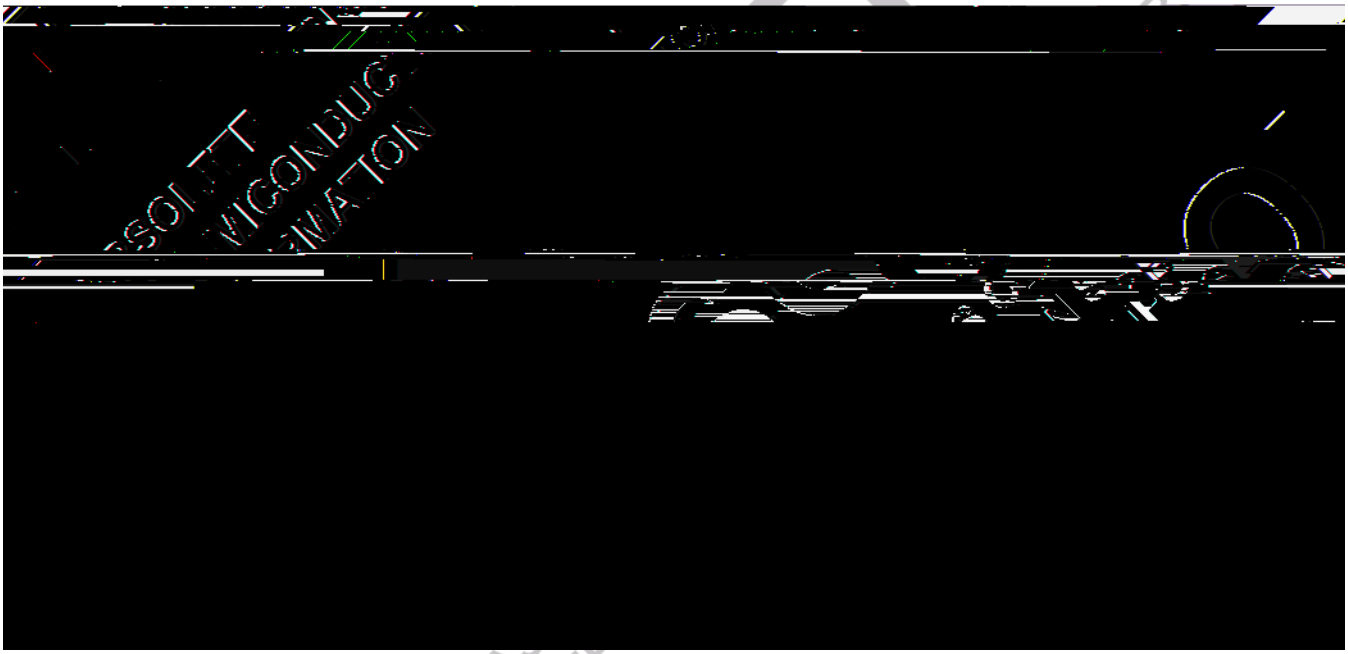
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SUPPLY						
Supply Voltage Range	VCC		4.15		7.5	V
Quiescent Current	ICC_Q			1	2	mA
PWM INPUT						
Input Voltage High[2]			2.3			V
Input Voltage Low[2]					0.8	V
HIGH SIDE DRIVER						
Output Resistance, Sourcing Current		$V_{BST} - V_{SW}$ = 5 V		3.0	5.0	Ω
		$V_{BST} - V_{SW}$ = 7 V		2.0	3.5	Ω
Output Resistance, Sinking Current		$V_{BST} - V_{SW}$ = 5 V		1.25	2.5	Ω
		$V_{BST} - V_{SW}$ = 7 V		1.0	2.5	Ω
Transition Times[3] (See Figure 2)	tr_{DRVH}	$V_{BST} - V_{SW}$ = 7 V, C_{LOAD} = 3 nF		36	47	ns
	tf_{DRVH}	$V_{BST} - V_{SW}$ = 7 V, C_{LOAD} = 3 nF		20	30	ns
Propagation Delay[3, 4] (See Figure 2)	$tpdh_{DRVH}$	$V_{BST} - V_{SW}$ = 7 V		65	86	ns
	$tpdl_{DRVH}$	$V_{BST} - V_{SW}$ = 7 V		21	32	ns
LOW SIDE DRIVER						
Output Resistance, Sourcing Current		VCC = 7 V		3.0	5.0	Ω
		VCC = 5 V		2.0	3.5	Ω
Output Resistance, Sinking Current		VCC = 7 V		1.25	2.5	Ω
		VCC = 5 V		1.0	2.5	Ω
Transition Times[3] (See Figure 2)	tr_{DRVL}	VCC = 7 V, C_{LOAD} = 3 nF		36	47	ns
	tf_{DRVL}	VCC = 7 V, C_{LOAD} = 3 nF		20	30	ns
Propagation Delay[3, 4] (See Figure 2)	$tpdh_{DRVL}$	VCC = 7 V		65	86	ns
	$tpdl_{DRVL}$	VCC = 7 V		21	32	ns

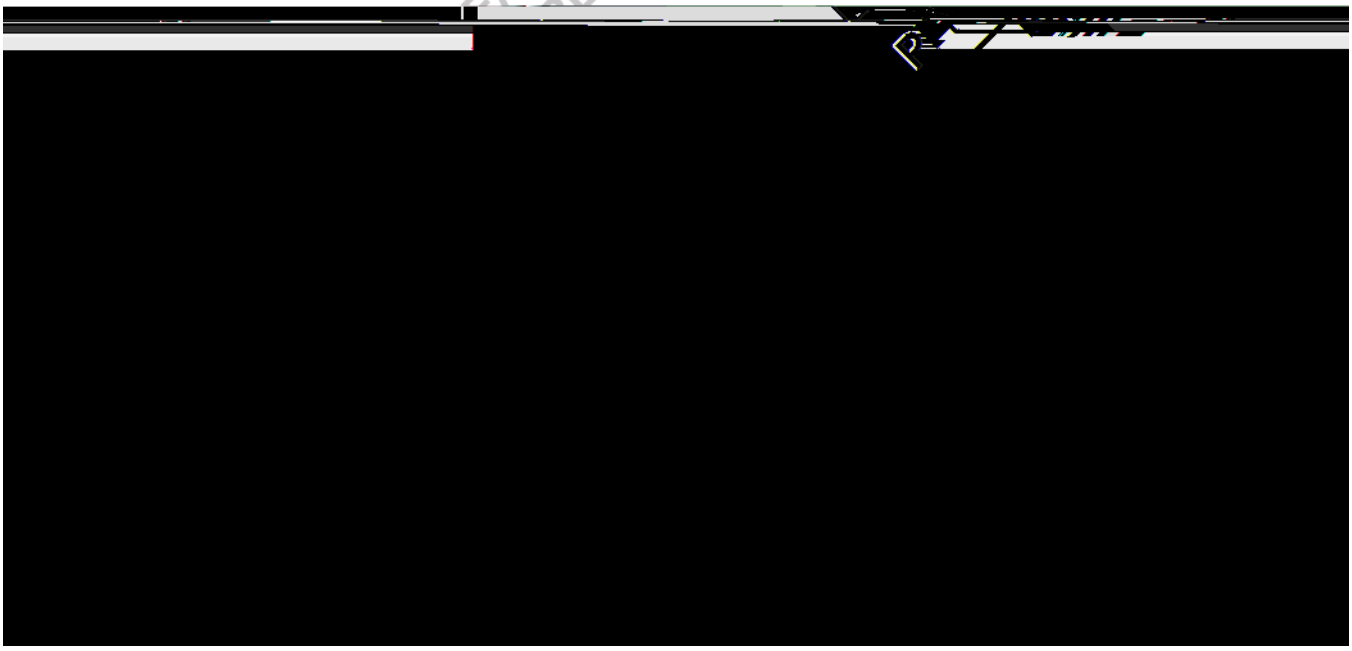







IN
DRVL
DRVH-SW
tpdl$_{DRVL}$
tf$_{DRVL}$
tpdl$_{DRVH}$
tr$_{DRVL}$
tf$_{DRVH}$
tpdh$_{DRVH}$
tr$_{DRVH}$





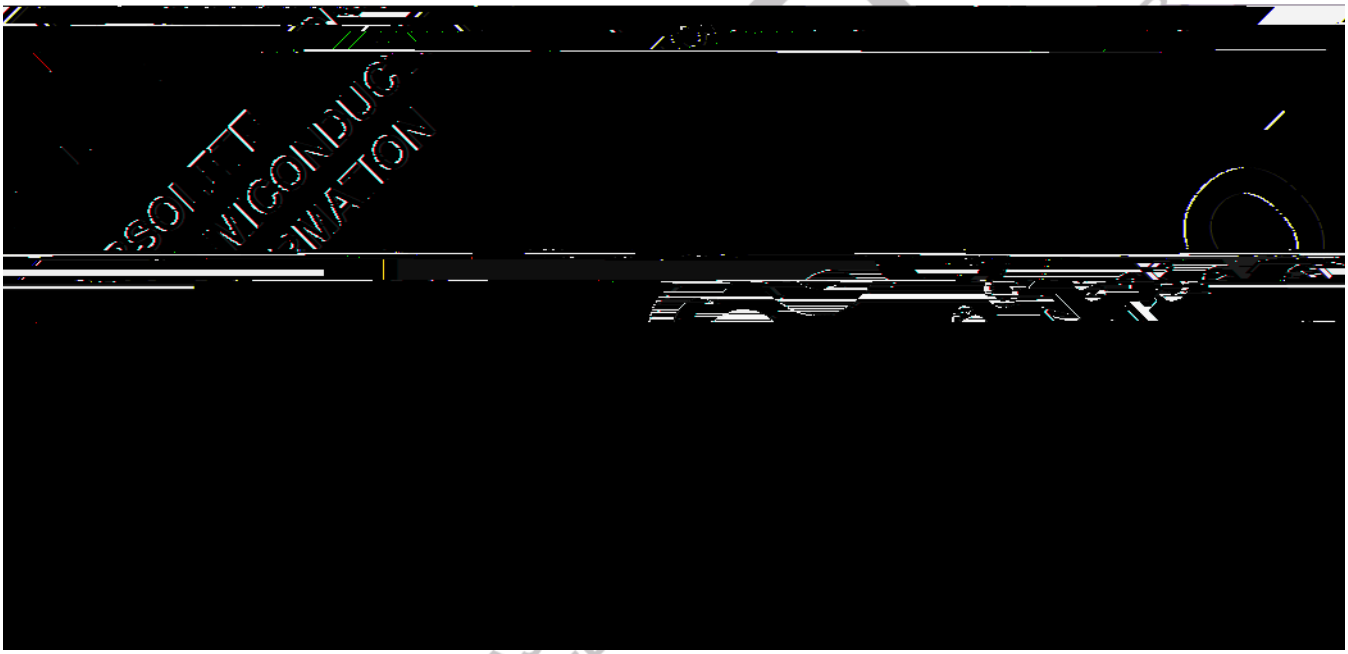
THEORY OF OPERATION

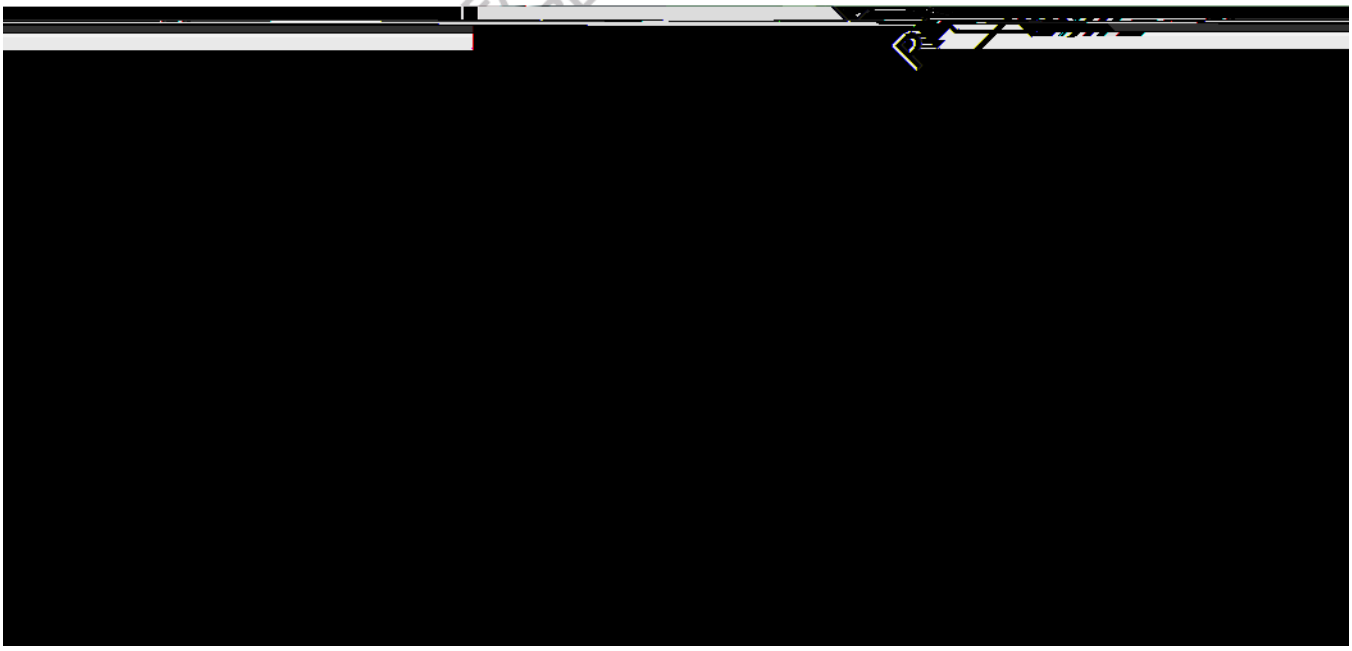
The ADP3414 is a dual MOSFET driver optimized for driving two N-channel MOSFETs in a synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high side and the low side FETs. Each driver is capable of driving a 3 nF load.

A more detailed description of the ADP3414 and its features follows. Refer to the Functional Block Diagram.

Low Side Driver

The low side driver is designed to drive low $R_{DS(ON)}$ N-channel MOSFETs. The maximum output resistance for the driver is 3.5 Ω for sourcing and 2.5 Ω for sinking gate current. The low output resistance allows the driver to have 20 ns rise and fall times into a 3 nF load. The bias to the low side driver is internally connected to the VCC supply and PGND.

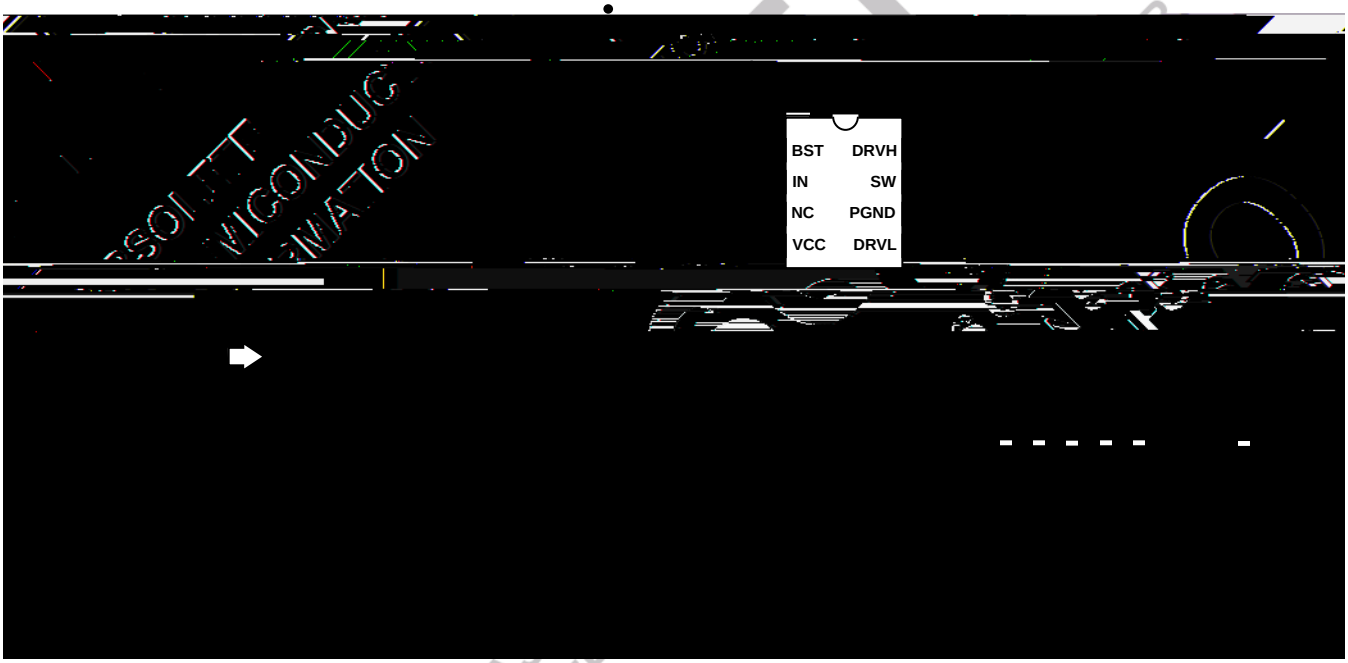


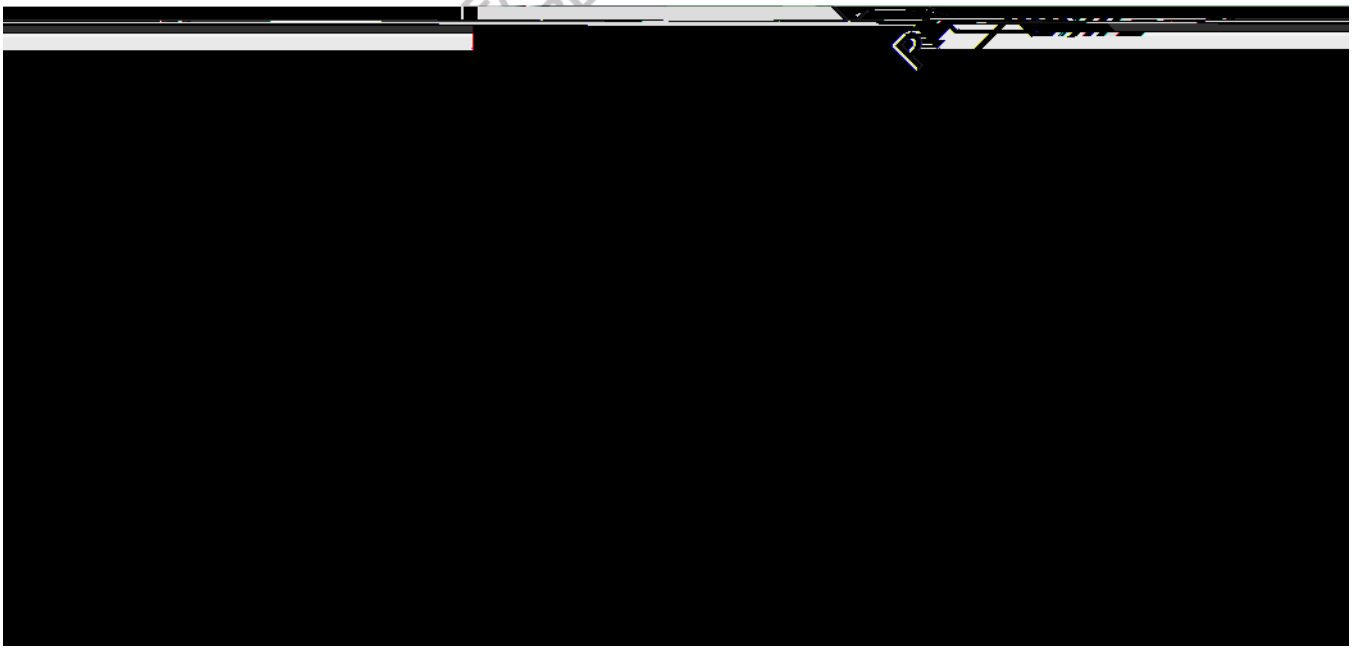


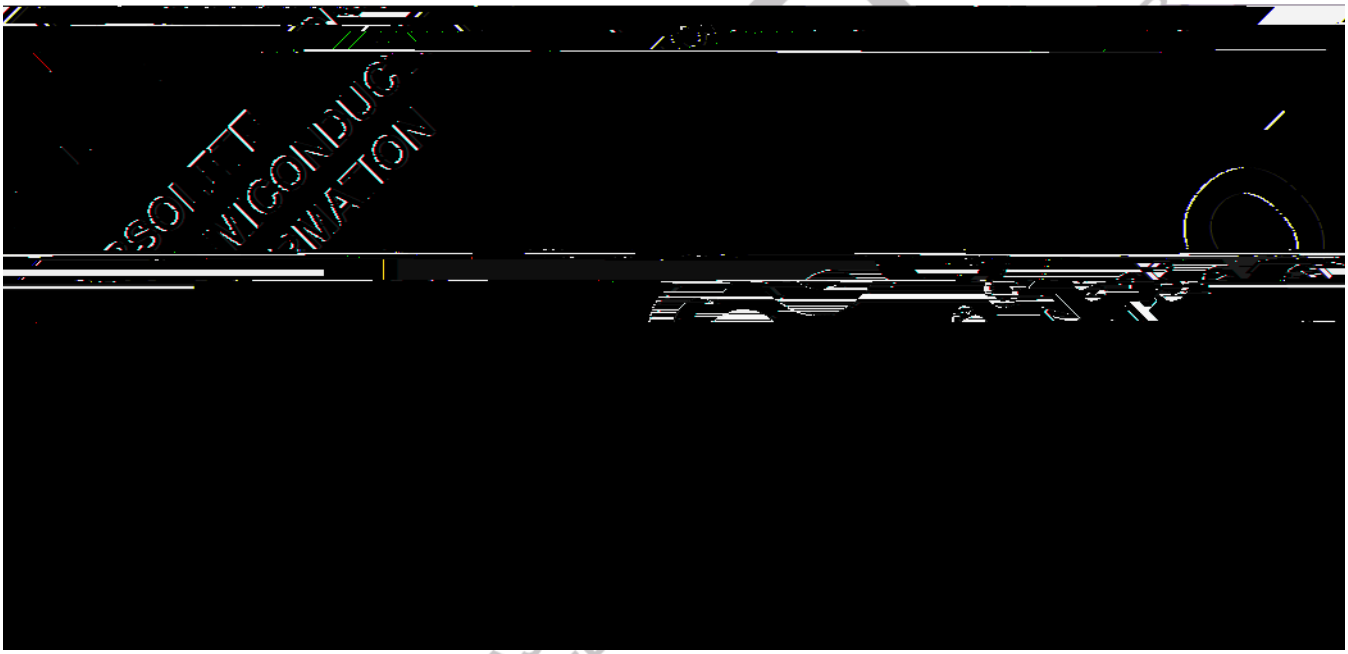
Printed Circuit Board Layout Considerations

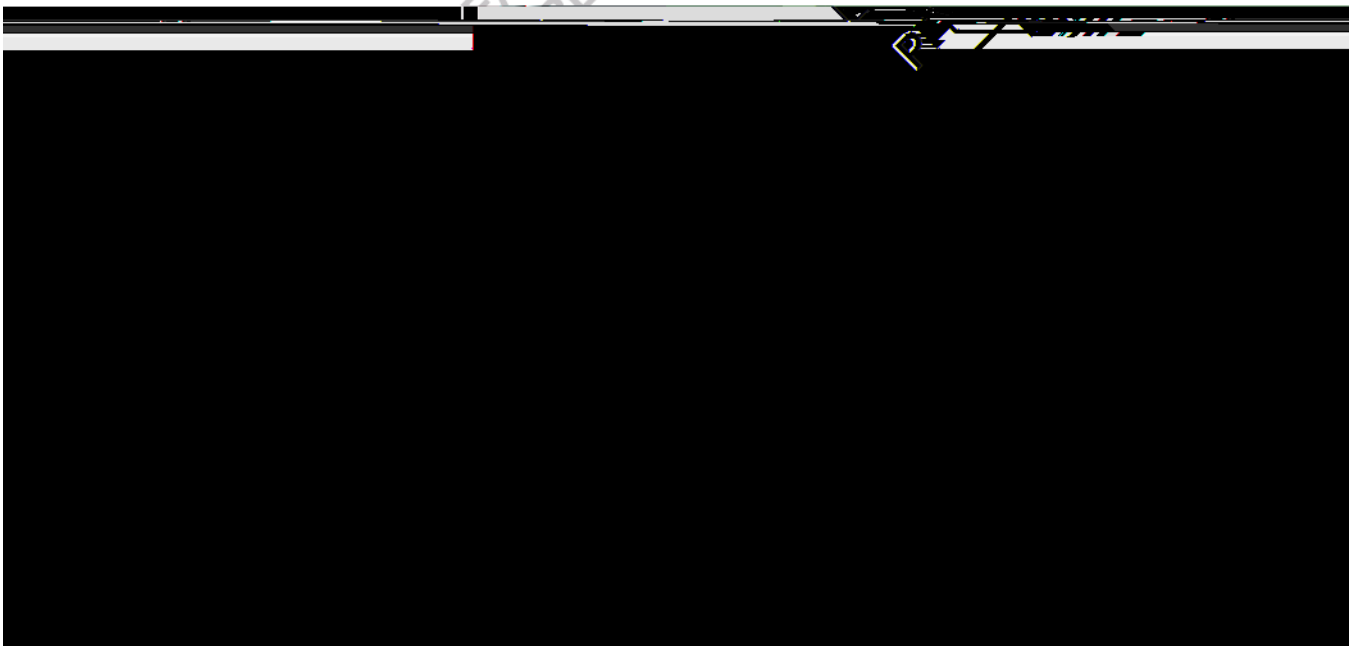
se t e fo ow n enera u de nes w en des n n pr nted c rcu t boards

- race out t e current pat s and use s ort_w de traces to a e t ese connect ons-
- Connect t e PGND p n of t e ADP as c ose as poss b e to t e source of t e ower MO FE -
- e CC bypass capac tor s ou d be ocated as c ose as poss b e to CC and PGND P ns-









8-Lead Standard Small Outline Package [SOIC]
Narrow Body
(R-8)