ADP3419

D a B a, ed, H V a e MOSFET D e O , D ab e

The ADP3419 is a dual MOSFET driver optimized for driving two N-channel switching MOSFETs in nonisolated synchronous buck power converters used to power CPUs in portable computers. The driver impedances have been chosen to provide optimum performance in multiphase regulators at up to 25 A per phase. The high-side driver can be bootstrapped relative to the switch node of the buck converter and is designed to accommodate the high voltage slew rate associated with floating high-side gate drivers.

The ADP3419 includes an anticross-conduction protection circuit, undervoltage lockout to hold the switches off until the driver has sufficient voltage for proper operation, a crowbar input that turns on the low-side MOSFET independently of the input signal state, and a low-side MOSFET disable pin to provide higher efficiency at light loads. The $\overline{SD}$

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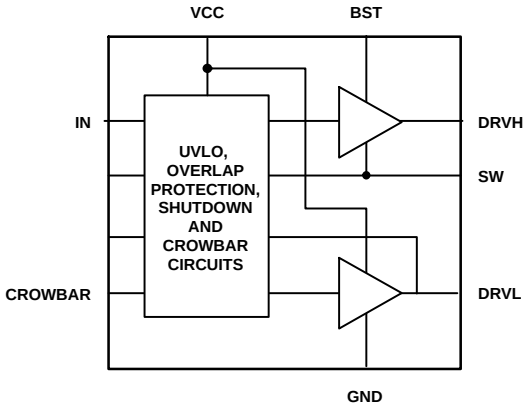

Figure 1. Simplified Block Diagram

Figure 2. General Application Circuit

PIN ASSIGNMENT

Pin No.	Mnemonic	Description
1	IN	Logic Level PWM Input. This pin has primary control of the drive outputs. In normal operation, pulling this pin low turns on the low-side driver; pulling it high turns on the high-side driver.
2	$\overline{SD}$	Shutdown Input. When low, this pin disables normal operation, forcing DRVH and DRVL low.
3	$\overline{DRVLSD}$	Synchronous Rectifier Shutdown Input. When low, DRVL is forced low; when high, DRVL is enabled

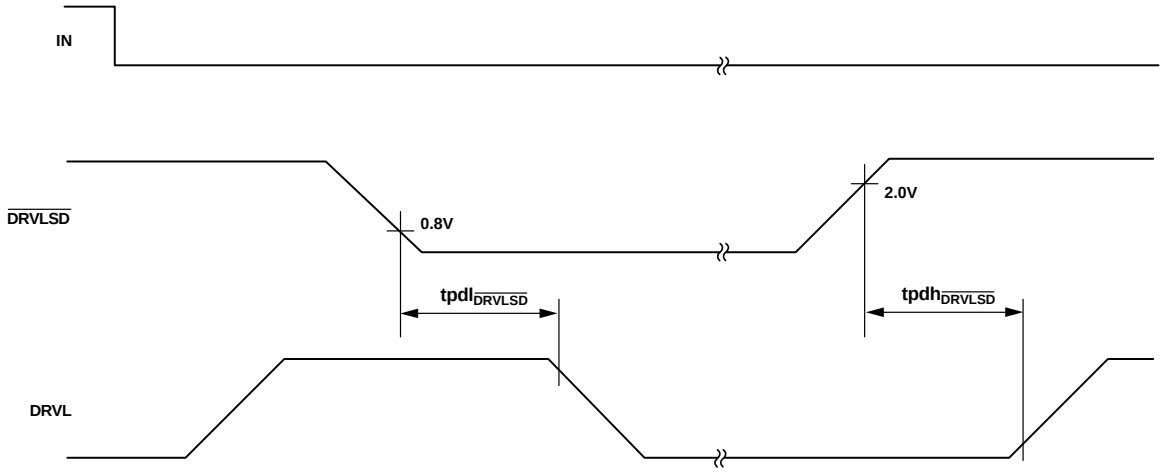

Figure 3. Output Disable Timing Diagram
(Timing is Referenced to the 90% and 10% Points Unless Otherwise Noted)

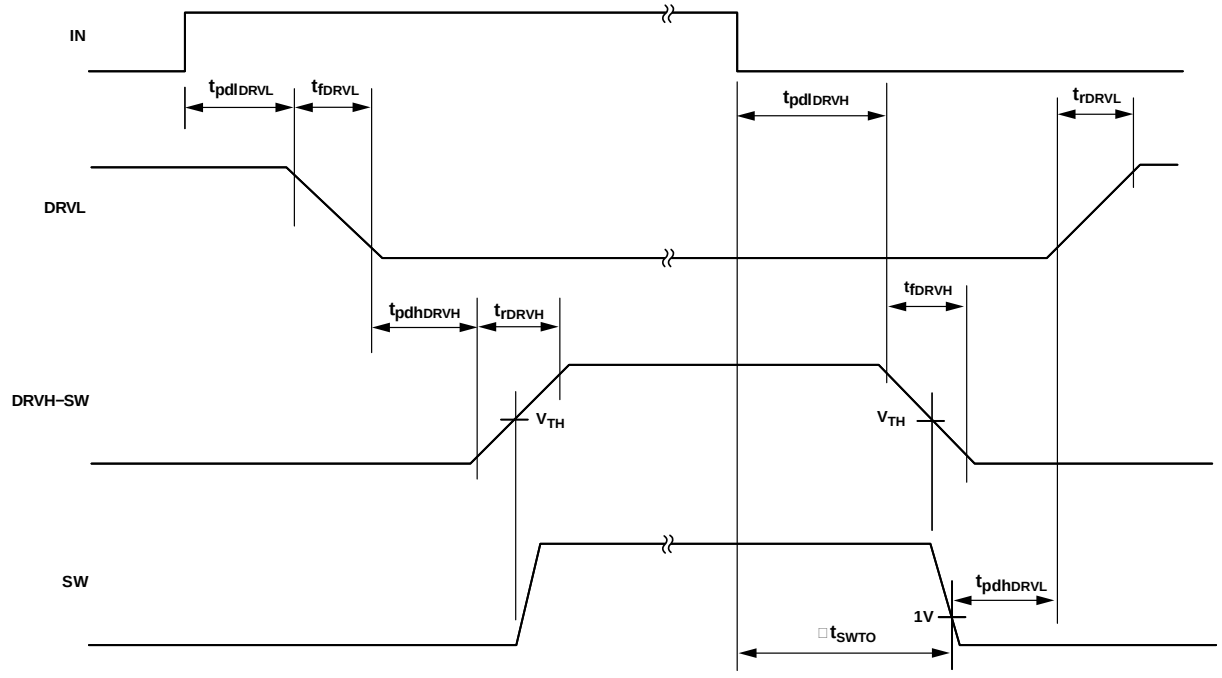

Figure 4. Non−Overlap Timing Diagram
(Timing is Referenced to the 90% and 10% Points Unless Otherwise Noted)

TYPICAL CHARACTERISTICS

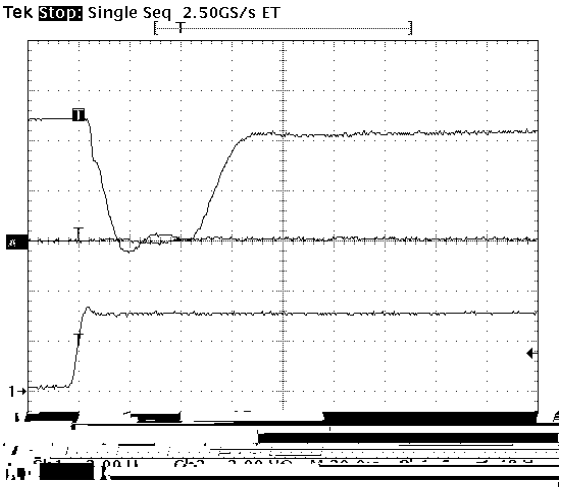

Figure 5. DRVH Rise and DRVL Fall Times
CH1 = IN, CH2 = DRVH, CH3 = DRVL

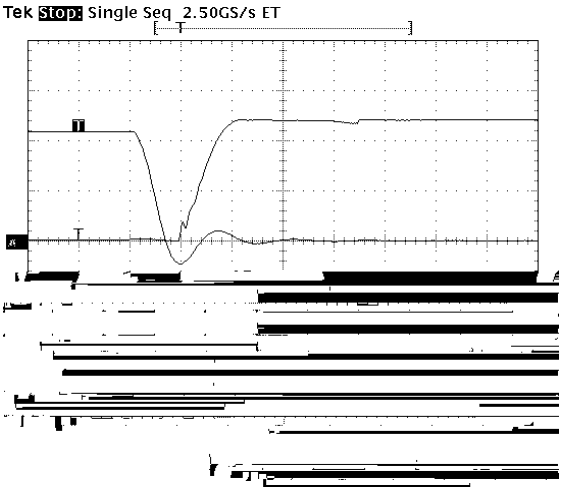

Figure 6. DRVH Fall and DRVL Rise Times
CH1 = IN, CH2 = DRVH, CH3 = DRVL

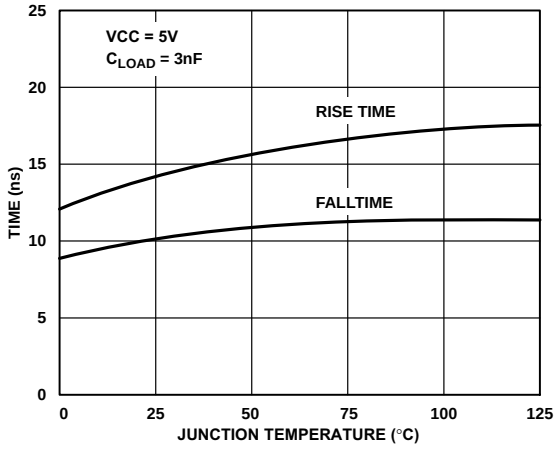

Figure 7. DRVH Rise and Fall Times vs. Temperature

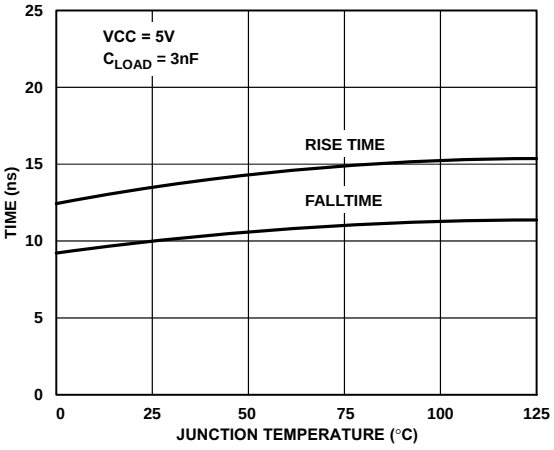

Figure 8. DRVL Rise and Fall Times vs. Temperature

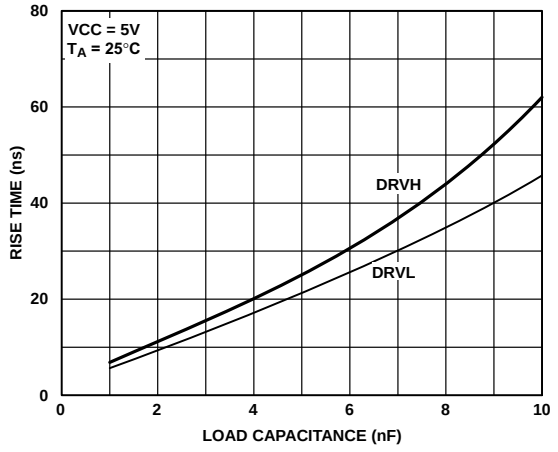

Figure 9. DRVH and DRVL Rise Times vs. Load Capacitance

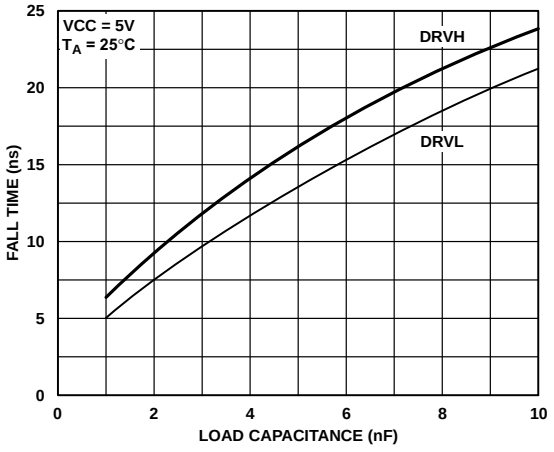

Figure 10. DRVH and DRVL Fall Times vs. Load Capacitance

TYPICAL CHARACTERISTICS

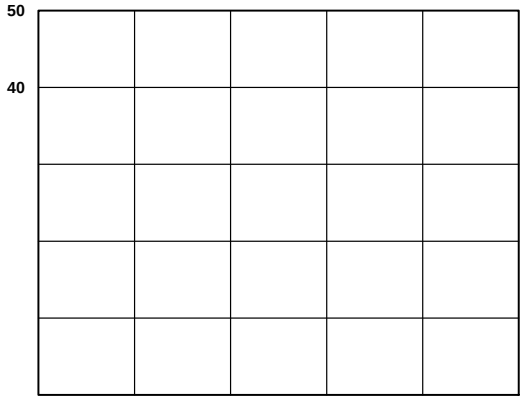

Figure 11. DRVH and DRVL t_{pdh} vs. Temperature

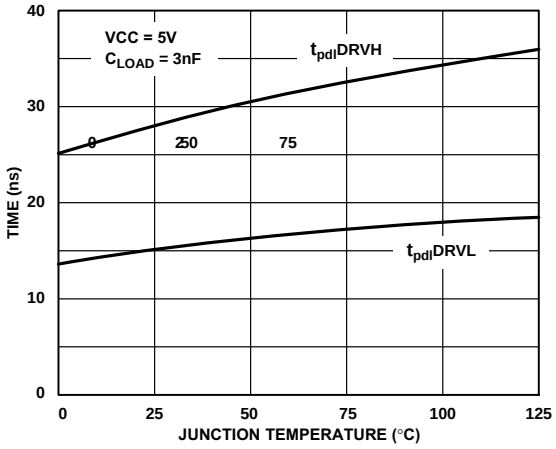

Figure 12. DRVH and DRVL t_{pdl} vs. Temperature

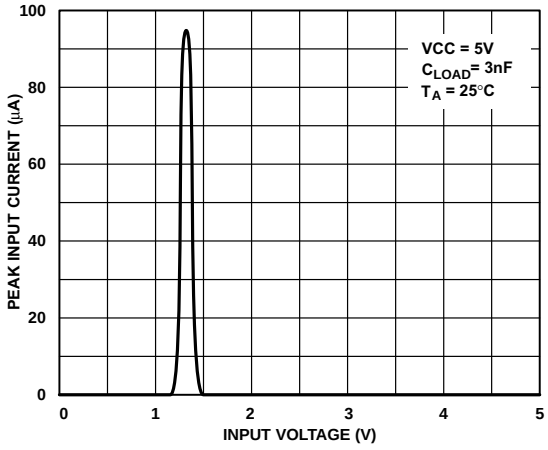

Figure 13. IN Pin Input Current vs. Input Voltage

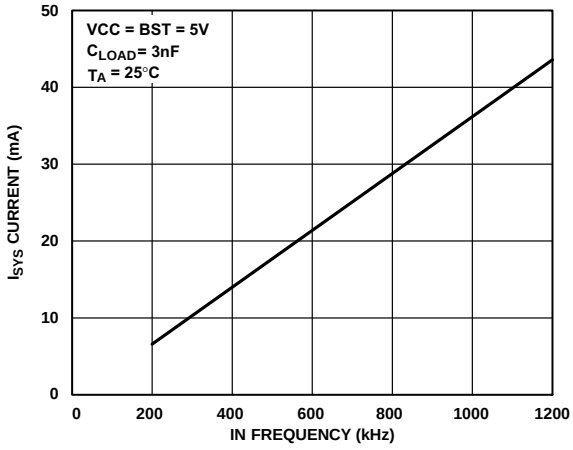

Figure 14. Supply Current vs. Frequency

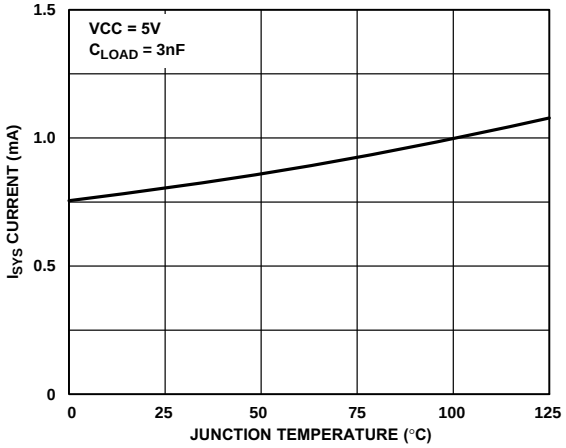

Figure 15. Supply Current vs. Temperature

Theory of Operation

The ADP3419 is a dual MOSFET driver optimized for driving two N-channel MOSFETs in a synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high-side and the low-side MOSFETs. Each driver is capable of driving a 3 nF load at speeds up to 1 MHz. A more detailed description of the ADP3419 and its features follows. Refer to the detailed block diagram in Figure 16.

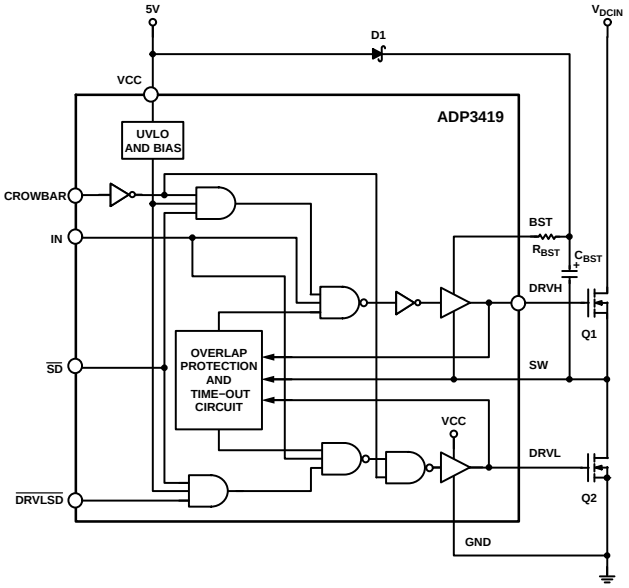

Figure 16. Detailed Block Diagram of the ADP3419

When $\overline{\text{DRVLSD}}$ is low, the low-side driver stays low. When $\overline{\text{DRVLSD}}$ is high, the low-side driver is enabled and controlled by the driver signals, as previously described.

Low-Side Driver Timeout

In normal operation, the DRVH signal tracks the IN signal and turns off the Q1 high-side switch with a few 10 ns delay ($t_{pdlDRVH}$) following the falling edge of the input signal. When Q1 is turned off, DRVL is allowed to go high, Q2 turns on, and the SW node voltage collapses to zero. But in a fault condition such as a high-side Q1 switch drain-source short circuit, the SW node cannot fall to zero, even when DRVH goes low. The ADP3419 has a timer circuit to address this scenario. Every time the IN goes low, a DRVL on-time delay timer is triggered. If the SW node voltage does not trigger a low-side turn-on, the DRVL on-time delay circuit does it instead, when it times out with $t_{SW(TO)}$ delay. If Q1 is still turned on, that is, its drain is shorted to the source, Q2 turns on and creates a direct short circuit across the V_{DCIN} voltage rail. The crowbar action causes the fuse in the V_{DCIN} current path to open. The opening of the fuse saves the load (CPU) from potential damage that the high-side switch short circuit could have caused.

Crowbar Function

In addition to the internal low-side drive time-out circuit, the ADP3419 includes a CROWBAR input pin to provide a means for additional overvoltage protection. When CROWBAR goes high, the ADP3419 turns off DRVH and turns on DRVL. The crowbar logic overrides the overlap protection circuit, the shutdown logic, the $\overline{\text{DRVLSD}}$ logic, and the UVLO protection on DRVL. Thus, the crowbar function maximizes the overvoltage protection coverage in the application. The CROWBAR can be either driven by the CLAMP pin of buck controllers, such as the ADP3422, ADP3203, ADP3204, or ADP3205, or controlled by an independent overvoltage monitoring circuit.

Table 1. ADP3419 Truth Table

CROWBAR	UVLO	$\overline{\text{SD}}$	$\overline{\text{DRVLSD}}$	IN	DRVH	DRVL
L	L	H	H	H	H	L
L	L	H	H	L	L	H
L	L	H	L	H	H	L
L	L	H	L	L	L	L
L	L	L	*	*	L	L
L	H	*	*	*	L	L
H	L	*	*	*	L	H
H	H	*	*	*	L	H

* = Don't Care.

Application Information

Supply Capacitor Selection

For the supply input (VCC) of the ADP3419, a local bypass capacitor is recommended to reduce the noise and to supply some of the peak currents drawn. Use a 10 μF or 4.7 μF multilayer ceramic (MLC) capacitor. MLC capacitors provide the best combination of low ESR and small size, and can be obtained from the following vendors.

Table 2.

Vendor	Part Number	Web Address
Murata	GRM235Y5V106Z16	www.murata.com
Taiyo-Yuden	EMK325F106ZF	www.t-yuden.com
Tokin	C23Y5V1C106ZP	www.tokin.com

Keep the ceramic capacitor as close as possible to the ADP3419.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BST}) and a Schottky diode (D1), as shown in Figure 16. Selection of these components can be done after the high-side MOSFET has been chosen. The bootstrap capacitor must have a voltage rating that is able to handle at least 5.0 V more than the maximum supply voltage. The capacitance is determined by:

$$C_{BST} = \frac{Q_{HSGATE}}{\Delta V_{BST}} \quad \text{(eq. 1)}$$

where:

Q_{HSGATE} is the total gate charge of the high-side MOSFET.

ΔV_{BST} is the voltage droop allowed on the high-side MOSFET drive.

For example, two IRF7811 MOSFETs in parallel have a total gate charge of about 36 nC. For an allowed droop of 100 mV, the required bootstrap capacitance is 360 nF. A good quality ceramic capacitor should be used, and derating for the significant capacitance drop of MLCs at high temperature must be applied. In this example, selection of 470 nF or even 1 μF would be recommended.

A Schottky diode is recommended for the bootstrap diode due to its low forward drop, which maximizes the drive Tw((C)Tj8 0

PACKAGE DIMENSIONS

MSOP10
CASE 846AC−01
ISSUE O