ADP3611

D B ', H
MO FE D
O D

ON Semiconductor

http://onsemi.com

DFN8
CP SUFFIX
CASE 506AA

MARKING DIAGRAMS

Features

- All in one Synchronous Buck Driver
- One PWM Signal Generates Both Drives
- Anticross conduction Protection Circuitry
- Output Disable Function
- Crowbar Control
- Synchronous Override Control
- This is a Pb Free Device

Applications

- Mobile Computing CPU Core Power Converters
- Multiphase Desk note CPU Supplies
- Single supply Synchronous Buck Converters
- Nonsynchronous to Synchronous Drive Conversion

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM

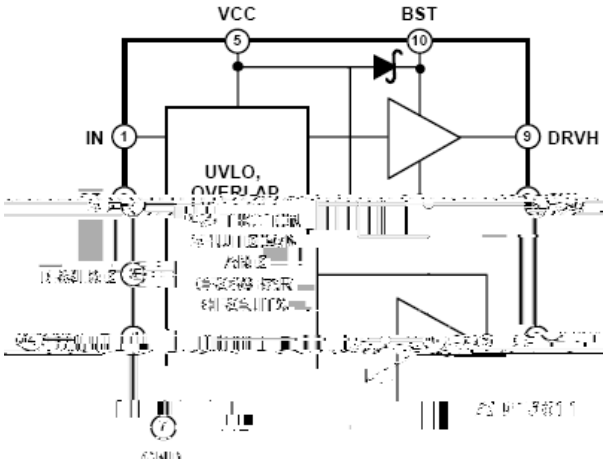


Figure 1. MSOP−10 Package Block Diagram

GENERAL APPLICATION CIRCUIT

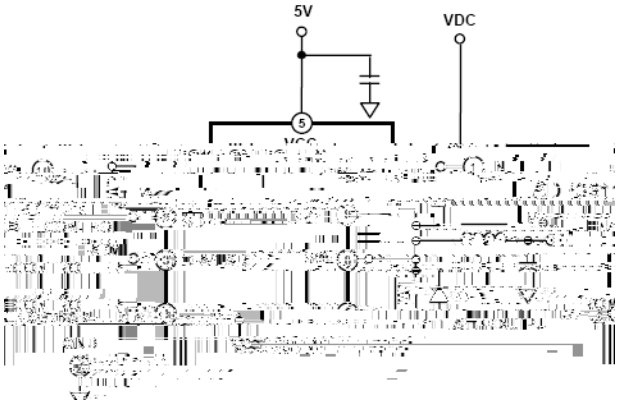


Figure 2. MSOP−10 Package Application Circuit

Table 1. ORDERING INFORMATION

Model	Temperature Range	Package Description	Package Option	Quantity per Reel	Branding
–	– ° °	–	–		

Table 2. ELECTRICAL CHARACTERISTICS — – – ° °

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LOGIC INPUTS (IN, $\overline{SD}$, $\overline{DRVLSD}$, CROWBAR)						

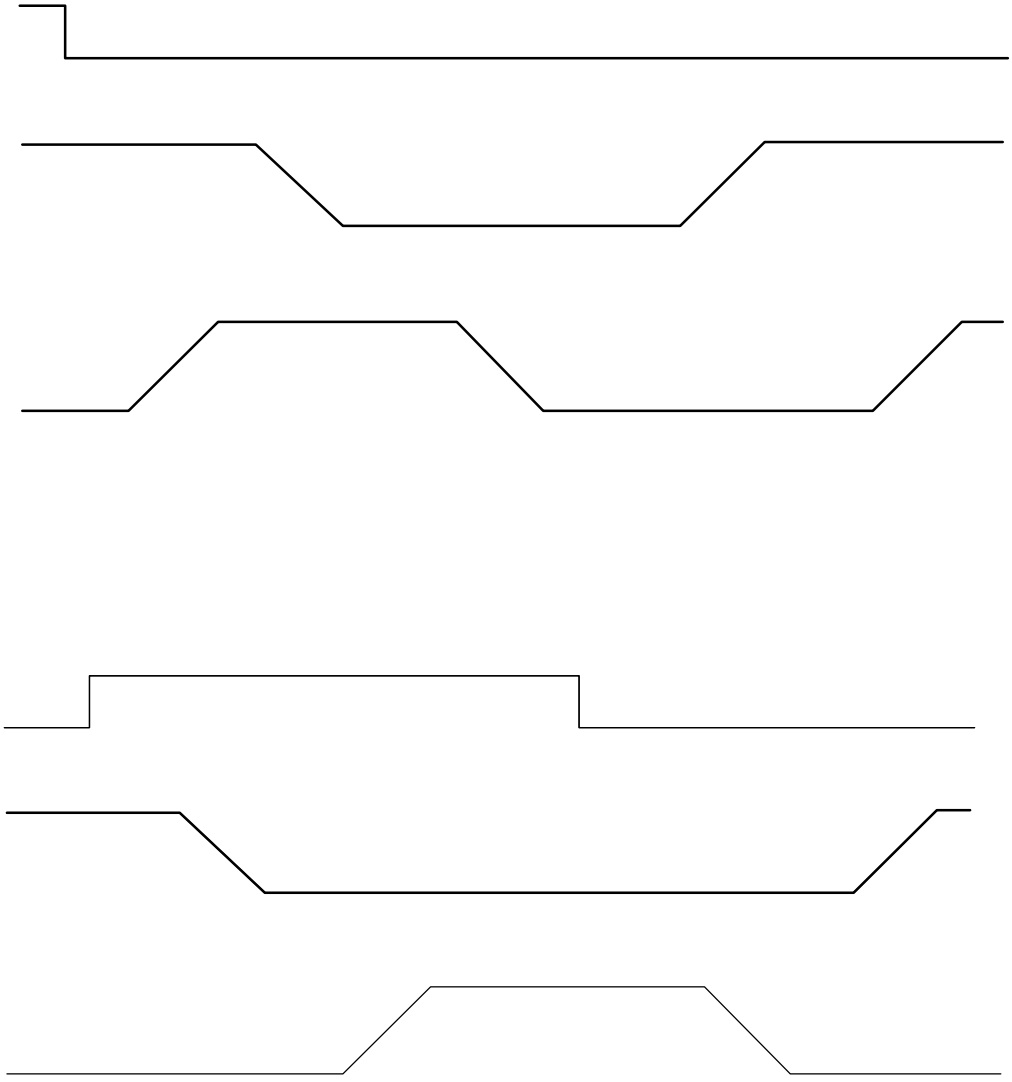


Table 3. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
	–	
	– –	
	–	
	– –	
	– –	
	–	
	–	
	– –	
	–	
– – –		°
–		°
	– –	°

Table 4. PIN FUNCTION DESCRIPTIONS

Pin No. QFN	

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 7. DRVH Rise and DRVL Fall Times
CH1 = IN, CH2 = DRVH, CH3 = DRVL

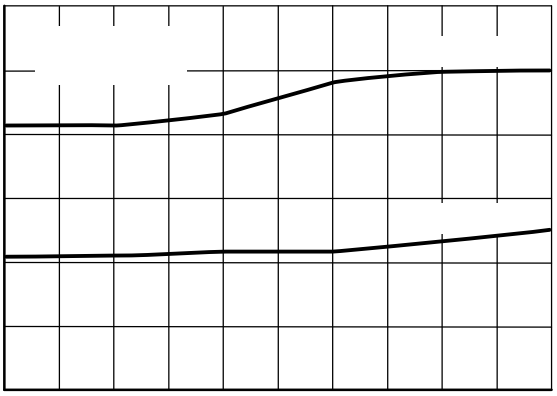


Figure 8. DRVH Fall and DRVL Rise Times
CH1 = IN, CH2 = DRVH, CH3 = DRVL

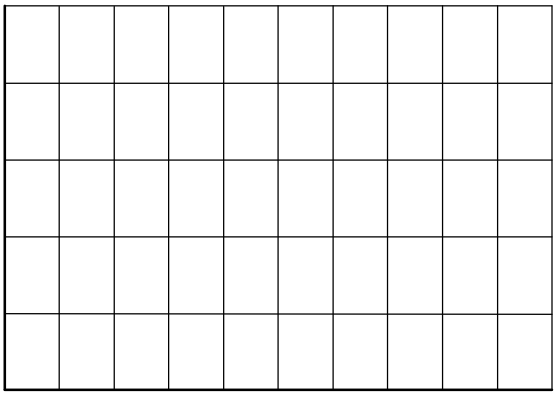


Figure 9. DRVH Rise and Fall Times vs. Temperature

Figure 10. DRVL Rise and Fall Times vs. Temperature

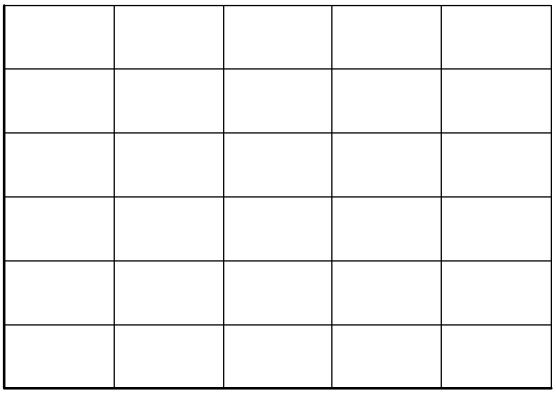


Figure 11. DRVH and DRVL Rise Times vs. Load Capacitance

Figure 12. DRVH and DRVL Fall Times vs. Load Capacitance

TYPICAL PERFORMANCE CHARACTERISTICS

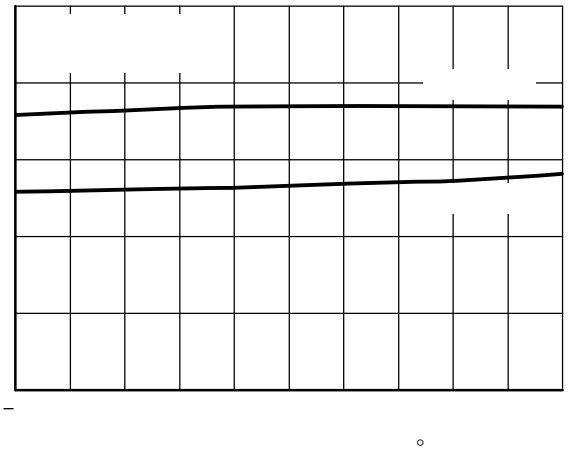


Figure 13. DRVH and DRVL t_{pdh} vs. Temperature

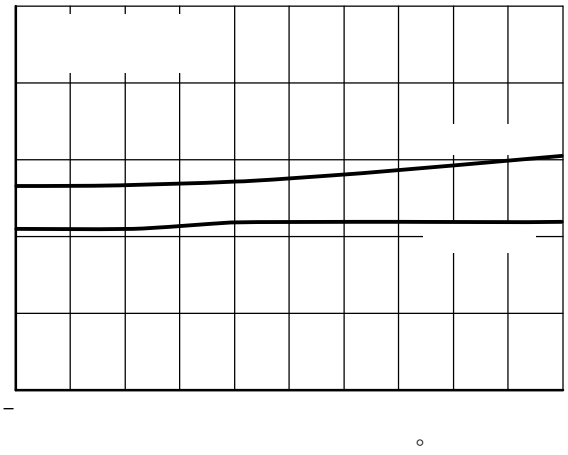


Figure 14. DRVH and DRVL t_{pdl} vs. Temperature

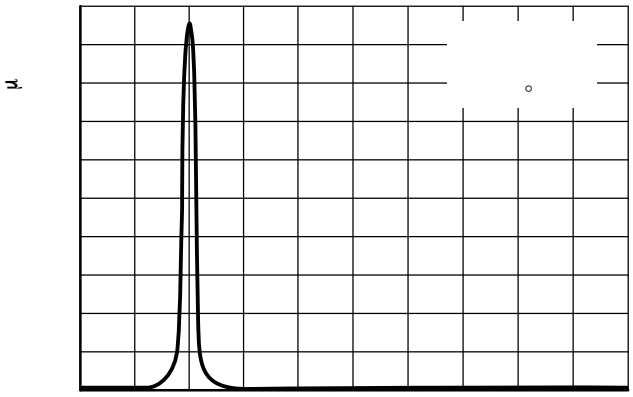


Figure 15. IN Pin Input Current vs. Input Voltage

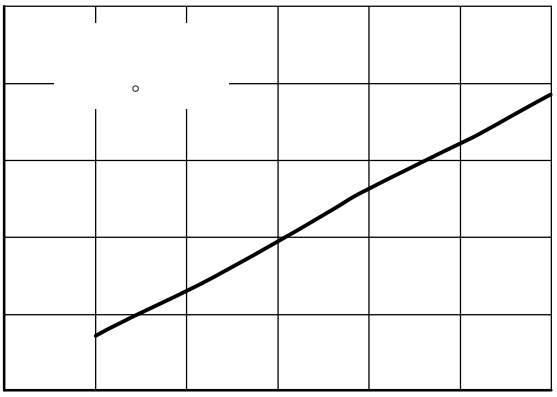


Figure 16. Supply Current vs. Frequency

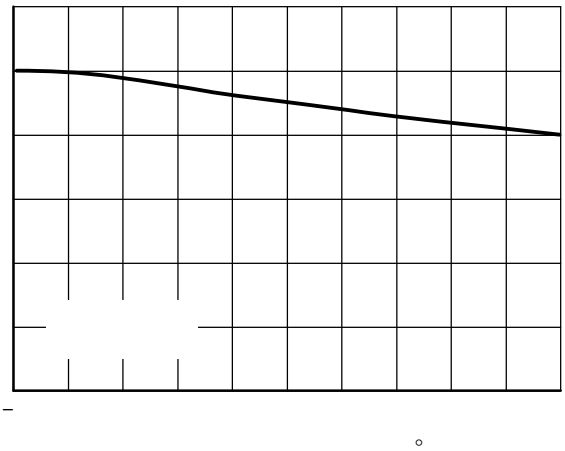


Figure 17. Supply Current vs. Temperature

THEORY OF OPERATION

The ADP3611 is a dual MOSFET driver optimized for driving two N-channel MOSFETs in a synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high-side and the low-side MOSFETs. Each driver is capable of driving a 3 nF load at speeds up to 1 MHz. A more detailed description of the ADP3611 and its features follows. Refer to the detailed block diagram in Figure 18.

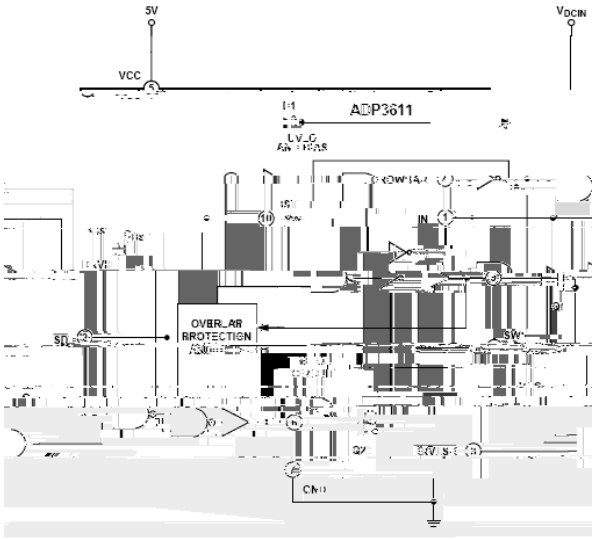


Figure 18. Detailed Block Diagram of the ADP3611

Undervoltage Lockout

The undervoltage lockout (UVLO) circuit hold4-twboth for

polarity reversal of the inductor current to maximize light load conversion efficiency. $\overline{\text{DRVLSD}}$ can also be pulled low for reverse voltage protection purposes.

When $\overline{\text{DRVLSD}}$ is low, the low-side driver stays low. When $\overline{\text{DRVLSD}}$ is high, the low-side driver is enabled and controlled by the driver signals, as previously described.

Low−Side Driver Timeout

In normal operation, the DRVH signal tracks the IN signal and turns off the Q1 high-side switch with a few 10 ns delay ($t_{pdlDRVH}$) following the falling edge of the input signal. When Q1 is turned off, DRVL is allowed to go high, Q2 turns on, and the SW node voltage collapses to zero. But in a fault condition such as a high-side Q1 switch drain-source short circuit, the SW node cannot fall to zero, even when DRVH goes low. The ADP3611 has a timer circuit to address this scenario. Every time the IN goes low, a DRVL on-time delay timer is triggered. If the SW node voltage does not trigger a low-side turn-on, the DRVL on-time delay circuit does it instead, when it times out with $t_{SW(TO)}$ delay. If Q1 is still turned on, that is, its drain is shorted to the source, Q2 turns on and creates a direct short circuit across the V_{DCIN} voltage rail. The crowbar action causes the fuse in the V_{DCIN} current path to open. The opening of the fuse saves the load (CPU) from potential damage that the high-side switch short circuit could have caused.

Crowbar Function

In addition to the internal low-side drive time-out circuit, the ADP3611 includes a CROWBAR input pin to provide a means for additional overvoltage protection. When CROWBAR goes high, the ADP3611 turns off DRVH and turns on DRVL. The crowbar logic overrides the overlap protection circuit, the shutdown logic, the $\overline{\text{DRVLSD}}$ logic,

Power and Thermal Considerations

The major power consumption of the ADP3611-based driver circuit is from the dissipation of MOSFET gate charge. It can be estimated as

≈ × + ×

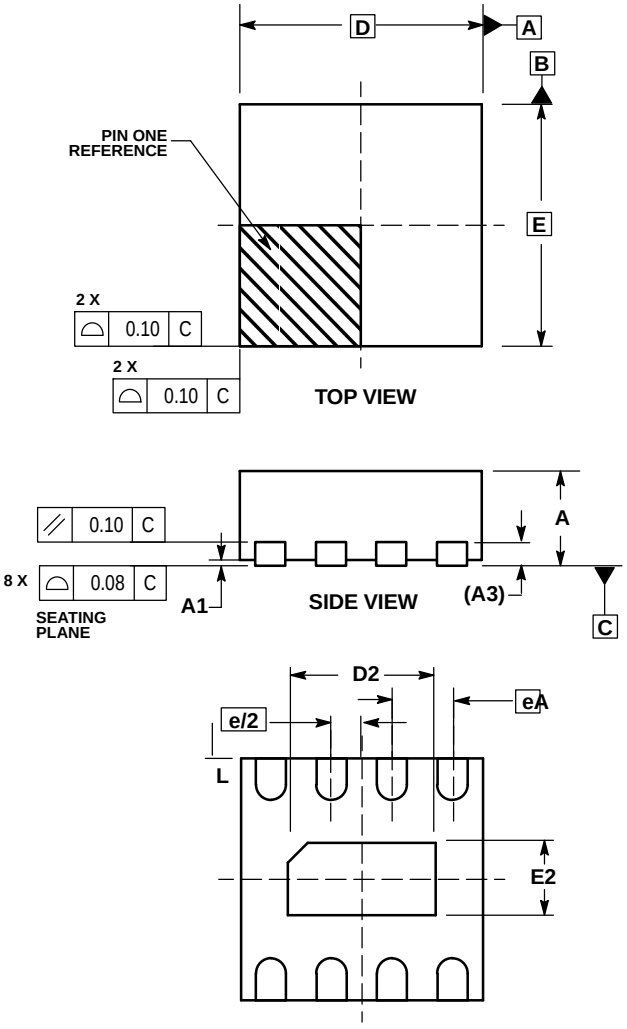
where:

V_{CC} is the supply voltage 5 V.

f_{MAX}

PACKAGE DIMENSIONS

DFN8



PACKAGE DIMENSIONS

MSOP10