ADP4000

with I²C Interface

The ADP4000 is an integrated power control IC with an I²C interface. The ADP4000 can be programmed for 1-, 2-, 3-, 4-, 5- or 6-phase operation, allowing for the construction of up to six complementary buck switching stages. The ADP4000 supports PSI, which is a power state indicator and can be used to reduce number of operating phases at light loads. The ADP4000 includes an I²C interface, which can be used to program system set points such as voltage offset, load line, phase balance and output voltage. Key system performance data such as CPU current, CPU voltage, and power and fault conditions can also be read back over the I²C interface from the ADP4000.

Features

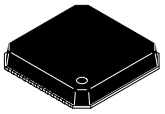
- I²C Interface
- Supports Both VR11 and VR11.1 Specifications
- Digitally Programmable 0.375 V to 1.6 V Output
- Additional 200 mV Offset Programmable (Max 1.8 V Output)
- Selectable 1-, 2-, 3-, 4-, 5-, or 6-Phase Operation
- Fast-Enhanced PWM FlexMode™
- TRDET to Improve Load Release
- Active Current Balancing Between All Output Phases
- Supports On−The−Fly (OTF) VID Code Changes
- Supports $\overline{\text{PSI}}$ – Power Saving Mode
- This is a Pb−Free Device

Typical Applications

- Servers
- Desktop PC's
- POLs (Memory)

http://onsemi.com

MARKING DIAGRAM



PIN ASSIGNMENT

ORDERING INFORMATION

Device*	Package	Shipping†
ADP4000JCPZ−REEL	LFCSP48	2500/Tape & Reel
ADP4000JCPZ−RL7	LFCSP48	750/Tape & Reel

*The "Z' suffix indicates Pb−Free package.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Figure 1. Block Diagram

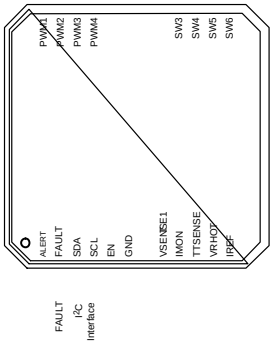


Figure 2. Application Schematic

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Range (Note 1)	V_{IN}	−0.3 to 6	V
FBRTN	V_{FBRTN}	−0.3 to + 0.3	V
PWM2 to PWM6, Rampadj		−0.3 to V_{IN} + 0.3	V
SW1 to SW6		−5 to +25	V
SW1 to SW6 (<200 ns|)		−10 to +25	V
All other Inputs and Outputs		−0.3 to V_{IN} + 0.3	V
Storage Temperature Range	TSTG	−65 to 150	°C
Operating Ambient Temperature Range		0 to 85	°C

PIN ASSIGNMENT

Pin No.	Pin Name	Description
1	ALERT	

ELECTRICAL CHARACTERISTICS
V_{IN}

ELECTRICAL CHARACTERISTICS

V_{IN} = (5.0 V) FBRTN = GND, for typical values T_A = 25°C, for min/max values T_A = 0°C to 85°C; unless otherwise noted. (Notes 1 and 2)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
PSI						
Input Low Voltage					0.3	V
Input High Voltage			0.8			V
Input Current				−5		□A
Assertion Timing	Fsw = 300kHz			3.3		□s
Deassertion Timing	Fsw = 300kHz				825	ns
TRDET						
Output Low Voltage	I_{OUT} 685.9278.6662 60d2 .9071 ref489.77 617	87Tf.582 0 TD	-.00586	mA00kHz		

0.8 V

ADP4000

TEST CIRCUITS

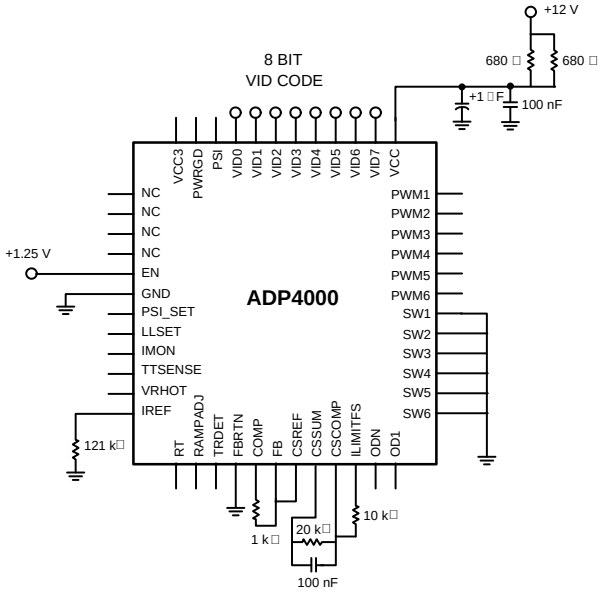


Figure 4. Closed-Loop Output Voltage Accuracy

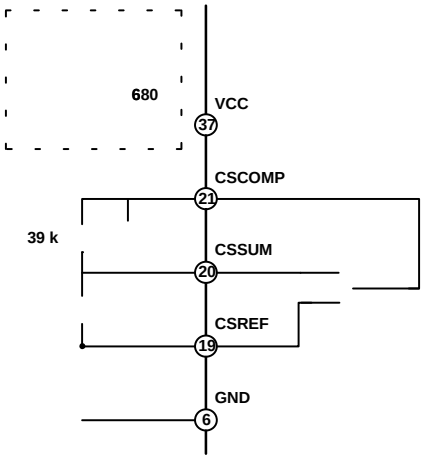


Figure 5. Current Sense Amplifier VOS

Description

The ADP4000 is a 6−Phase VR11.1 regulator with an I^2C Interface Typical application circuits is shown in Figure 2.

Startup Sequence

The ADP4000 follows the VR11 startup sequence shown in Figure 7. After both the EN and UVLO conditions are met, a programmable internal timer goes through one delay cycle TD1. This delay cycle is programmed using Delay Command, default delay = 2 ms, see Table 1 for programmable values). The first six clock cycles of TD2 are blanked from the PWM outputs and used for phase detection as explained in the following section. Then the programmable internal soft−start ramp is enabled (TD2) and the output comes up to the boot voltage of 1.1 V. The boot hold time is also set by Delay Command. This second delay cycle is called TD3. During TD3 the processor VID pins settle to the required VID code. When TD3 is over, the ADP4000 reads the VID inputs and soft−starts either up or down to the final VID voltage (TD4). After TD4 has been completed and the PWRGD masking time (equal to VID on the fly masking) is finished, a third cycle of the internal timer sets the PWRGD blanking (TD5).

The internal delay and soft−start times are programmable using the serial interface and the Delay Command and the Soft−

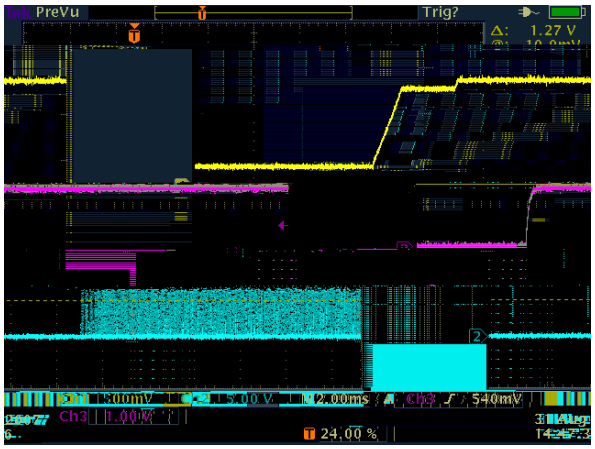


Figure 8. System Startup Sequence for VR11

Figure 8 shows typical startup waveforms for the ADP4000.

Figure 8. Typical Startup Waveforms
Channel 1: CSREF (yellow)
Channel 2: PWM1 (blue)
Channel 3 : Enable (pink)

Phase Detection

During startup, the number of operational phases and their phase relationship is determined by the internal circuitry that monitors the PWM outputs. Normally, the ADP4000

using the I^{2}C Loadline Calibration (0xDE) and Loadline Set (0xDF) commands.

The difference between CSREF and CSCOMP is used as a differential input for the current-limit comparator.

To provide the best accuracy for sensing current, the CSA is designed to have a low offset input voltage. Also, the sensing gain is determined by external resistors to make it extremely accurate.

The CPU current can also be monitored over the I^{2}C interface. The current limit and the load line can be adjusted from the circuit component values over the I^{2}C interface.

Current Limit Setpoint

The current limit threshold on the ADP4000 is programmed by a resistor between the ILIMFS pin and the CSCOMP pin. The ILIMFS current, I_{ILIMFS}, is compared with an internal current reference of 22 □A. If I_{ILIMFS} exceeds 22 □A then the output current has exceeded the limit and the current limit protection is tripped.

Where $V_{ILIMFS} = V_{CSREF}$

$$I_{ILIMFS} = \frac{V_{ILIMFS} - V_{CSCOMP}}{R_{ILIMFS}} \quad \text{(eq. 2)}$$

$$V_{CSREF} - V_{CSCOMP} = \frac{R_{CS}}{R_{PH}} \times R_L \times I_{LOAD} \quad \text{(eq. 3)}$$

Where R_L = DCR of the Inductor.

Assuming that

$$\frac{R_{CS}}{R_{PH}} \times R_L = 1\ m\Omega \quad \text{(eq. 4)}$$

i.e. the external circuit is set up for a 1m□ Loadline then the R_{ILIMFS} is calculated as follows

$$I_{ILIMFS} = \frac{1\ m\Omega \times I_{LOAD}}{R_{ILIMITFS}} \quad \text{(eq. 5)}$$

Assuming we want a current limit of 150A that means that I_{LIMFS} must equal 22 □A at that load.

$$20\ \mu A = \frac{1\ m\Omega \times 150\ AD}{R_{ILIMITFS}} = 6.8\ k\Omega \quad \text{(eq. 6)}$$

Solving this equation for $R_{LIMITFS}$ we get 6.8 k□. The closest 1% resistor value is 6.8 k□.

The current limit threshold can be modified from the resistor programmed value by using the I^{2}C interface using Bits <4:0> of the Current Limit Threshold command (0xE2). The limit is programmable between 50% of the external limit and 146.7% of the external limit. The resolution is 3.3%. Table 3 gives some examples codes.

Table 3. Current Limit

Code	Current Limit (% of external limit)
0 0000	50%
0 0001	53.3%
1 0000	100% = default
1 0001	103.3%
1 1110	143.3%
1 1111	146.7%

Current Limit, Short−Circuit and Latchoff protection

If the current limit is reached and TD5 has completed the controller will start to latchoff. If there is a current limit during startup, the ADP4000 will go through TD1 to TD5, and then start the latchoff. Because the controller continues to cycle the phases during the latchoff, if the short is removed before the timer is complete, the controller can return to normal operation.

The latchoff function can be reset by either removing and reapplying the supply voltage to the ADP4000, or by toggling the EN pin low for a short time.

During startup when the output voltage is below 200 mV, a secondary current limit is active. This is necessary because the voltage swing of CSCOMP cannot go below ground. This secondary current limit limits the internal COMP voltage to the PWM comparators to 1.5 V. This limits the

commonly known as active voltage positioning. The output of the amplifier is the COMP pin, which sets the termination voltage for the internal PWM ramps.

The negative input (FB) is tied to the output sense location with Resistor R_B and is used for sensing and controlling the output voltage at this point. A current source (equal to I_{FB}) from the FB pin flowing through R_B is used for setting the no load offset voltage from the VID voltage. The no load voltage is negative with respect to the VID DAC for Intel CPU's.

The value of R_B can be found using the following equation:

$$R_B = \frac{V_{VID} - V_{ONL}}{I_{IFB}} \quad \text{(eq. 12)}$$

An offset voltage can be added to the control voltage over the serial interface. This is done using Bits <5:0> of the V_{OUT}_TRIM (0xDB) and V_{OUT}_CAL (0xDC) Commands. The max offset that can be applied is ±193.75 mV (even if the sum of the offsets > 193.75mV). The LSB size is 6.25 mV. A positive offset is applied when Bit 5 = 0. A negative offset is applied when Bit 5 = 1.

Table 5. Offset Codes

VOUT_ TRIM CODE	TRIM OFFSET VOLTAGE	VOUT_ CAL CODE	CAL OFFSET VOLTAGE	TOTAL OFFSET VOLTAGE
00 1000	50 mV			

The transition slew rate is programmed using Bits <2:0> of the Ton_Transition (0xD6) command code. Table 6 provides the soft−start values.

Table 6. Transition Rate Codes

Code	Transition Rate (V/msec)
000	1
001	3 = default
010	5
011	7
100	9
101	11
110	13
111	15

Enhanced Transients Mode

The ADP4000 incorporates enhanced transient response for both load step up and load release. For load step up it senses the output of the error amp to determine if a load step up has occurred and then sequences on the appropriate number of phases to ramp up the output current.

For load release, it also senses the output of the error amp and uses the load release information to trigger the TRDET pin, which is then used to adjust the error amp feedback for optimal positioning. This is especially important during high frequency load steps.

Additional information is used during load transients to ensure proper sequencing and balancing of phases during high frequency load steps as well as minimizing the stress on components such as the input filter and MOSFET’s.

TRDET and Phase Shuffling

The ADP4000 senses the error amp output and triggers the TRDET pin when a load release takes place. The TRDET

The user can program how many phases are enabled when $\overline{PSI}$ is asserted. By default only phase 1 is enabled. The number of phases enabled can be changed over the I^2C interface. However extreme care should be taken to ensure that $\overline{OD1}$ is connected to all phases enabled during $\overline{PSI}$. The number of phases enabled during $\overline{PSI}$ is programmed using Bits 7 and 6 of the MFR Config Command (0xD1)

Table 9. # Phases Enabled During $\overline{PSI}$

# of Phases Running Normally	Code	# of Phases Running During $\overline{PSI}$	Phases Running
6	00	1	1
	01	2	1 and 4
	10	3	1, 3 and 5
	11	1	1
5	00	1	1
	01	2	1 and 4
	10	1	1
	11	1	1
4	00	1	1
	01	2	1 and 3
	10	1	1
	11	1	1
3	00	1	1
	01	1	1
	10	1	1
	11	1	1
2	00	1	1
	01	1	1
	10	1	1
1	00		1

0 V to 2.0 V. Voltages greater than 2.0 V can monitored using a resistor divider network. Voltage measurements are 10 bits wide.

Vsense1 is intended to measure the input voltage and report this back in the READ_VIN command. However the input voltage is typically 12 V and the ADC range is only 0 V to 2.0 V. Therefore an external resistor divided is needed, the ADP4000 assumes that an 8−1 resistor divider is used, the ADP4000 measures the voltage on the pin and multiples by 8 and places the result in the Read V_{in} register. The circuit in Figure 2 uses a 6.8 K and a 1.0 k resistor to divide the input voltage by 8.

Shunt Resistor

The ADP4000 uses a shunt to generate 5.0 V from the 12 V supply range. A trade-off can be made between the power dissipated in the shunt resistor and the UVLO threshold. Figure 10 shows the typical resistor value needed to realize certain UVLO voltages. It also gives the maximum power dissipated in the shunt resistor for these UVLO voltages.

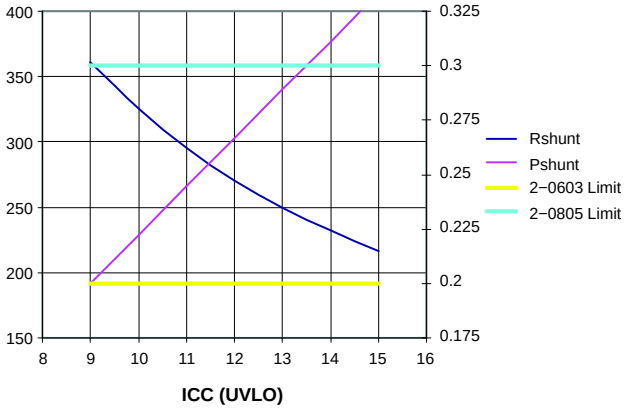


Figure 10. Typical Shunt Resistor Value and Power Dissipation for Different UVLO Voltage

The maximum power dissipated is calculated using the Equation 18.

$$P_{MAX} = \frac{\left(V_{IN(MAX)} - V_{CC(MIN)}\right)^2}{R_{SHUNT}} \qquad \text{(eq. 18)}$$

where:

$V_{IN(MAX)}$ is the maximum voltage from the 12 V input supply (if the 12 V input supply is 12 V ±5%, $V_{IN(MAX)}$ = 12.6 V; if the 12 V input supply is 12 V ±10%, $V_{IN(MAX)}$ = 13.2 V). $V_{CC(MIN)}$ is the minimum V_{CC} voltage of the ADP4000. This is specified as 4.75 V.

R_{SHUNT} is the shunt resistor value.

The CECC standard specification for power rating in surface-mount resistors is: 0603 = 0.1 W, 0805 = 0.125 W, 1206 = 0.25 W.

I²C Interface

Control of the ADP4000 is carried out using the I²C Interface.

The ADP4000 is connected to this bus as a slave device, under the control of a master controller.

To setup the I²C Address the ADP4000 sources a 10 □A current from the ADD pin through an external resistor. The voltage is then measured by the ADC and user to set the I²C address. The table below gives the thresholds for each possible I²C address.

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Table 10. Setting Up the I²C Address

Address (8 Bits)	High Threshold	Low Threshold
0xC0	0.1	–
0xC2	0.225	0.15
0xC4	0.45	0.3
0xC6	0.675	0.5
0xC8	0.9	0.75
0xCA	1.25	1.0
0xCC	1.7	1.35
0xCE	–	1.8

Data is

10. The master asserts a stop condition on SDA and the transaction ends.

The word write operation is shown in Figure 16.

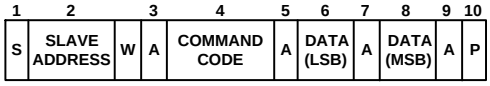

Figure 16. Single Word Write to a Register

Block Write

In this operation, the master device sends a command byte and a byte count followed by the stated number of data bytes to the slave device as follows:

1. The master device asserts a START condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends the byte count N.
7. The slave asserts ACK on SDA.
8. The master sends the first data byte.
9. The slave asserts ACK on SDA.
10. The master sends the second data byte.
11. The slave asserts ACK on SDA.
12. The master sends the remainder of the data byes.
13. The slave asserts an ACK on SDA after each data byte.
14. After the last data byte the master asserts a STOP condition on SDA.

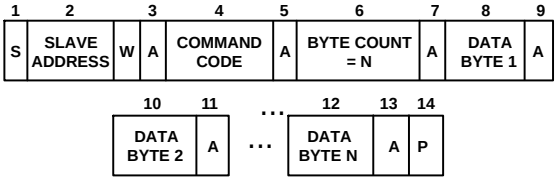

Figure 17. Block Write to a Register

Read Operations

The ADP4000 uses the following I^2C read protocols.

Read Byte

In this operation, the master device receives a single byte from a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserted ACK on SDA.
6. The master sends a repeated start condition on SDA.
7. The master sends the 7 bit slave address followed by the read bit (high).
8. The slave asserts ACK on SDA.
9. The slave sends the Data Byte.
10. The master asserts NO ACK on SDA.
11. The master asserts a stop condition on SDA and the transaction ends.

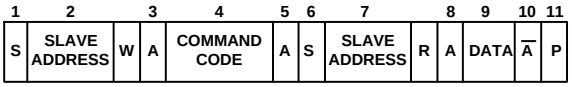

Figure 18. Single Read from a Register

Read Word

In this operation, the master device receives two data bytes from a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserted ACK on SDA.
6. The master sends a repeated start condition on SDA.
7. The master sends the 7 bit slave address followed by the read bit (high).
8. The slave asserts ACK on SDA.
9. The slave sends the first Data Byte (low Data Byte).
10. The master asserts ACK on SDA.
11. The slave sends the second Data Byte (high Data Byte).
12. The masters asserts a No ACK on SDA.
13. The master asserts a stop condition on SDA and the transaction ends.

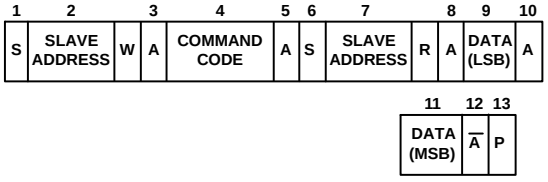

Figure 19. Word Read from a Command Code

Block Read

In this operation, the master device sends a command byte, the slave sends a byte count followed by the stated number of data bytes to the master device as follows:

1. The master device asserts a START condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a REPEATED START condition on SDA.
5. The master sends the 7-bit slave address followed by the read bit (high).
6. The slave asserts ACK on SDA
7. The slave sends the byte count N.

8. The master asserts ACK on SDA.
9. The slave sends the first data byte
10. The master asserts ACK on SDA.
11. The slave sends the remainder of the data byes, the master asserts an ACK on SDA after each data byte.
12. After the last data byte the master asserts a No ACK on SDA.
13. The master asserts a STOP condition on SDA.

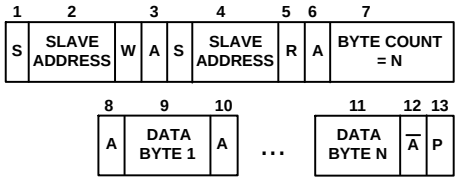

Figure 20. Block Write to a Command Coder

Bus Timeout

The ADP4000 includes an I^2C timeout feature. If there is no I^2C activity for 35 ms, the ADP4000 assumes that the bus is locked and releases the bus. This prevents the device from locking or holding the I^2C expecting data. The timeout feature can be disabled.

Configuration Register 1 (0xTBD)

Bit 3 BUS_TO_EN = 1; bus timeout enabled.

Bit 3 TODIS = 0; I^2C timeout disabled (default).

Virus Protection

To prevent rogue programs or viruses from accessing critical ADP4000 register settings, the lock bit can be set. Setting Bit 0 of the Lock/Reset sets the lock bit and locks critical registers. In this mode, certain registers can no longer be written to until the ADP4000 is powered down and powered up again. For more information on which registers are locked see the register map.

ON_OFF_Config Command

The I^2C interface has an ON_OFF_Config which allows the user to configure when the ADP4000 should start and stop switching. There two control inputs, the EN input (specified as per VR11.1) and the Operation Command. The user can program the ADP4000 to respond to or ignore each of the control inputs. The default configuration is the EN pin

mantissa and exponent are 2's compliment values, if the MSB are 1 then they are negative values.

IOUT_CAL_GAIN and IOUT_CAL_OFFSET

The ADP4000 measures the voltage on the Imon pin and stores that in the READ_IOUT Command (0x8C). However this register should read back Amps. Therefore the IOUT_CAL_GAIN and IOUT_CAL_OFFSET commands need to be programmed to convert the Imon voltage into current in Amps. The following equation is used:

$$\text{READ\_IOUT} = \left(I_{MON}\ \text{Voltage} \times \text{IOUT\_CAL\_GAIN}\right) + \text{IOUT\_CAL\_OFFSET} \quad \text{(eq. 19)}$$

The IOUT_CAL_GAIN defaults to 1 and IOUT_CAL_OFFSET defaults to 0 which means the Imon voltage is stored in the READ_IOUT Command.

VR11 VID CODES for the ADP4000

OUTPUT	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
1.32500	0	0	1	0	1	1	1	0
1.31875	0	0	1	0	1	1	1	1
1.31250	0	0	1	1	0	0	0	0
1.30625	0	0	1	1	0	0	0	1
1.30000	0	0	1	1	0	0	1	0
1.29375	0	0	1	1	0	0	1	1
1.28750	0	0	1	1	0	1	0	0
1.28125	0	0	1	1	0	1	0	1
1.27500	0	0	1	1	0	1	1	0
1.26875	0	0	1	1	0	1	1	1
1.26250	0	0	1	1	1	0	0	0
1.25625	0	0	1	1	1	0	0	1
1.25000	0	0	1	1	1	0	1	0
1.24375	0	0	1	1	1	0	1	1
1.23750	0	0	1	1	1	1	0	0
1.23125	0	0	1	1	1	1	0	1
1.22500	0	0	1	1	1	1	1	0
1.21875	0	0	1	1	1	1	1	1
1.21250	0	1	0	0	0	0	0	0
1.20625	0	1	0	0	0	0	0	1
1.20000	0	1	0	0	0	0	1	0
1.19375	0	1	0	0	0	0	1	1
1.18750	0	1	0	0	0	1	0	0
1.18125	0	1	0	0	0	1	0	1
1.17500	0	1	0	0	0	1	1	0
1.16875	0	1	0	0	0	1	1	1
1.16250	0	1	0	0	1	0	0	0
1.15625	0	1	0	0	1	0	0	1
1.15000	0	1	0	0	1	0	1	0
1.14375	0	1	0	0	1	0	1	1
1.13750	0	1	0	0	1	1	0	0
1.13125	0	1	0	0	1	1	0	1
1.12500	0	1	0	0	1	1	1	0
1.11875	0	1	0	0	1	1	1	1
1.11250	0	1	0	1	0	0	0	0
1.10625	0	1	0	1	0	0	0	1
1.10000	0	1	0	1	0	0	1	0
1.09375	0	1	0	1	0	0	1	1
1.08750	0	1	0	1	0	1	0	0
1.08125	0	1	0	1	0	1	0	1
1.07500	0	1	0	1	0	1	1	0
1.06875	0	1	0	1	0	1	1	1
1.06250	0	1	0	1	1	0	0	0
1.05625	0	1	0	1	1	0	0	1
1.05000	0	1	0	1	1	0	1	0
1.04375	0	1	0	1	1	0	1	1

VR11 VID CODES for the ADP4000

OUTPUT	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0

VR11 VID CODES for the ADP4000

OUTPUT	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
0.75000	1	0	0	0	1	0	1	0
0.74375	1	0	0	0	1	0	1	1
0.73750	1	0	0	0	1	1	0	0
0.73125	1	0	0	0	1	1	0	1
0.72500	1	0	0	0	1	1	1	0
0.71875	1	0	0	0	1	1	1	1
0.71250	1	0	0	1	0	0	0	0
0.70625	1	0	0	1	0	0	0	1
0.70000	1	0	0	1	0	0	1	0
0.69375	1	0	0	1	0	0	1	1
0.68750	1	0	0	1	0	1	0	0
0.68125	1	0	0	1	0	1	0	1
0.67500	1	0	0	1	0	1	1	0
0.66875	1	0	0	1	0	1	1	1
0.66250	1	0	0	1	1	0	0	0
0.65625	1	0	0	1	1	0	0	1
0.65000	1	0	0	1	1	0	1	0
0.64375	1	0	0	1	1	0	1	1
0.63750	1	0	0	1	1	1	0	0
0.63125	1	0	0	1	1	1	0	1
0.62500	1	0	0	1	1	1	1	0
0.61875	1	0	0	1	1	1	1	1
0.61250	1	0	1	0	0	0	0	0
0.60625	1	0	1	0	0	0	0	1
0.60000	1	0	1	0	0	0	1	0
0.59375	1	0	1	0	0	0	1	1
0.58750	1	0	1	0	0	1	0	0
0.58125	1	0	1	0	0	1	0	1
0.57500	1	0	1	0	0	1	1	0
0.56875	1	0	1	0	0	1	1	1
0.56250	1	0	1	0	1	0	0	0
0.55625	1	0	1	0	1	0	0	1
0.55000	1	0	1	0	1	0	1	0
0.54375	1	0	1	0	1	0	1	1
0.53750	1	0	1	0	1	1	0	0
0.53125	1	0	1	0	1	1	0	1
0.52500	1	0	1	0	1	1	1	0
0.51875	1	0	1	0	1	1	1	1
0.51250	1	0	1	1	0	0	0	0
0.50625	1	0	1	1	0	0	0	1
0.50000	1	0	1	1	0	0	1	0
OFF	1	1	1	1	1	1	1	0
OFF	1	1	1	1	1	1	1	1

Table 11. I²C Commands for the ADP4000

Cmd Code	R/W	Default	Description	# Byte	Comment
0x01	R/W	0x80	Operation	1	00xx xxxx – Immediate Off

Cmd Code	R/W	Default	Description	# Byte	Comment		
					4	1	ADP4000 has an SMBus $\overline{\text{ALERT}}$ pin and ARA is supported.
					3:0	000	Reserved
0x20	R	0x20	VOUT_MODE	1	The ADP4000 supports VID mode for programming the output voltage.		
0x21	R/W	0x00	VOUT_COMMAND	2	Sets the output voltage using VID.		
0x25	R/W	0x0020	VOUT_MARGIN_ HIGH	2	Sets the output voltage when operation command is set to Margin High. Programmed in VID Mode.		
0x26	R/W	0x00B2	VOUT_MARGIN_ LOW	2	Sets the output voltage when operation command is set to Margin Low. Programmed in VID Mode.		
0x38	R/W	0x0001	IOUT_CAL_GAIN	2	0x0064	Sets the ratio of voltage sensed to current output. Scale is Linear and is expressed in 1/□	
0x39	R/W	0x0000	IOUT_CAL_OFFSET	2	This offset is used to null out any offsets in the output current sensing circuitry. Programmed in Linear mode and units are Amps.		
0x4A	R/W	0x0064	IOUT_OC_WARN_				

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Table 12. Manufacturer Specific Command Codes for the ADP4000

Cmd Code	R/W	Default	Description	# Byte	Comment		
0xD0	R/W	0x00	Lock/Reset	1	**Bit**	**Name**	**Description**
					1	Reset	Resets all registers to their POR Value. Has no effect if Lock bit is set.
					0	Lock	Logic 1 locks all limit values to their current settings. Once this bit is set, all lockable registers become read-only and cannot be modified until the ADP4000 is powered down and powered up again. This prevents rogue programs such as viruses from modifying critical system limit settings (Lockable).
0xD1	R/W	0x07	Mfr Config	1	**Bit**	**Name**	**Description**
					7:6	$\overline{\text{PSI}}$	These bits sets the number of phases turned on during $\overline{\text{PSI}}$. 00 = 1 Phase enabled during $\overline{\text{PSI}}$ 01 = 2 Phases enabled during $\overline{\text{PSI}}$ 10 = 3 Phases enabled during $\overline{\text{PSI}}$ 11 = 1 Phase enabled during $\overline{\text{PSI}}$
					5	Reserved	Reserved
					4	Reserved	Reserved
					3	BUS_TO_EN	Bus Timeout Enable. When the BUS_TO_EN bit is set to 1, the I^2C Timeout feature is enabled. In this state if, at any point during an I^2C transaction involving the ADP4000, activity ceases for more than 35 ms, the ADP4000 assumes the bus is locked and releases the bus. This allows the ADP4000 to be used with SMBus controllers that cannot handle SMBus timeouts (Lockable).
					2	$\overline{\text{FAULT}}$_EN	Enable the $\overline{\text{FAULT}}$ pin, Default = 1
					1	$\overline{\text{ALERT}}$_EN	Enable the $\overline{\text{ALERT}}$ pin
					0	ENABLE_ MONITOR	When the ENABLE_MONITOR bit is set to 1, the ADP4000 starts conversions with the ADC and monitors the voltages and temperatures.
0xD2	R/W	0x52	VR Config 1A	1	**Bit**	**Name**	**Description**
					6:4	Phase Enable Bits	000 = Phase 1 001 = Phase 2 010 = Phase 3 011 = Phase 4 100 = Phase 5 101 = Phase 6 All other codes = Phase 6
					3	VID_EN	When the VID_EN bit is set to 1, the VID code in the VOUT_COMMAND register sets the output voltage. When VID_EN is set to 0, the output voltage follows the VID input pins.
					2	LOOP_EN	When the LOOP_EN bit is set to 1 in both registers, the control loop test function is enabled. This allows measurement of the control loop AC gain and phase response with appropriate instrumentation. The control loop signal insertion pin is IMON. The control loop output pin is COMP.

Cmd Code	R/W	Default	Description	# Byte	Comment	
					1	CLIM_EN

Cmd Code	R/W	Default	Description	# Byte	Comment
0xE0	R/W	0x00	PWRGD Hi Threshold	1	This value sets the PWRGD Hi Threshold and the CROWBAR Threshold: Code = 00, PWRGD HI = 300 mV (default) Code = 01, PWRGD HI = 250 mV Code = 10, PWRGD HI = 200 mV Code = 11, PWRGD HI = 150 mV
0xE1	R/W	0x00	PWRGD Lo Threshold	1	This value sets the PWRGD Lo Threshold: Code = 000, PWRGD Lo = -500 mV (default) Code = 001, PWRGD Lo = -450 mV Code = 010, PWRGD Lo = -400 mV Code = 011, PWRGD Lo = -350 mV Code = 100, PWRGD Lo = -300 mV Code = 101, PWRGD Lo = -250 mV Code = 110, PWRGD Lo = -200 mV Code = 111, PWRGD Lo = -150 mV
0xE2	R/W	0x10	Current Limit Threshold	1	This value sets the internal current limit adjust value. The default current limit is programmed using a resistor to ground on the LIMIT pin. The value of this register adjusts this value by a percentage between 50% and 146.7%. Each LSB represents a 3.33% change in the threshold. 11111 = 146.7% of external current limit 10000 = 100% of external current limit (default) 00000 = 50% of external current limit
0xE3	R/W	0x10	Phase Bal SW1	1	pin. Theshold.

Cmd Code	R/W	Default	Description	# Byte	Comment		
0xF6	R/W	0x0002	VMON Warn Limit	2	VMON Warn Limit.		
0xF7	R/W	0x07CE	TTSENSE Gain	2	Gain information used to convert TTSENSE Voltage to temperature.		
0xF8	R/W	0x007B	TTSENSE Offset	2	Offset information used to convert TTSENSE Voltage to temperature.		
0xF9	R/W	0x00	Mask $\overline{\text{ALERT}}$	1	**Bit**	**Name**	**Description**
					7	Mask V_{OUT}	Masks any $\overline{\text{ALERT}}$ caused by bits in Status V_{OUT} Register.
					6	Mask I_{OUT}	Masks any $\overline{\text{ALERT}}$ caused by bits in Status I_{OUT} Register.
					5	Mask Input	Masks any $\overline{\text{ALERT}}$ caused by bits in Status Input Register.
					4	Mask Temperature	Masks any $\overline{\text{ALERT}}$ caused by bits in Status Temperature Register.
					3	Mask CML	Masks any $\overline{\text{ALERT}}$ caused by bits in Status CML Register.
					2	VMON	Masks any $\overline{\text{ALERT}}$ caused by VMON exceeding its high or low limit.
					1	VSENSE2	Masks any $\overline{\text{ALERT}}$ caused by VSENSE2 exceeding its high or low limit.
					0	Mask POUT	Masks any $\overline{\text{ALERT}}$ caused by POUT exceeding its programmed limit.
0xFA	R/W	0x00	Mask $\overline{\text{FAULT}}$	1	**Bit**	**Name**	**Description**
					7	Mask V_{OUT}	Masks any $\overline{\text{FAULT}}$ caused by bits in Status V_{OUT} Register.
					6	Mask I_{OUT}	Masks any $\overline{\text{FAULT}}$ caused by bits in Status I_{OUT} Register.
					5	Mask Input	Masks any $\overline{\text{FAULT}}$ caused by bits in Status Input Register.
					4	Mask Temperature	Masks any $\overline{\text{FAULT}}$ caused by bits in Status Temperature Register.
					3	Mask CML	Masks any $\overline{\text{FAULT}}$ caused by bits in Status CML Register.
					2	VMON	Masks any $\overline{\text{FAULT}}$ caused by VMON exceeding its high or low limit.
					1	VSENSE2	Masks any $\overline{\text{FAULT}}$ caused by VSENSE2 exceeding its high or low limit.
					0	Mask POUT	Masks any $\overline{\text{FAULT}}$ caused by POUT exceeding its programmed limit.
0xFB	R/W	0x00	General Status	1	**Bit**	**Name**	**Description**
					7	$\overline{\text{FAULT}}$	
					6	$\overline{\text{ALERT}}$	
					5	POWER−GOOD	Replaced by Bit 3 of the Status Word Command.
					4	RDY	
0xFC	R	0x00	Phase Status	1	**Bit**	**Name**	**Description**
					7	Phase 6	This bit is set to 1 when Phase 6 is enabled.
					6	Phase 5	This bit is set to 1 when Phase 5 is enabled.
					5	Phase 4	This bit is set to 1 when Phase 4 is enabled.
					4	Phase 3	This bit is set to 1 when Phase 3 is enabled.
					3	Phase 2	This bit is set to 1 when Phase 2 is enabled.

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