ADP4100

Product Preview

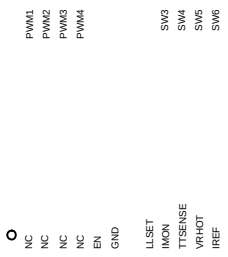

Figure 2. Application Schematic

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Range (Note 1)	V_{IN}	−0.3 to 6	V
FBRTN	V_{FBRTN}	−0.3 to + 0.3 V	

PIN ASSIGNMENT

Pin No.	Pin Name	Description
1	NC	No Connect
2	NC	No Connect
3	NC	No Connect
4	NC	No Connect
5	EN	Power Supply Enable Input. Pulling this pin to GND disables the PWM outputs and pulls the PWRGD output low.
6	GND	Ground. All internal biasing and the logic output signals of the device are referenced to this ground.
7	PSI_SET	This input sets the number of phases enabled during $\overline{\text{PSI}}$. Pulling this input high means that two phases, Phases 1 and Phase 4 (when 6 phases are enabled during normal operation), are enabled during $\overline{\text{PSI}}$. Grounding this pin means only Phase 1 is enabled during $\overline{\text{PSI}}$.
8	LLSET	Output Loadline Programming Input. This pin can be connected directly to CSCOMP or it can be connected to the centerpoint of a resistor divider between CSCOMP and CSREF. Connecting LLSET to CSREF disables the loadline.
9	IMON	Total Current Output Pin.
10	TTSENSE	VR Temperature Sense Input. An NTC thermistor between this pin and GND is used to remotely sense the temperature at the desired thermal monitoring point.
11	VRHOT	VR HOT Output. Open drain output that signals when the temperature at the monitoring point connected to TTSENSE exceeds the VRHOT temperature threshold.
12	IREF	Current Reference Input. An external resistor from this pin to ground sets the reference current for I_{FB}, IILIMFS, and ITH(X).
13	RT	Frequency Setting Resistor Input. An external resistor connected between this pin and GND sets the oscillator frequency of the device.
14	RAMPADJ	PWM Ramp Current Input. An external resistor from the converter input voltage to this pin sets the internal PWM ramp.
15	TRDET	Transient Detect. This output is asserted low whenever a load release is detected
16	FBRTN	Feedback Return. VID DAC and error amplifier reference for remote sensing of the output voltage.
17	COMP	Error Amplifier Output and Compensation Point.
18	FB	Feedback Input. Error amplifier input for remote sensing of the output voltage. An external resistor between this pin and the output voltage sets the no load offset point.
19	CSREF	Current Sense Reference Voltage Input. The voltage on this pin is used as the reference for the current sense amplifier and the power−good and crowbar functions. This pin should be connected to the common point of the output inductors.
20	CSSUM	Current Sense Summing Node. External resistors from each switch node to this pin sum the average inductor currents together to measure the total output current.
21	CSCOMP	Current Sense Compensation Point. A resistor and capacitor from this pin to CSSUM determines the gain of the current sense amplifier and the positioning loop response time.
22	ILIMFS	Current Sense and Limit Scaling Pin. An external resistor from this pin to CSCOMP sets the internal current sensing signal for current−limit and IMON.
23	$\overline{\text{ODN}}$	Output Disable Logic Output for $\overline{\text{PSI}}$ operation. This pin is actively pulled low when $\overline{\text{PSI}}$ is low, otherwise it functions in the same way as $\overline{\text{OD1}}$.
24	$\overline{\text{OD1}}$	Output Disable Logic Output. This pin is actively pulled low when the EN input is low or when V_{CC} is below its UVLO threshold to signal to the Driver IC that the driver high−side and low−side outputs should go low.
25 to 30	SW6 to SW1	Current Balance Inputs. Inputs for measuring the current level in each phase. The SW pins of unused phases should be left open.
31 to 36	PWM6 to PWM1	Logic−Level PWM Outputs. Each output is connected to the input of an external MOSFET driver such as the ADP3121. Connecting PWM6 to V_{CC} disables PWM6, connecting PWM5 to V_{CC} disables PWM5 and PWM6, etc. This means the ADP4100 can be setup to operate as a 1− 2−, 3−, 4−, 5−, or 6−phase controller.
37	V_{CC}	Supply Voltage for the Device. A 340 Ω resistor should be placed between the 12 V system supply and the V_{CC} pin. The internal shunt regulator maintains V_{CC} = 5.0 V.
38 to 45	VID7 to VID0	Voltage Identification DAC Inputs. These eight pins are pulled down to GND, providing a logic zero if left open. When in normal operation mode, the DAC output programs the FB regulation voltage from 0.375 V to 1.6 V.
46	$\overline{\text{PSI}}$	Power State Indicator. Pulling this pin low places the controller in lower power state operation.
47	PWRGD	Power−Good Output. Open−drain output that signals when the output voltage is outside of the proper operating range.
48	VCC3	3.3 V Power Supply Output. A capacitor from this pin to ground provided decoupling for the interval 3.3V LDO.

ELECTRICAL CHARACTERISTICS

V_{in} = (5.0 V) FBRTN − GND, for typical values T_A = 25°C, for min/max values T_A = 0°C to 85°C; unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Reference Current						
Reference Bias Voltage		V_{IREF}	1.75	1.8	1.85	V
Reference Bias Current	R_{IREF} = 121 kΩ	I_{IREF}		15		μA
Error Amplifier						
Output Voltage Range (Note 6)		V_{COMP}	0		4.4	V
Accuracy	Relative to nominal DAC output, referenced to FBRTN (see Figure 4)	V_{FB}	7		7	mV
	In startup	$V_{FB(BOOT)}$	1.093	1.1	1.107	V
Load Line Positioning Accuracy			−77	−80	−83	mV
LLSET Input Voltage Range			−250		250	

Unit
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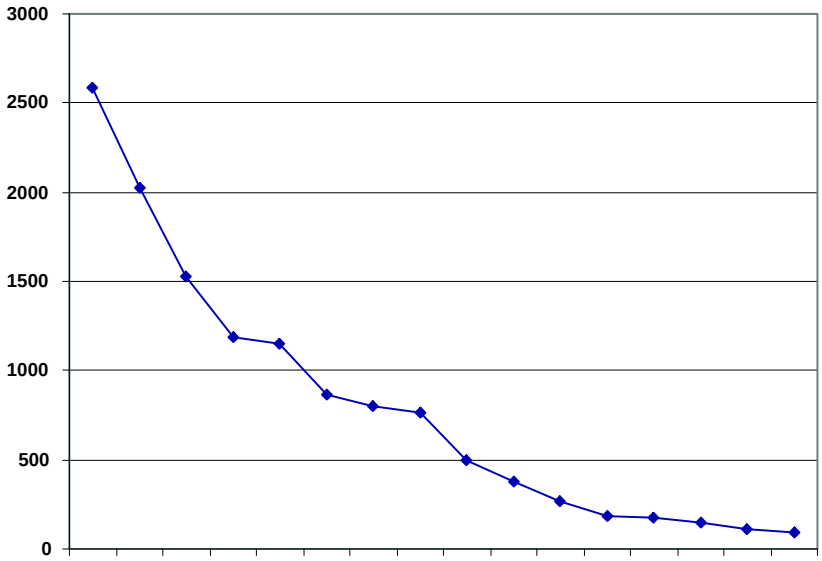
4.7

TYPICAL CHARACTERISTICS



TEST CIRCUITS

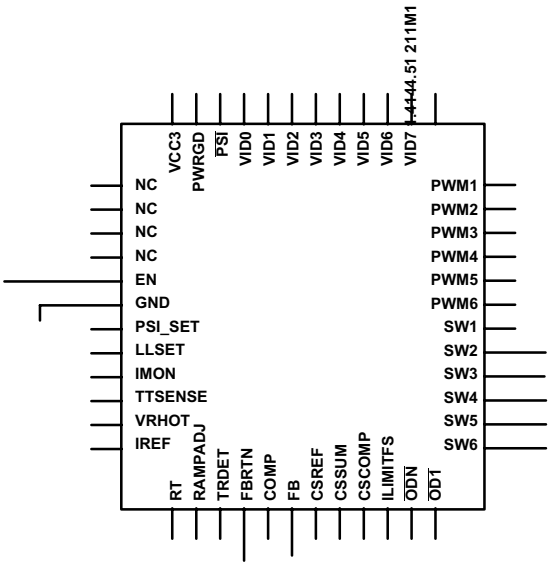


Figure 4. Closed−Loop Output Voltage Accuracy

through a resistor, R_B, to the regulation point, usually the remote sense pin of the microprocessor. FBRTN is connected directly to the remote sense ground point. The internal VID DAC and precision reference are referenced to FBRTN, which has a minimal current of 100 μA to allow accurate remote sensing. The internal error amplifier compares the output of the DAC to the FB pin to regulate the output voltage.

Output Current Sensing

The ADP4100 provides a dedicated Current−Sense Amplifier (CSA) to monitor the total output current for proper voltage positioning vs. load current, for the IMON output and for current−limit detection. Sensing the load current at the output gives the total real time current being delivered to the load, which is an inherently more accurate method than peak current detection or sampling the current across a sense element such as the low−side MOSFET. This amplifier can be configured several ways, depending on the objectives of the system, as follows:

- Output inductor DCR sensing without a thermistor for lowest cost.
- Output inductor DCR sensing with a thermistor for improved accuracy with tracking of inductor temperature.
- Sense resistors for highest accuracy measurements.

The positive input of the CSA is connected to the CSREF pin, which is connected to the average output voltage. The inputs to the amplifier are summed together through resistors from the sensing element, such as the switch node side of the output inductors, to the inverting input CSSUM. The feedback resistor between CSCOMP and CSSUM sets the gain of the amplifier and a filter capacitor is placed in parallel with this resistor. The gain of the amplifier is programmable by adjusting the feedback resistor. This difference signal is used internally to offset the VID DAC for voltage positioning.

The difference between CSREF and CSCOMP is used as a differential input for the current−limit comparator.

To provide the best accuracy for sensing current, the CSA is designed to have a low offset input voltage. Also, the sensing gain is determined by external resistors to make it extremely accurate.

Current−Limit Setpoint

The current limit threshold on the ADP4100 is programmed by a resistor between the I_{LIMFS} pin and the CSCOMP pin. The I_{LIMFS} current, I_{ILIMFS}, is compared with an internal current reference of 22 μA. If I_{ILIMFS} exceeds 22 μA then the output current has exceeded the limit and the current limit protection is tripped.

$$I_{ILIMFS} = \frac{V_{ILIMFS} - V_{CSCOMP}}{R_{ILIMFS}} \quad \text{(eq. 2)}$$

Where: $V_{ILIMFS} = V_{CSREF}$

$$I_{ILIMFS} = \frac{V_{CSREF} - V_{CSCOMP}}{R_{ILIMFS}} \quad \text{(eq. 3)}$$

$$V_{CSREF} - V_{CSCOMP} = \frac{R_{CS}}{R_{PH}} \times R_L \times I_{LOAD}$$

Where: R_L = DCR of the Inductor

Assuming that:

$$\frac{R_{CS}}{R_{PH}} \times R_L = 1\ m\Omega \quad \text{(eq. 4)}$$

i.e. the external circuit is set up for a 1 mΩ Loadline then the R_{ILIMFS} is calculated as follows:

$$I_{ILIMFS} = \frac{1\ m\Omega \times I_{LOAD}}{R_{LIMITS}} \quad \text{(eq. 5)}$$

Assuming we want a current limit of 150 A that means that I_{LIMFS} must equal 22 μA at that load.

$$22\ \mu A = \frac{1\ m\Omega \times 150\ A}{R_{LIMITFS}} \quad \text{(eq. 6)}$$

Solving this equation for $R_{LIMITFS}$

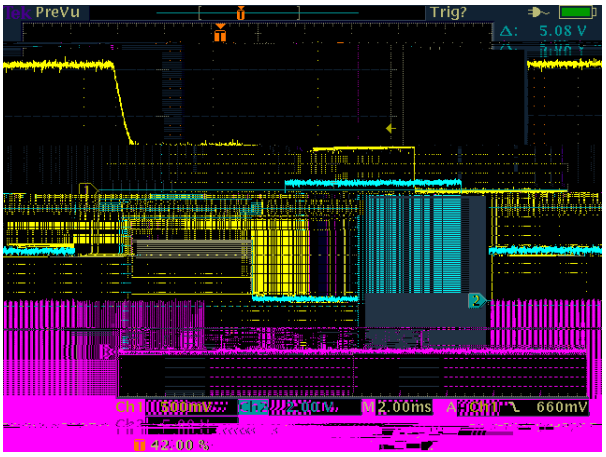


Figure 9. Overcurrent Latchoff Waveforms Channel 1: CSREF, Channel 2: COMP, Channel 3: PWM1

An inherent per phase current limit protects individual phases if one or more phases stops functioning because of a faulty component. This limit is based on the maximum normal mode COMP voltage.

Output Current Monitor

IMON is an analog output from the ADP4100 representing the total current being delivered to the load. It outputs an accurate current that is directly proportional to the current set by the ILIMFS resistor.

$$I_{IMON} = 10 \times I_{SW} \times I_{LIMFS} \quad \text{(eq. 7)}$$

The current is then run through a parallel RC connected from the I_{MON} pin to the FBRTN pin to generate an accurately scaled and filtered voltage as per the VR11.1 specification. The size of the resistor is used to set the I_{MON} scaling.

The scaling is set such that I_{MON} = 900 mV at the TDC current of the processor. This means that the RIMON resistor should be chosen as follows.

From the Current−Limit Setpoint paragraph we know the following:

$$I_{ILIMFS} = \frac{1\ m\Omega \times I_{LOAD}}{R_{LIMFS}} \quad \text{(eq. 8)}$$

$$I_{IMON} = 10 \times \frac{1\ m\Omega \times I_{LOAD}}{R_{LIMFS}}$$

For a 150 A current limit R_{LIMFS} = 6.81 kΩ. Assuming the TDC = 135 A then V_{MON} should equal 900 mV when I_{LOAD} = 135 A.

When I_{LOAD} = 135 A, I_{MON} equals:

I

(eq. 9)

This ramp voltage should be set to at least 0.5 V for noise immunity reasons. If it is less than 0.5 V then decrease the ramp resistor.

Dynamic VID

The ADP4100 has the ability to respond to dynamically changing VID inputs while the controller is running. This allows the output voltage to change while the supply is running

$\overline{\text{PSI}}$ Set Table

# of Phases Normally	$\overline{\text{PSI}}$ Set	Phases on During $\overline{\text{PSI}}$
6	High Low	Phase 1 and 4 Phase 1
5	High Low	Phase 1 and 4 Phase 1
4	High Low	Phase 1 and 3 Phase 1
3	High Low	Phase 1 Phase 1
2	High Low	Phase 1 Phase 1
1	High Low	Phase 1 Phase 1

Output Crowbar

As part of the protection for the load and output components of the supply, the PWM outputs are driven low (turning on the low−side MOSFETs) when the output voltage exceeds the upper crowbar threshold. This crowbar action stops once the output voltage falls below the release threshold of approximately 300 mV.

The value for the crowbar limit follows the PWRGD high limit.

Turning on the low−side MOSFETs pulls down the output as the reverse current builds up in the inductors. If the output overvoltage is due to a short in the high−5(enen 4(EN wbalesse)a(dueirc.spv Tcve(the uppers, iu)ws t Ifr2 re 539.4m0 g09.3(wbadis Twr crow

The maximum power dissipated is calculated using Equation 21.

$$P_{MAX} = \frac{\left(V_{IN(MAX)} - V_{CC(MIN)}\right)^2}{R_{SHUNT}} \quad \text{(eq. 21)}$$

where:

$V_{IN(MAX)}$ is the maximum voltage from the 12 V input supply (if the 12 V input supply is 12 V ± 5%, $V_{IN(MAX)}$ = 12.6 V; if the 12 V input supply is 12 V ±

VR11 VID CODES for the ADP4100

OUTPUT	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0

VR11 VID CODES for the ADP4100

OUTPUT	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
0.75000	1	0	0	0	1	0	1	0
0.74375	1	0	0	0	1	0	1	1
0.73750	1	0	0	0	1	1	0	0
0.73125	1	0	0	0	1	1	0	1
0.72500	1	0	0	0	1	1	1	0
0.71875	1	0	0	0	1	1	1	1
0.71250	1	0	0	1	0	0	0	0
0.70625	1	0	0	1	0	0	0	1
0.70000	1	0	0	1	0	0	1	0
0.69375	1	0	0	1	0	0	1	1
0.68750	1	0	0	1	0	1	0	0
0.68125	1	0	0	1	0	1	0	1

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