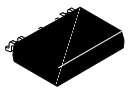
Remote Thermal Monitor and Fan Controller

ADT7460



QSOP−16
CASE 492

PIN ASSIGNMENT

The ADT7460 controller is a thermal monitor and multiple PWM fan controller for noise-sensitive applications requiring active system cooling. It can monitor the temperature of up to two remote sensor diodes plus its own internal temperature. It can measure and control the speed of up to four fans so that they operate at the lowest possible speed for minimum acoustic noise. The automatic fan speed control loop optimizes fan speed for a given temperature. A unique dynamic T_{MIN} control mode enables the system thermals/acoustics to be intelligently managed. The effectiveness of the system's thermal solution can be monitored using the $\overline{\text{THERM}}$ input. The ADT7460 also provides critical thermal protection to the system by using the bidirectional $\overline{\text{THERM}}$ pin as an output to prevent system or component overheating.

Features

- Controls and Monitors Up to 4 Fans
- 1 On-chip and 2 Remote Temperature Sensors
- Dynamic T_{MIN} Control Mode Optimizes System Acoustics Intelligently
- Automatic Fan Speed Control Mode Controls System Cooling Based on Measured Temperature
- Enhanced Acoustic Mode Dramatically Reduces User Perception of Changing Fan Speeds
- Thermal Protection Feature via $\overline{\text{THERM}}$ Output
- Monitors Performance Impact of Intel® Pentium® 4 Processor
- Processor Thermal Control Circuit via $\overline{\text{THERM}}$ Input
- 2-wire and 3-wire Fan Speed Measurement
- Limit Comparison of All Monitored Values
- This is a Pb-Free Device

Applications

- Low Acoustic Noise PCs
- Networking and Telecommunications Equipment

MARKING DIAGRAM

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 46 of this data sheet.

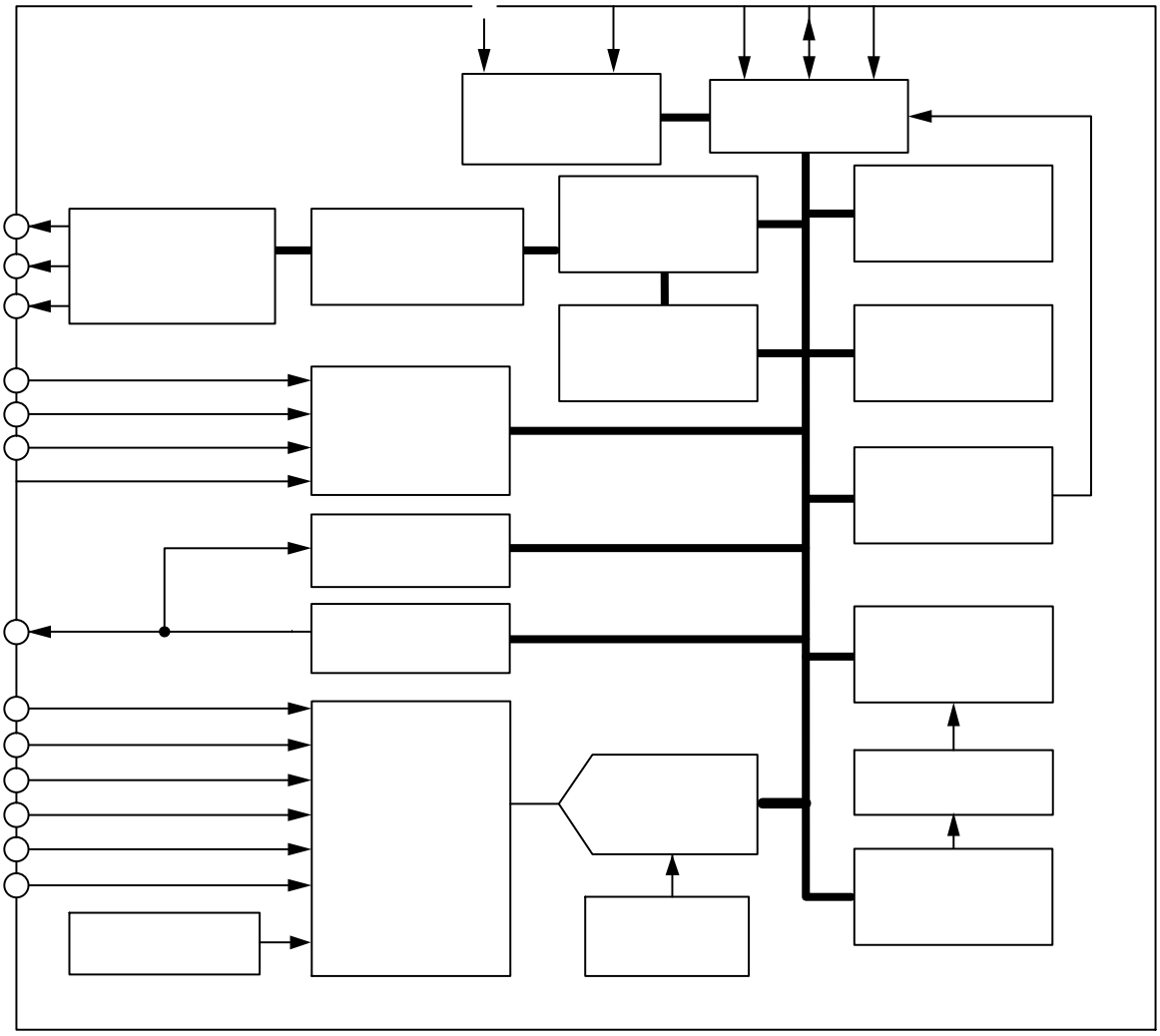


Figure 1. Functional Block Diagram

	θ_{JA}	θ_{JC}	Unit
	150	39	°C/W

oard for surface-mount packages.

scription
ck input. Requires SMBus pullup.
ndby if monitoring in low power states is required. ADT7460 can also be powered from a 5.0 V er 1 (Reg. 0x40) rescales the V_{CC} input attenuators
nput to measure speed of Fan 3. Can be easure the speed of 2-wire fans.
2 typical pullup. Pulse-width modulated output to
e reconfigured as an $\overline{\text{SMBALERT}}$ interrupt output
nput to measure speed of Fan 1. Can be easure the speed of 2-wire fans.
nput to measure speed of Fan 2. Can be easure the speed of 2-wire fans.
ated output to control Fan 3/4 speed. Requires
T7460 into address select mode, and the state of ess.
nput to measure speed of Fan 4. Can be easure the speed of 2-wire fans.
s the SMBus device address.

s a bidirectional $\overline{\text{THERM}}$ pin. Can be used to time . For example, can be connected to the

Table 4. ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted.)

Parameter (Note 1)	**Test Conditions/Comments**	**Min**	**Typ** (Note 2)	**Max**	**Unit**
POWER SUPPLY					
Supply Voltage		3.0	5.0	5.5	V
Supply Current, I_{CC}	Interface Inactive, ADC Active Standby Mode	− −	− −	3.0 20	mA μA
TEMPERATURE-TO-DIGITAL CONVERTER					
Local Sensor Accuracy	0°C ≤ T_A ≤ 70°C −40°C ≤ T_A ≤ +120°C	− −	− −	±1.5 ±3.0	°C
Resolution		−	0.25	−	°C
Remote Diode Sensor Accuracy	0°C ≤ T_A ≤ 70°C; 0°C ≤ T_D ≤ 120°C 0°C ≤ T_A ≤ 105°C; 0°C ≤ T_D ≤ 120°C 0°C ≤ T_A ≤ 120°C; 0°C ≤ T_D ≤ 120°C	− − −	− − −	±1.5 ±2.5 ±3.0	°C
Resolution		−	0.25	−	°C
Remote Sensor Source Current	High Level Low Level	− −	180 11	− −	μA
ANALOG-TO-DIGITAL CONVERTER (INCLUDING MUX AND ATTENUATORS)					
Total Unadjusted Error, TUE		−	−	±1.5	%
Differential Non-linearity, DNL	8 Bits	−	−	±1.0	LSB
Power Supply Sensitivity		−	±0.1	−	%/V
Conversion Time (Voltage Input)	Averaging Enabled	−	11.38	13	ms
Conversion Time (Local Temperature)	Averaging Enabled	−	12.09	13.50	ms
Conversion Time (Remote Temperature)	Averaging Enabled	−	25.59	28	ms
Total Monitoring Cycle Time	Averaging Enabled (Incl. Delay) (Note 3) Averaging Disabled	− −	120.17 13.51	134.50 15	ms
Input Resistance		80	140	200	kΩ
FAN RPM-TO-DIGITAL CONVERTER					
Accuracy	0°C ≤ T_A ≤ 70°C 0°C ≤ T_A ≤ 105°C −40°C ≤ T_A ≤ +120°C	− − −	− − −	±7 ±11 ±13	%
Full-scale Count		−	−	65,535	
Nominal Input RPM	Fan Count = 0xBFFF Fan Count = 0x3FFF Fan Count = 0x0438 Fan Count = 0x021C	− − − −	109 329 5000 10000	− − − −	RPM
Internal Clock Frequency		82.8	90.0	97.2	kTm(65,535)TjET468.51

Table 4. ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted.)

Parameter (Note 1)	**Test Conditions/Comments**	**Min**	**Typ** (Note 2)	**Max**	**Unit**
DIGITAL INPUT LOGIC LEVELS (TACH INPUTS)					
Hysteresis		–	0.5		

ADT7460

TYPICAL PERFORMANCE CHARACTERISTICS (CONT'D)

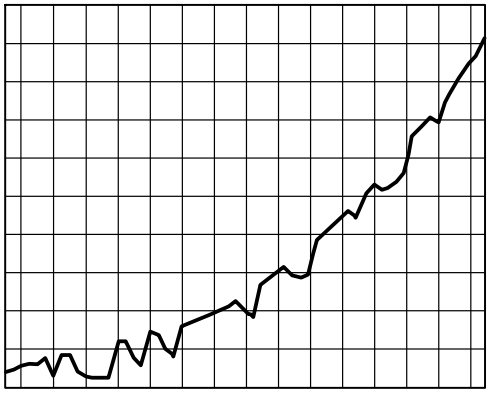


Figure 9. Supply Current vs. Supply Voltage

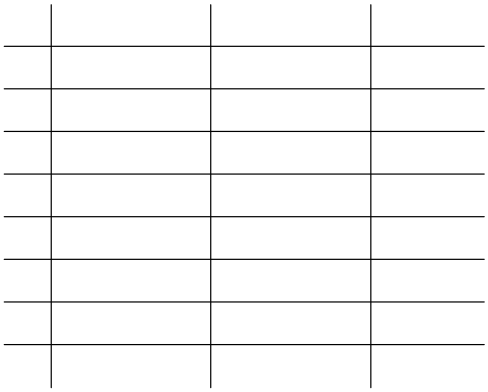


Figure 10. Remote Temperature Error vs. Differential-Mode Noise Frequency

Figure 11. Remote Temperature Error vs. Common-Mode Noise Frequency

Product Description

The ADT7460 is a thermal monitor and multiple fan controller for any system requiring monitoring and cooling. The device communicates with the system via a serial System Management Bus (SMBus). The serial bus controller has an optional address line for device selection (Pin 9), a serial data line for reading and writing addresses and data (Pin 16), and an input line for the serial clock (Pin 1). All control and programming functions of the ADT7460 are performed over the serial bus. In addition, two of the pins can be reconfigured as an $\overline{\text{SMBALERT}}$ output to indicate out-of-limit conditions.

Measurement Inputs

The device has three measurement inputs, one for voltage and two for temperature. It can also measure its own supply voltage and can measure ambient temperature with its on-chip temperature sensor.

Pin 14 is an analog input with an on-chip attenuator and is configured to monitor 2.5 V.

Power is supplied to the chip via Pin 3, and the system also monitors V_{CC} through this pin. In PCs, this pin is normally connected to a 3.3 V standby supply. This pin can, however, be connected to a 5.0 V supply and monitor it without over-ranging.

Remote temperature sensing is provided by the D1± and D2± inputs, to which diode-connected, external temperature-sensing transistors, such as a 2N3904 or CPU thermal diode, may be connected.

The ADC also accepts input from an on-chip band gap temperature sensor, which monitors system ambient temperature.

Sequential Measurement

When the ADT7460 monitoring sequence is started, it cycles sequentially through the measurement of 2.5 V input

ADT7460

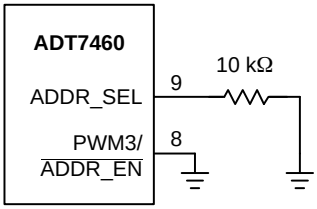


Figure 14. SMBus Address 0x2C (Pin 9 = 0)

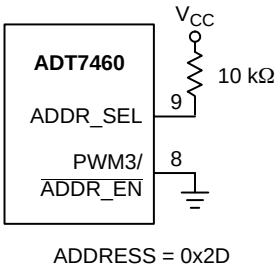


Figure 15. SMBus Address 0x2D (Pin 9 = 1)

UNCONNECTED. CAN
CAUSE UNPREDICTABLE
ADDRESSES

NOTE THAT IF THE ADT7460 IS PLACED INTO ADDRESS

Figure 16. Unpredictable SMBus Address if Pin 8 is Unconnected

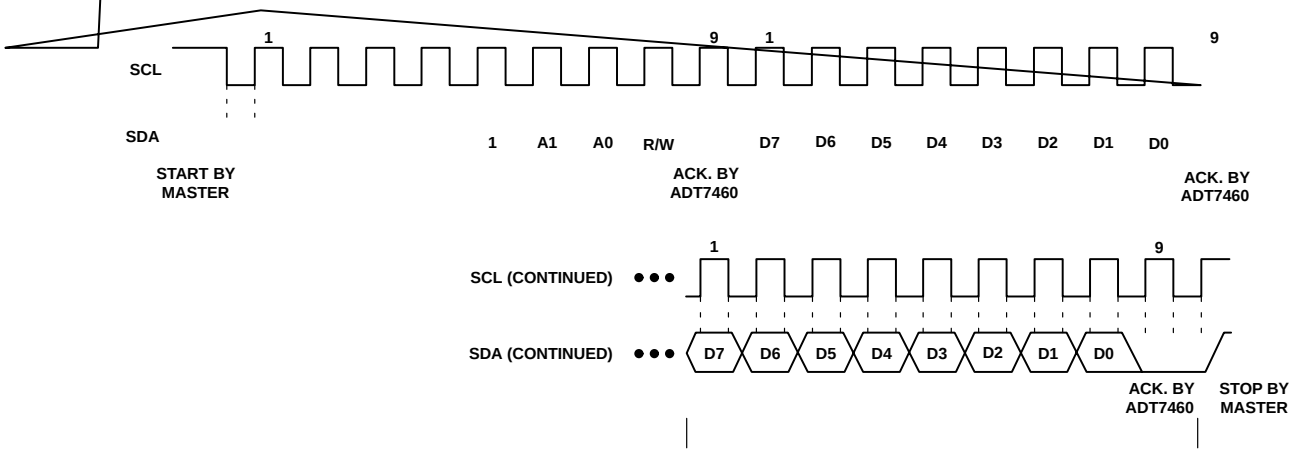


Figure 17. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

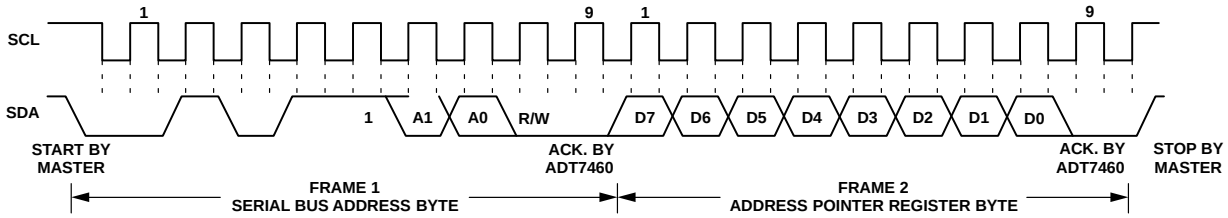


Figure 18. Writing to the Address Pointer Register Only

Table 10. 10-BIT A/D OUTPUT CODE VS. V_{IN}

Input Voltage		ADC Output
5 V_{IN}	V_{CC}	

applications. The input range of the ADC without the attenuators is 0 V to 2.25 V.

Single-channel ADC Conversion

Setting Bit 6 of Configuration Register 2 (Reg. 0x73) places the ADT7460 into single-channel ADC conversion mode. In this mode, the ADT7460 can be made to read a single voltage channel only. If the internal ADT7460 clock is used, the selected input is read every 711 μs. The appropriate ADC channel is selected by writing to Bits <7:5> of the TACH1 Minimum High Byte register (Reg. 0x55).

Table 11. CONFIGURATION REGISTER 2 (REG. 0X73)

Bit	Description
<4>	1: Averaging Off
<5>	1: Bypass Input Attenuators
<6>	1: Single-channel Convert Mode

Table 12. TACH1 MINIMUM HIGH BYTE (REG. 0X55)

Bit	Description

to a chopper stabilized amplifier that performs the functions of amplification and rectification of the waveform to produce a dc voltage proportional to ΔV_{BE}. This voltage is measured by the ADC to give a temperature output in 10-bit, twos complement format. To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles. A remote temperature measurement takes nominally 25.5 ms. The results of remote temperature measurements are stored in 10-bit, twos complement format, as illustrated in Table 13. The extra resolution for the temperature measurements is held in the Extended Resolution Register 2 (Reg. 0x77). This gives temperature readings with a resolution of 0.25°C.

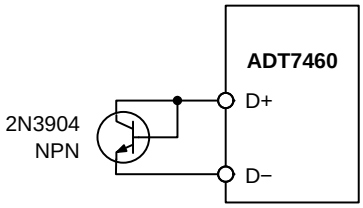


Figure 25. Measuring Temperature by Using an NPN Transistor

Figure 26. Measuring Temperature by Using a PNP Transistor

Table 16. TEMPERATURE OFFSET REGISTERS

Register	Description	Default
0x70	Remote 1 Temperature Offset	0x00 (0°C)
0x71	Local Temperature Offset	0x00 (0°C)
0x72	Remote 2 Temperature Offset	0x00 (0°C)

Temperature Measurement Limit Registers

Associated with each temperature measurement channel are high and low limit registers. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate $\overline{\text{SMBALERT}}$ interrupts.

Table 17. TEMPERATURE MEASUREMENT LIMIT REGISTERS

Register	Description	Default
0x4E	Remote 1 Temperature Low Limit	0x81
0x4F	Remote 1 Temperature High Limit	0x7F
0x50	Local Temperature Low Limit	0x81
0x51	Local Temperature High Limit	0x7F
0x52	Remote 2 Temperature Low Limit	0x81
0x53	Remote 2 Temperature High Limit	0x7F

0x7FR

Table 21. TEMPERATURE LIMIT REGISTERS

Register	Description	Default
0x4E	Remote 1 Temperature Low Limit	0x81
0x4F	Remote 1 Temperature High Limit	0x7F
0x6A	Remote 1 $\overline{\text{THERM}}$ Limit	0x64
0x50	Local Temperature Low Limit	0x81
0x51	Local Temperature High Limit	0x7F
0x6B	Local $\overline{\text{THERM}}$ Limit	0x64
0x52	Remote 2 Temperature Low Limit	0x81
0x53	Remote 2 Temperature High Limit	0x7F
0x6C	Remote 2 $\overline{\text{THERM}}$ Limit	0x64

Table 22. $\overline{\text{THERM}}$ TIMER LIMIT REGISTERS

Register	Description	Default
0x7A	THERM	

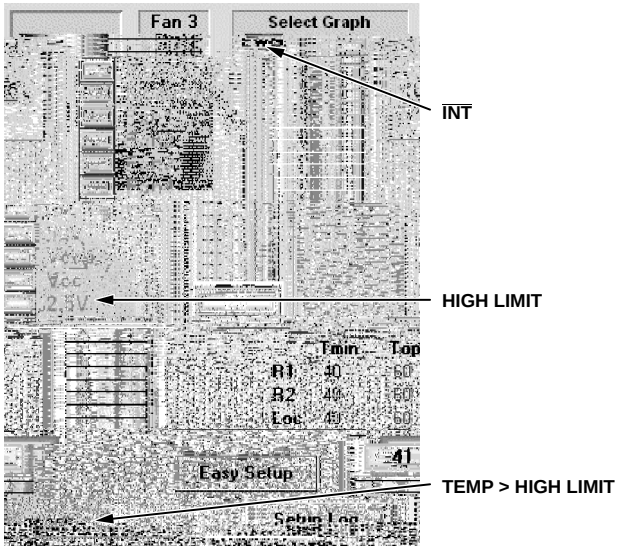


Figure 31. Temperature > High Limit: $\overline{\text{INT}}$ Occurs

Analog Monitoring Cycle Time

The analog monitoring cycle begins when a 1 is written to the start bit (Bit 0) of Configuration Register 1 (Reg. 0x40). The ADC measures each analog input in turn and, as each measurement is completed, the result is automatically stored in the appropriate value register. This round-robin monitoring cycle continues unless disabled by writing a 0 to Bit 0 of Configuration Register 1.

As the ADC is normally allowed to free-run in this manner,

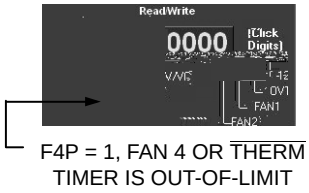


Figure 33. Status Register 2

Table 25. STATUS REGISTER 2 (REG. 0X42)

Bit	Mnemonic	Description
7	D2	

Table 26. INTERRUPT MASK REGISTER 1 (REG. 0X74)

Bit	Mnemonic	Description
7	OOL	1 masks $\overline{\text{SMBALERT}}$ for any alert condition flagged in Status Register 2.
6	R2T	1 masks $\overline{\text{SMBALERT}}$ for Remote 2 temperature.
5	LT	1 masks $\overline{\text{SMBALERT}}$ for local temperature.
4	R1T	1 masks $\overline{\text{SMBALERT}}$ for Remote 1 temperature.
3	−	Unused
2	VCC	1 masks $\overline{\text{SMBALERT}}$ for the V_{CC} channel.
1	−	Unused
0	2.5 V	1 masks $\overline{\text{SMBALERT}}$ for the 2.5 V channel.

Table 27. INTERRUPT MASK REGISTER 2 (REG. 0X75)

Bit	Mnemonic	Description
7	D2	1 masks $\overline{\text{SMBALERT}}$ for Diode 2 errors.
6	D1	1 masks $\overline{\text{SMBALERT}}$ for Diode 1 errors.
5	FAN4	1 masks $\overline{\text{SMBALERT}}$ for Fan 4 failure. If the TACH4 pin is being used as the $\overline{\text{THERM}}$ input, this bit masks $\overline{\text{SMBALERT}}$ for a $\overline{\text{THERM}}$ event.
4	FAN3	1 masks $\overline{\text{SMBALERT}}$ for Fan 3.
3	FAN2	1 masks $\overline{\text{SMBALERT}}$ for Fan 2.
2	FAN1	1 masks $\overline{\text{SMBALERT}}$ for Fan 1.
1	OVT	1 masks $\overline{\text{SMBALERT}}$ for overtemperature (exceeding $\overline{\text{THERM}}$ limits).
0	−	Unused

Enabling the $\overline{\text{SMBALERT}}$ Interrupt Output

The $\overline{\text{SMBALERT}}$ interrupt function is disabled by default. Pin 5 or Pin 14 can be reconfigured as an $\overline{\text{SMBALERT}}$ output to signal out-of-limit conditions.

Table 28. CONFIGURATION REGISTER 4 (REG. 0X7D)

Pin No.	Bit Setting
14	<0> AL2.5V = 1

Table 29. CONFIGURATION REGISTER 3 (REG. 0X78)

Pin No.	Bit Setting
5	<0> ALERT = 1

To Assign $\overline{\text{THERM}}$ Functionality to Pin 9

Pin 9 can be configured as the $\overline{\text{THERM}}$ pin on the ADT7460. To configure Pin 9 as the $\overline{\text{THERM}}$ pin, set the $\overline{\text{THERM}}$ ENABLE Bit (Bit 1) in Configuration Register 3 (Address 0x78) = 1.

$\overline{\text{THERM}}$ as an Input

When configured as an input, the $\overline{\text{THERM}}$ pin allows the user to time assertions on the pin. This can be useful for connecting to the $\overline{\text{PROCHOT}}$ output of a CPU to gauge system performance. For more information on timing $\overline{\text{THERM}}$ assertions and generating $\overline{\text{SMBALERT}}$s based on $\overline{\text{THERM}}$, see the Generating Interrupts from Events sections.

The user can also set up the ADT7460 so when the $\overline{\text{THERM}}$ pin is driven low externally, the fans run at 100%. The fans run at 100% while the $\overline{\text{THERM}}$ pin is pulled low.

This is done by setting the BOOST bit (Bit 2) in Configuration Register 3 (Address 0x78) to 1. This works only if the fan is already running, for example, in manual mode when the current duty cycle is above 0x00 or in automatic mode when the temperature is above T_{MIN}. If the temperature is below T_{MIN} or if the duty cycle in manual mode is set to 0x00, pulling $\overline{\text{THERM}}$ low externally has no effect. See Figure 36 for more information.

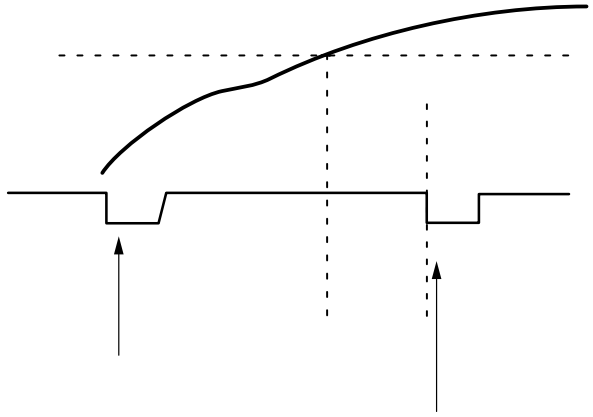


Figure 36. Asserting $\overline{\text{THERM}}$ Low as an Input in Automatic Fan Speed Control Mode

The 8-bit $\overline{\text{THERM}}$ timer register (Reg. 0x79) is designed such that Bit 0 is set to 1 on the first $\overline{\text{THERM}}$ assertion. Once the cumulative $\overline{\text{THERM}}$ assertion time exceeds 45.52 ms, Bit 1 of the $\overline{\text{THERM}}$ timer is set and Bit 0 becomes the LSB of the timer with a resolution of 22.76 ms.

Figure 37 illustrates how the $\overline{\text{THERM}}$ timer behaves as the $\overline{\text{THERM}}$ input is asserted and negated. Bit 0 is set on the first $\overline{\text{THERM}}$ assertion detected. This bit remains set until the cumulative $\overline{\text{THERM}}$ assertions exceed 45.52 ms. At this time, Bit 1 of the $\overline{\text{THERM}}$ timer is set, and Bit 0 is cleared. Bit 0 now reflects timer readings with a resolution of 22.76 ms.

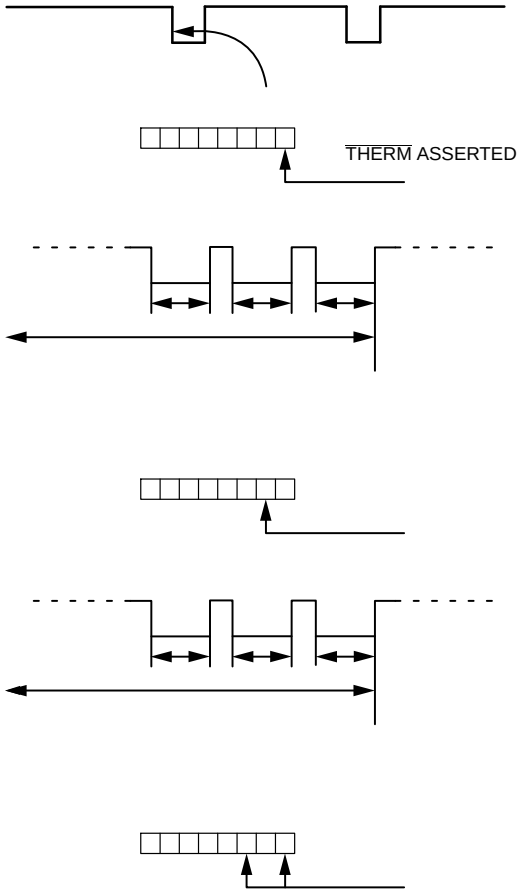


Figure 37. Understanding the $\overline{\text{THERM}}$ Timer

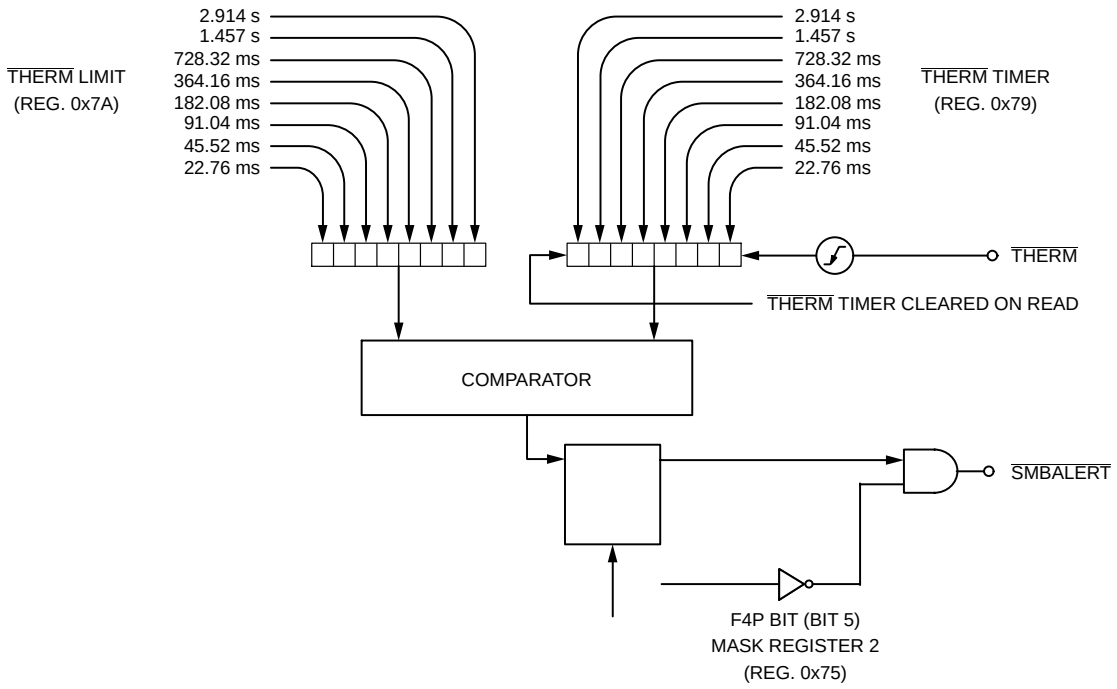


Figure 38. Functional Diagram of the ADT7460 THERM Monitoring Circuitry

shows how the $\overline{\text{THERM}}$ pin asserts low as an output in the event of a critical overtemperature.

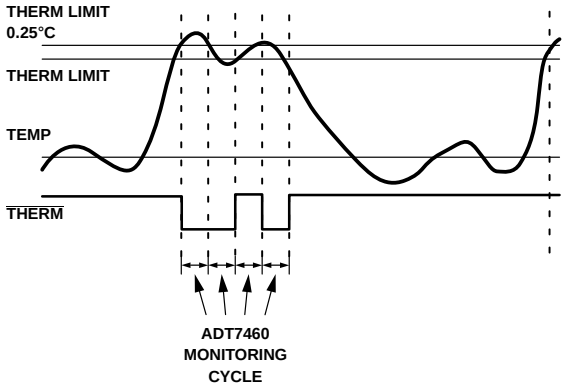


Figure 39. Asserting $\overline{\text{THERM}}$ as an Output, Based on Tripping $\overline{\text{THERM}}$ Limits

Fan Speed Measurement

The fan counter does not count the fan TACH output pulses directly because the fan speed may be less than 1000 RPM. It would take several seconds to accumulate a reasonably large and accurate count. Instead, the period of the fan revolution is measured by gating an on-chip 90 kHz oscillator into the input of a 16-bit counter for N periods of the fan TACH output (Figure 51). The accumulated count is actually proportional to the fan tachometer period and inversely proportional to the fan speed.

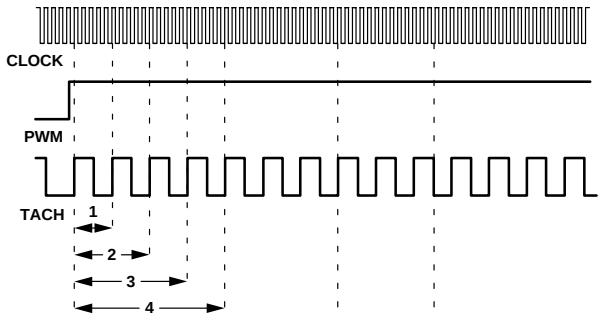


Figure 51. Fan Speed Measurement

N, the number of pulses counted, is determined by the settings of Register 0x7B (fan pulses per revolution register). This register contains two bits for each fan, allowing one, two (default), three, or four TACH pulses to be counted.

The fan tachometer readings are 16-bit values consisting of a 2-byte read from the ADT7460.

Table 31. FAN SPEED MEASUREMENT REGISTERS

Register	Description	Default
0x28	TACH1 Low Byte	0x00
0x29	TACH1 High Byte	0x00
0x2A	TACH2 Low Byte	0x00

Table 39. PWM1 TO PWM3 FREQUENCY REGISTERS (REG. 0X5F TO 0X61)

Bit	Mnemonic	Description
<2:0>	FREQ	000 = 11.0 Hz 001 = 14.7 Hz 010 = 22.1 Hz 011 = 29.4 Hz

Operating from 3.3 V Standby

The ADT7460 has been specifically designed to operate from a 3.3 V STBY supply. In computers that support S3 and S5 states, the core voltage of the processor is lowered in these states. If using the dynamic TMIN mode, lowering the core voltage of the processor would change the CPU temperature and change the dynamics of the system under dynamic TMIN control. Likewise, when monitoring $\overline{\text{THERM}}$, the $\overline{\text{THERM}}$ timer should be disabled during these states.

XNOR Tree Test Mode

The ADT7460 includes an XNOR tree test mode. This mode is useful for in-circuit test equipment at board-level testing. By applying stimulus to the pins included in the XNOR tree, it is possible to detect opens or shorts on the system board. Figure 53 shows the signals that are exercised in the XNOR tree test mode.

The XNOR tree test is invoked by setting Bit 0 (XEN) of the XNOR tree test enable register (Reg. 0x6F).

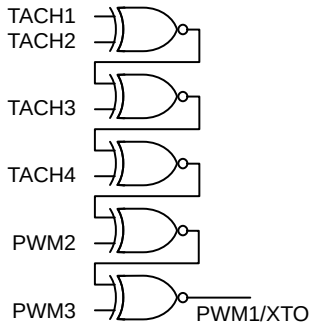


Figure 53. XNOR Tree Test

Table 42. ADT7460 REGISTERS

Addr	R/W	Desc	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	Lock-able
0x6A	R/W	Remote1 $\overline{\text{THERM}}$ Limit	7	6	5	4	3	2	1	0	0x64	YES
0x6B	R/W	Local $\overline{\text{THERM}}$ Limit	7	6	5	4	3	2	1	0	0x64	YES
0x6C												

Table 45. FAN TACHOMETER READING REGISTERS (POWER-ON DEFAULT = 0X00) (Note 1)

Register Address	R/W	Description
0x28	Read-only	TACH1 Low Byte
0x29	Read-only	TACH1 High Byte
0x2A	Read-only	TACH2 Low Byte
0x2B	Read-only	TACH2 High Byte
0x2C		

Table 48. REGISTER 0X36 − DYNAMIC T_{MIN} CONTROL REGISTER 1 (POWER-ON DEFAULT = 0X00) (Note 1)

Bit No.	Mnemonic	R/W	Description
<0>	CYR2	R/W	MSB of 3-bit Remote 2 Cycle Value. The other two bits of the code reside in Dynamic T_{MIN} Control Register 2 (Reg. 0x37). These three bits define the delay time between making subsequent T_{MIN} adjustments in the control loop, in terms of number of monitoring cycles. The system has associated thermal time constants that need to be found to optimize the response of fans and the control loop.
<1>	Reserved	Read-only	Reserved for future use.
<2>	PHTR1	R/W	PHTR1 = 1 copies the Remote 1 current temperature to the Remote 1 operating point register if $\overline{\text{THERM}}$ is asserted. The operating point contains the temperature at which $\overline{\text{THERM}}$ is

Table 49. REGISTER 0X37 − DYNAMIC T_{MIN} CONTROL REGISTER 2 (POWER-ON DEFAULT = 0X00) (Note 1)

Bit No.	Mnemonic	R/W	Description		
<2:0>	CYR1	R/W	3-bit Remote 1 Cycle Value. These three bits define the delay time between making subsequent T_{MIN} adjustments in the control loop for the Remote 1 channel, in terms of number of monitoring cycles. The system has associated thermal time constants that need to be found to optimize the response of fans and the control loop.		
			Bits	**Decrease Cycle**	**Increase Cycle**
			000	4 Cycles (0.5 s)	8 Cycles (1 s)
			001	8 Cycles (1 s)	16 Cycles (2 s)
			010	16 Cycles (2 s)	32 Cycles (4 s)
			011	32 Cycles (4 s)	64 Cycles (8 s)
			100	64 Cycles (8 s)	128 Cycles (16 s)
			101	128 Cycles (16 s)	256 Cycles (32 s)
			110	256 Cycles (32 s)	512 Cycles (64 s)
			111	512 Cycles (64 s)	1024 Cycles (128 s)
<5:3>	CYL	R/W	3-bit Local Temperature Cycle Value. These three bits define the delay time between making subsequent T_{MIN} adjustments in the control loop for local temperature channel, in terms of number of monitoring cycles. The system has associated thermal time constants that need to be found to optimize the response of fans and the control loop.		
			Bits	**Decrease Cycle**	**Increase Cycle**
			000	4 Cycles (0.5 s)	8 Cycles (1 s)
			001	8 Cycles (1 s)	16 Cycles (2 s)
			010	16 Cycles (2 s)	32 Cycles (4 s)
			011	32 Cycles (4 s)	64 Cycles (8 s)
			100	64 Cycles (8 s)	128 Cycles (16 s)
			101	128 Cycles (16 s)	256 Cycles (32 s)
			110	256 Cycles (32 s)	512 Cycles (64 s)
			111	512 Cycles (64 s)	1024 Cycles (128 s)
<7:6>	CYR2	R/W	2 LSBs of 3-bit Remote 2 Cycle Value. The MSB of the 3-bit code resides in Dynamic T_{MIN} Control Register 1 (Reg. 0x36). These three bits define the delay time between making subsequent T_{MIN} adjustments in the control loop for the Remote 2 channel, in terms of number of monitoring cycles. The system has associated thermal time constants that need to be found to optimize the response of fans and the control loop.		
			Bits	**Decrease Cycle**	**Increase Cycle**
			000	4 Cycles (0.5 s)	8 Cycles (1 s)
			001	8 Cycles (1 s)	16 Cycles (2 s)
			010	16 Cycles (2 s)	32 Cycles (4 s)
			011	32 Cycles (4 s)	64 Cycles (8 s)
			100	64 Cycles (8 s)	128 Cycles (16 s)
			101	128 Cycles (16 s)	256 Cycles (32 s)
			110	256 Cycles (32 s)	512 Cycles (64 s)
			111	512 Cycles (64 s)	1024 Cycles (128 s)

1. This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Further attempts to write to this register have no effect.

Table 52. REGISTER 0X42 − INTERRUPT STATUS REGISTER 2 (POWER-ON DEFAULT = 0X00)

Bit No.	Mnemonic	R/W	Description
<0>	RES	Read-only	Reserved for future use.
<1>	OVT	Read-only	A 1 indicates that one of the $\overline{\text{THERM}}$ overtemperature limits has been exceeded. This bit is cleared on a read of the status register when the temperature drops below $\overline{\text{THERM}}$ − T_{HYST}.
<2>	FAN1	Read-only	A 1 indicates that Fan 1 has dropped below minimum speed or has stalled. This bit is NOT set when the PWM1 output is off.
<3>	FAN2	Read-only	A 1 indicates that Fan 2 has dropped below minimum speed or has stalled. This bit is NOT set when the PWM2 output is off.
<4>	FAN3	Read-only	A 1 indicates that Fan 3 has dropped below minimum speed or has stalled. This bit is NOT set when the PWM3 output is off.
<5>	F4P	Read-only	A 1 indicates that Fan 4 has dropped below minimum speed or has stalled. This bit is NOT set when the PWM3 output is off. If Pin 9 is configured as the $\overline{\text{THERM}}$ timer input for $\overline{\text{THERM}}$ monitoring, this bit is set when the $\overline{\text{THERM}}$

Table 56. PWM CONFIGURATION REGISTERS (POWER-ON DEFAULT = 0X62) (Note 1)

Register Address	R/W	Description
0x5C	R/W	PWM1 Configuration
0x5D	R/W	PWM2 Configuration
0x5E	R/W	PWM3 Configuration

1. These registers become read-only when the Configuration Register 1 loer

Table 59. TEMP T_{RANGE}/PWM FREQUENCY REGISTER BITS

Bit No.	Mnemonic	R/W	Description
<2:0>	FREQ	R/W	These bits control the PWMx frequency. 000 = 11.0 Hz 001 = 14.7 Hz 010 = 22.1 Hz 011 = 29.4 Hz 100 = 35.3 Hz (Default) 101 = 44.1 Hz 110 = 58.8 Hz 111 = 88.2 Hz
<3>	THRM	R/W	THRM = 1 causes the $\overline{\text{THERM}}$ pin (Pin 9) to assert low as an output when this temperature channel's $\overline{\text{THERM}}$ limit is exceeded by 0.25°C. The $\overline{\text{THERM}}$ pin remains asserted until the temperature is equal to or below the $\overline{\text{THERM}}$ limit. The minimum time that $\overline{\text{THERM}}$ asserts for is one monitoring cycle. This allows clock modulation of devices that incorporate this feature. THRM = 0 makes the $\overline{\text{THERM}}$ pin act as an input only, for example, for Pentium® 4 $\overline{\text{PROCHOT}}$ monitoring, when Pin 9 is configured as $\overline{\text{THERM}}$.
<7:4>	RANGE	R/W	These bits determine the PWM duty cycle vs. temperature slope for automatic fan control. 0000 = 2°C 0001 = 2.5°C 0010 = 3.33°C 0011 = 4°C 0100 = 5°C 0101 = 6.67°C 0110 = 8°C 0111 = 10°C

Table 60. REGISTER 0X62 − ENHANCED ACOUSTICS REGISTER 1 (POWER-ON DEFAULT = 0X00) (Note 1)

Bit No.	Mnemonic	R/W	Description	
[2:0]	ACOU	R/W	These bits select the ramp rate applied to the PWM1 output. Instead of PWM1 jumping instantaneously to its newly calculated speed, PWM1 ramps gracefully at the rate determined by these bits. This feature enhances the acoustics of the fan being driven by the PWM1 output.	
			Time Slot Increase 000 = 1 001 = 2 010 = 3 011 = 4 100 = 8 101 = 12 110 = 24 111 = 48	**Time for 33% to 100%** 35 sec 17.6 sec 11.8 sec 7 sec 4.4 sec 3 sec 1.6 sec 0.8 sec
<3>	EN1	R/W	When this bit is 1, acoustic enhancement is enabled on PWM1 output.	
<4>	SYNC	R/W	SYNC = 1 synchronizes fan speed measurements on TACH2, TACH3, and TACH4 to PWM3. This allows up to three fans to be driven from PWM3 output and their speeds to be measured. SYNC = 0, only TACH3 and TACH4 are synchronized to PWM3 output.	
<5>	MIN1	R/W	When the ADT7460 is in automatic fan control mode, this bit defines whether PWM1 is off (0% duty cycle) or at PWM1 minimum duty cycle when the controlling temperature is below its T_{MIN} − Hysteresis value. 0 = 0% Duty Cycle below T_{MIN} − Hysteresis 1 = PWM1 Minimum Duty Cycle below T_{MIN} − Hysteresis	
<6>	MIN2	R/W	When the ADT7460 is in automatic fan speed control mode, this bit defines whether PWM2 is off (0% duty cycle) or at PWM2 minimum duty cycle when the controlling temperature is below its T_{MIN} − Hysteresis value. 0 = 0% Duty Cycle below T_{MIN} − Hysteresis 1 = PWM2 Minimum Duty Cycle below T_{MIN} − Hysteresis	
<7>	MIN3	R/W	When the ADT7460 is in automatic fan speed control mode, this bit defines whether PWM3 is off (0% duty cycle) or at PWM3 minimum duty cycle when the controlling temperature is below its T_{MIN}− Hysteresis value. 0 = 0% Duty Cycle below T_{MIN} − Hysteresis 1 = PWM3 Minimum Duty Cycle below T_{MIN} − Hysteresis	

1. This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Further attempts to write to this register have no effect.

Table 61. REGISTER 0X63 − ENHANCED ACOUSTICS REGISTER 2 (POWER-ON DEFAULT = 0X00) (Note 1)

Bit No.	Mnemonic	R/W	Description	
[2:0]	ACOU3	R/W	These bits select the ramp rate applied to the PWM3 output. Instead of PWM3 jumping instantaneously to its newly calculated speed, PWM3 ramps gracefully at the rate determined by these bits. This effect enhances the acoustics of the fan being driven by the PWM3 output.	
			Time Slot Increase 000 = 1 001 = 2 010 = 3 011 = 4 100 = 8 101 = 12 110 = 24 111 = 48	**Time for 33% to 100%** 35 sec 17.6 sec 11.8 sec 7 sec 4.4 sec 3 sec 1.6 sec 0.8 sec
<3>	EN3	R/W	When this bit is 1, acoustic enhancement is enabled on PWM3 output.	
<6:4>	ACOU2	R/W	These bits select the ramp rate applied to the PWM2 output. Instead of PWM2 jumping instantaneously to its newly calculated speed, PWM2 ramps gracefully at the rate determined by these bits. This effect enhances the acoustics of the fans being driven by the PWM2 output.	
			Time Slot Increase 000 = 1 001 = 2 010 = 3 011 = 4 100 = 8 101 = 12 110 = 24 111 = 48	**Time for 33% to 100%** 35 sec 17.6 sec 11.8 sec 7 sec 4.4 sec 3 sec 1.6 sec 0.8 sec
<7>	EN2	R/W	When this bit is 1, acoustic enhancement is enabled on PWM2 output.	

1. This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Further attempts to write to this register have no effect.

Table 62. PWM MIN DUTY CYCLE REGISTERS (Note 1)

Register Address	R/W	Description	Power-On Default
0x64	R/W	PWM1 Min Duty Cycle	0x80 (50% duty cycle)
0x65	R/W	PWM2 Min Duty Cycle	0x80 (50% duty cycle)
0x66	R/W	PWM3 Min Duty Cycle	0x80 (50% duty cycle)

1. These registers become read-only when the ADT7460 is in automatic fan control mode.

Table 63. PWM MIN DUTY CYCLE REGISTER BITS

Bit No.	Mnemonic	R/W	Description
<7:0>	PWM Duty Cycle	R/W	These bits define the PWM_{MIN} duty cycle for PWMx. 0x00 = 0% Duty Cycle (Fan Off) 0x40 = 25% Duty Cycle 0x80 = 50% Duty Cycle 0xFF = 100% Duty Cycle (Fan Full Speed)

Table 64. T_{MIN} REGISTERS (Note 1)

Register Address	R/W	**Description** (Note 2)	Power-On Default
0x67	R/W	Remote 1 Temperature T_{MIN}	0x5A (90°C)
0x68	R/W	Local Temperature T_{MIN}	0x5A (90°C)
0x69	R/W	Remote 2 Temperature T_{MIN}	0x5A (90°C)

1. These registers become read-only when the Configuration Register 1 lock bit is set. Further attempts to write to these registers have no effect.
2. These are the T_{MIN} registers for each temperature channel. When the temperature measured exceeds T_{MIN}, the appropriate fan runs at minimum speed and increase with temperature according to T_{RANGE}.

Table 65. $\overline{\text{THERM}}$ LIMIT REGISTERS (Note 1)

Register Address	R/W	**Description** (Note 2)	Power-On Default
0x6A	R/W	Remote 1 $\overline{\text{THERM}}$ Limit	0x64 (100°C)
0x6B	R/W	Local $\overline{\text{THERM}}$ Limit	0x64 (100°C)
0x6C	R/W	Remote 2 $\overline{\text{THERM}}$ Limit	0x64 (100°C)

1. This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Further attempts to write to this register have no effect.
2. If any temperature measured exceeds its $\overline{\text{THERM}}$ limit, all PWM outputs drive their fans at 100% duty cycle. This is a fail-safe mechanism incorporated to cool the system in the event of a critical overtemperature. It also ensures some level of cooling in the event that software or hardware locks up. If set to 0x80, this feature is disabled. The PWM output remains at 100% until the temperature drops below $\overline{\text{THERM}}$ Limit – Hysteresis. If the $\overline{\text{THERM}}$ pin is programmed as an output, exceeding these limits by 0.25°C can cause the $\overline{\text{THERM}}$ pin to assert low as an output.

Table 66. TEMPERATURE HYSTERESIS REGISTERS (Note 1)

Register Address	R/W	**Description** (Note 2)	Power-On Default
0x6D	R/W	Remote 1 Local Temperature Hysteresis	0x44

Table 67. XNOR TREE TEST ENABLE REGISTER (POWER-ON DEFAULT = 0X00) (Note 1)

Register Address	R/W	Description		
0x6F	R/W	XNOR Tree Test Enable		
		Bit	**Mnemonic**	**Description**
		<0>	XEN	If the XEN bit is set to 1, the device enters the XNOR tree test mode. Clearing the bit removes the device from the XNOR test mode.
		<7:1>	RES	Unused. Do not write to these bits.

1. This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Further attempts to write to this register have no effect.

Table 68. REMOTE 1 TEMPERATURE OFFSET REGISTER (POWER-ON DEFAULT = 0X00) (Note 1)

Register Address	R/W	Description
0x70	R/W	Remote 1 Temperature Offset
<7:0>	R/W	Allows a twos complement offset value to be automatically added to or subtracted from the Remote 1 temperature reading. This is to compensate for any inherent system offsets such as PCB trace resistance. LSB value = 0.25°C.

1. This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Further attempts to write to this register have no effect.

Table 69. LOCAL TEMPERATURE OFFSET REGISTER (POWER-ON DEFAULT = 0X00) (Note 1)

Register Address	R/W	Description
0x71	R/W	Local Temperature Offset
<7:0>	R/W	Allows a twos complement offset value to be automatically added to or subtracted from the local temperature reading. LSB value = 0.25°C.

1. This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Further attempts to write to this register have no effect.

Table 70. REMOTE 2 TEMPERATURE OFFSET REGISTER (POWER-ON DEFAULT = 0X00) (Note 1)

Register Address	R/W	Descriptiono e0x71.9(6.737.)289 (46fBaac2ter05i91Tm0 8 94.2236 462
		PCB trace resce. LSB value = 0.25 °C.

Table 71. REGISTER 0X73 − CONFIGURATION REGISTER 2 (POWER-ON DEFAULT = 0X00) (Note 1)

Bit No.	Mnemonic	R/W	Description
0	AIN1	R/W	AIN1 = 0, Speed of 3-wire fans measured using the TACH output from the fan. AIN1 = 1, Pin 6 is reconfigured to measure the speed of 2-wire fans using an external sensing resistor and coupling capacitor. AIN voltage threshold is set via Configuration Register 4 (Reg. 0x7D).
1	AIN2	R/W	AIN2 = 0, Speed of 3-wire fans measured using the TACH output from the fan. AIN2 = 1, Pin 7 is reconfigured to measure the speed of 2-wire fans using an external sensing resistor and coupling capacitor. AIN voltage threshold is set via Configuration Register 4 (Reg. 0x7D).
2	AIN3	R/W	AIN3 = 0, Speed of 3-wire fans measured using the TACH output from the fan. AIN3 = 1, Pin 4 is reconfigured to measure the speed of 2-wire fans using an external sensing resistor and coupling capacitor. AIN voltage threshold is set via Configuration Register 4 (Reg. 0x7D).
3	AIN4	R/W	AIN4 = 0, Speed of 3-wire fans measured using the TACH output from the fan. AIN4 = 1, Pin 9 is reconfigured to measure the speed of 2-wire fans using an external sensing resistor and coupling capacitor. AIN voltage threshold is set via Configuration Register 4 (Reg. 0x7D).
4	AVG	R/W	AVG = 1, Averaging on the temperature and voltage measurements is turned off. This allows measurements on each channel to be made much faster.
5	ATTN	R/W	ATTN = 1, the ADT7460 removes the attenuators from the 2.5 V input. The input can be used for other functions such as connecting up external sensors.
6	CONV	R/W	CONV = 1, the ADT7460 is put into a single-channel ADC conversion mode. In this mode, the ADT7460 can be made to read continuously from one input only, for example, Remote 1 temperature. It is also possible to start ADC conversions using an external clock on Pin 6 by setting Bit 2 of asure the speed of 2-wire fans using an egst2s.68036 re

Table 73. REGISTER 0X75 − INTERRUPT MASK REGISTER 2 (POWER-ON DEFAULT = 0X00)

Bit No.	Mnemonic	R/W	Description
0	RES	R/W	Reserved for future use.
1	OVT	Read-only	A 1 masks $\overline{\text{SMBALERT}}$ for overtemperature $\overline{\text{THERM}}$ conditions.
2	FAN1	R/W	A 1 masks $\overline{\text{SMBALERT}}$ for a Fan 1 fault.
3	FAN2	R/W	A 1 masks $\overline{\text{SMBALERT}}$ for a Fan 2 fault.
4	FAN3	R/W	A 1 masks $\overline{\text{SMBALERT}}$ for a Fan 3 fault.
5	F4P	R/W	A 1 masks $\overline{\text{SMBALERT}}$ for a Fan 4 fault. If the TACH4 pin is being used as the $\overline{\text{THERM}}$ input, this bit masks $\overline{\text{SMBALERT}}$ for a $\overline{\text{THERM}}$ timer event.
6	D1	R/W	A 1 masks $\overline{\text{SMBALERT}}$ for a diode open or short on Remote 1 channel.
7	D2	R/W	A 1 masks $\overline{\text{SMBALERT}}$ for a diode open or short on Remote 2 channel.

Table 74. REGISTER 0X76 − EXTENDED RESOLUTION REGISTER 1

Bit No.	Mnemonic	R/W	Description
<1:0>	2.5V	Read-only	2.5 V LSBs. Holds the 2 LSBs of the 10-bit 2.5 V measurement.
<3:2>	RES	R/W	Reserved for future use.
<5:4>	V_{CC}	Read-only	V_{CC} LSBs. Holds the 2 LSBs of the 10-bit V_{CC} measurement.
<7:6>	RES	R/W	Reserved for future use.

1. If this register is read, this register and the registers holding the MSB of each reading are frozen until read.

Table 75. REGISTER 0X77 − EXTENDED RESOLUTION REGISTER 2 (Note 1)

Bit No.	Mnemonic	R/W	Description
<1:0>	RES	R/W	Reserved for future use.
<3:2>	TDM1	Read-only	Remote 1 Temperature LSBs. Holds the 2 LSBs of the 10-bit Remote 1 temperature measurement.
<5:4>	LTMP	Read-only	Local Temperature LSBs. Holds the 2 LSBs of the 10-bit local temperature measurement.
<7:6>	TDM2	Read-only	Remote 2 Temperature LSBs. Holds the 2 LSBs of the 10-bit Remote 2 temperature measurement.

1. If this register is read, this register and the registers holding the MSB of each reading are frozen until read.

Table 76. REGISTER 0X78 − CONFIGURATION REGISTER 3 (POWER-ON DEFAULT = 0X00) (Note 1)

Bit No.	Mnemonic	R/W	Description
<0>	ALERT	R/W	ALERT = 1, Pin 5 (PWM2/ $\overline{\text{SMBALERT}}$) is configured as an $\overline{\text{SMBALERT}}$ interrupt output to indicate out-of-limit error conditions.
<1>	$\overline{\text{THERM}}$ ENABLE	R/W	$\overline{\text{THERM}}$ ENABLE = 1 enables $\overline{\text{THERM}}$

Table 77. REGISTER 0X79 − $\overline{\text{THERM}}$ STATUS REGISTER (POWER-ON DEFAULT = 0X00)

Bit No.	Mnemonic	R/W	Description
<7:1>	TMR	Read-only	Times how long $\overline{\text{THERM}}$ input is asserted. These seven bits read 0 until the $\overline{\text{THERM}}$ assertion time exceeds 45.52 ms.
<0>	ASRT/TMR0	Read-only	Is set high on the assertion of the $\overline{\text{THERM}}$

Table 81. REGISTER 0X7E − MANUFACTURER'S TEST REGISTER 1 (POWER-ON DEFAULT = 0X00)

Bit No.	Mnemonic	R/W	Description
<7:0>	RES	Read-only	Manufacturer's Test Register. These bits are reserved for manufacturer's test purposes and should NOT be written to under normal operation.

Table 82. REGISTER 0X7F − MANUFACTURER'S TEST REGISTER 2 (POWER-ON DEFAULT = 0X00)

Bit No.	Mnemonic	R/W	Description
<7:0>	RES	Read-only	Manufacturer's Test Register. These bits are reserved for manufacturer's test purposes and should NOT be written to under normal operation.

Table 83. ORDERING INFORMATION

Device Number	Temperature Range	Package Type	Package Option	Shipping†
ADT7460ARQZ REEL	−40°C to +120°C	16-lead QSOP	RQ−16	2,500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*The "Z" suffix indicates Pb−Free part.

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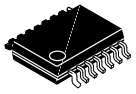
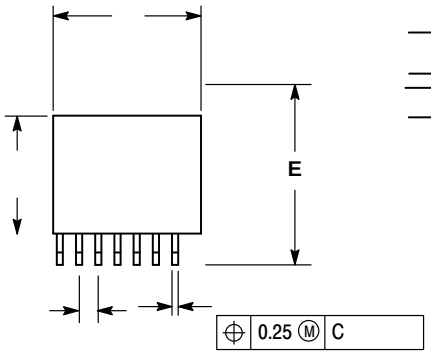
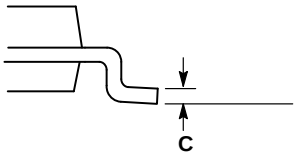


SCALE 2:1

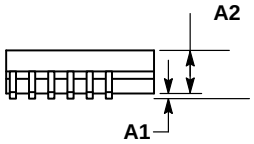
QSOP16
CASE 492−01
ISSUE A

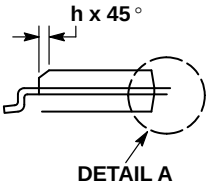
DATE 23 MAR 2011





DETAIL A





DETAIL A

NOTES:

DIM	INCHES MIN	MA
A	0.053	0.069
A1	0.004	0.010
	0.008	0.012
\	0.007	0.010
	0.025 BSC	
	0.009	0.020
L	0.016	0.050
M	0	8