

Figure 1. Functional Block Diagram

Table 4. ELECTRICAL CHARAC	TERISTICS ($T_A = T_{MIN}$ to T_{MAX} , V_{CC} =	= V_{MIN} to V_{MAX} , unless otherwise noted.) (Note 1)
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Parameter	Test Conditions/Comments	Min Typ		Max	Unit
Power Supply					
Supply Voltage		3.0	3.3	5.5	V
Supply Current, I _{CC}	ADC Active, Interface Inactive (Note 2)	-	1.5	4.0	mA

Parameter	Test Conditions/Comments	Min	Тур	Max	Unit
OPEN-DRAIN SERIAL BUS OUTPUT (SDA)					
Output Low Voltage, V _{OL}	$I_{OUT} = -3 \text{ mA}, V_{CC} = +3.3 \text{ V}$	-	-	0.4	V
High Level Output Leakage Current, I _{OH}	$V_{OUT} = V_{CC}$	-	0.1	±1.0	μΑ

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 3. Supply Current vs. Supply Voltage

Figure 4. Supply Current vs. Temperature

Figure 5. Local Sensor Temperature Error

Figure 6. Remote Sensor Temperature Error

Figure 7. Temperature Error Measuring Intel Pentium[®] 4 Processor

Figure 8. ADT7462 Response to Thermal Shock

TYPICAL PERFORMANCE CHARACTERISTICS (CONT'D)

Figure 9. Remote Temperature Error vs. Resistance (SRC) Figure 10. Local Temperature Error vs. Power Supply Noise Frequency

Figure 11. Remote Temperature Error vs. Power Supply Noise Frequency

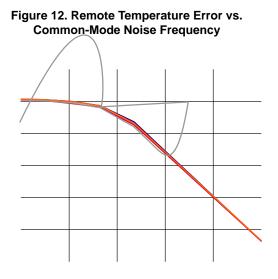


Figure 13. Remote Temperature Error vs. Differential-Mode Noise Frequency Figure 14. Remote Temperature Error vs. Capacitance Between D+ and D-

TYPICAL PERFORMANCE CHARACTERISTICS (CONT'D)

Figure 15. Local Temperature vs. Power-On Reset Timeout Figure 16. Applied Voltage vs. V_{BATT} Reading

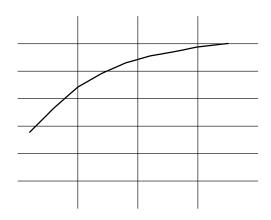


Figure 17. TACH Accuracy vs. Supply Voltage

Figure 18. TACH Accuracy vs. Temperature

FUNCTION DESCRIPTION: EASY CONFIGURATION OPTIONS

There are a number of multifunctional pins on the ADT7462 that need to be configured on powerup to suit the desired application. Note that due to the large number of pins that need to be configured, it could take several SMBus transactions to achieve the required configuration. For this reason, the ADT7462 has five easy configuration options. The user sets a bit in the easy configuration option register (0x14) to set up the required configuration (see Table 5).

Table 5. EASY CONFIGURATION REGISTER
SETTINGS

Easy Configuration Option	Register 0x14 Setting
Option 1	Bit 0 = 1
Option 2	Bit 1 = 1
Option 3	Bit 2 = 1
Option 4	Bit 3 = 1
Option 5	Bit 4 = 1

Once the most convenient easy configuration option has been set, the user can configure any of the pins individually. The setup complete bit (Bit 5 of Register 0x01) must then be set to 1 to indicate that the ADT7462 is configured correctly, and then monitoring of the selected channels begins.

The following is a detailed description of the five easy configuration options that are available.

Configuration Option 1

Configuration Option 1 is the default configuration. It is also the most suitable for thermal monitoring, voltage monitoring, and fan control for single and dual processor systems. Features of Configuration Option 1 include the following:

- One Local and Three Remote Temperature Channels
- Four PWM Drives and Eight TACH Inputs
- Two THERM I/Os
- Voltage Monitoring
- •

Configuration Option 2

Configuration Option 2 is used for thermal monitoring and fan control for Processor 1 and Processor 2 in a dual processor system. It can also monitor one set of VIDs, if required. Features of Configuration Option 2 include the following:

- One Local and Three Remote Thermal Channels
- Up to Four PWM Drives and Up to Eight TACH Inputs (VID Pins and TACHs/PWMs are Muxed Together)
- Two THERM I/Os
- Two VRD Inputs
- RESET I/O
- Two V_{CCP} Voltage Monitoring Channels

Figure 20 shows the pin configuration when Configuration Option 2 is chosen.

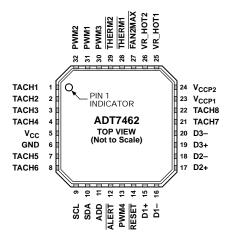


Figure 20. Configuration Option 2

Table 7. CONFIGURATION OPTION 2

Pin	Function	Configuration Register	Bit Value
1†	TACH1	Pin Configuration Reg 1	Bit 4 = 1
2†	TACH2	Pin Configuration Reg 1	Bit 3 = 1
34	TACH3	Pin Configuration Reg 1	Bit 2 = 1
4†	TACH4	Pin Configuration Reg 1	Bit 1 = 1
7	TACH5	Pin Configuration Reg 1	Bit 0 = 1

81 Tf10 0 0 10 69.8457 604.1198 Tm-.00344.385 0 = 1

Configuration Option 4

Configuration Option 4 is used to monitor temperature, voltages, and fans for Processor 1 in a dual processor system. Features of Configuration Option 4 include the following:

- One Local and Two Remote Temperature Channels
- •

Serial Bus Interface

The ADT7462 is controlled through use of the serial system management bus (SMBus). The ADT7462 is connected to this bus as a slave device, under the control of a master controller. The SMBus interface in the ADT7462

the data byte read from the data register (see Figure 26).

• If the address pointer register is known to be already at the desired address, data can be read from the corresponding data register without first writing to the address pointer register (see Figure 26).

It is possible to read a data byte from a data register without first writing to the address pointer register, if the address pointer register is already at the correct value.

However, it is not possible to write data to a register without writing to the address pointer register, because the

SCL		
SDA	A2	R/W

first data byte of a write is always written to the address pointer register.

In addition to supporting the send byte and receive byte protocols, the ADT7462 also supports the read byte protocol (see System Management Bus Specifications Rev. 2.0 for more information).

If several read or write operations must be performed in succession, then the master can send a repeat start condition, instead of a stop condition, to begin a new operation.

Figure 24. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

SMBus Timeout

The ADT7462 includes an SMBus timeout feature. If there is no SMBus activity for 25 ms, the ADT7462 assumes that the bus is locked and releases the bus. This prevents the device from locking or holding the SMBus while the device is expecting data. Some SMBus controllers cannot handle the SMBus timeout feature, so it can be disabled.

Configuration Register 3 (0x03)

Bit 1 SCL_Timeout = 1; SCL Timeout Enabled Bit 1 SCL_Timeout = 0; SCL Timeout Disabled (Default) Bit 2 SDA_Timeout = 1; SDA Timeout Enabled Bit 2 SDA_Timeout = 0; SDA Timeout Disabled (Default)

TEMPERATURE AND VOLTAGE MEASUREMENT

Temperature Measurement

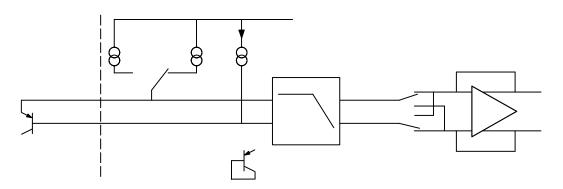


Figure 33. Input Signal Conditioning

Noise Filtering

For temperature sensors operating in noisy environments, the industry-standard practice is to place a capacitor across the D+ and D- pins to help combat the effects of noise. However, large capacitances affect the accuracy of the temperature measurement, leading to a recommended maximum capacitor value of 1000 pF. While this capacitor does reduce noise, it does not eliminate it, making it difficult to use the sensor in a very noisy environment.

The ADT7462 has a major advantage over other devices in eliminating the effects of noise on the external sensor. The series resistance cancellation feature allows a filter to be constructed between the external temperature sensor and the

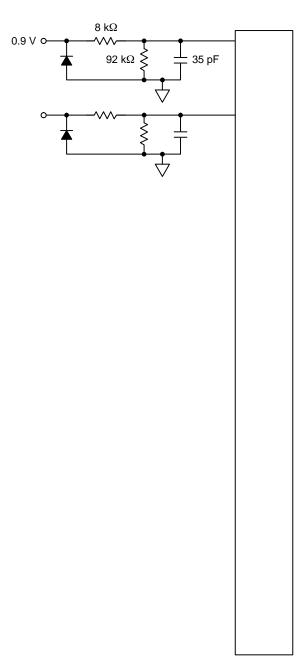


Figure 36. Voltage Input Structures

Table 17. VOLTAGE VALUE AND LIMIT REGISTERS

			Low Limit		High Limit	
Voltage Value	Pin No.	Value Register Address	Register	Default	Register	Default
+12V1	7	0xA3	0x6D	0x00	0x7C	0xFF
+12V2	8	0xA5	0x6E	0x00	0x7D	0xFF
+3.3V	13	0x96	0x70	0x00	0x68	0xFF
+1.8V or +2.5V	15	0x8B	0x45	0x40	0x49	0x95
+1.25V or +0.9V	19	0x8F	0x47	0x40	0x4B	0x95
+5V	21	0xA7	0x71	0x00	0x7E	0xFF
+12V3	22	0xA9	0x6F	0x00	0x7F	0xFF
V _{CCP1} , +1.5V, +1.8V, +2.5V	23	0x90	0x72	0x20	0x69	0xFF
V _{CCP2} , +1.5V, +1.8V, +2.5V	24	0x91	0x73	0x00	0x6A	0xFF
+1.2V1 (G _{BIT}) or +3.3V	25	0x92	0x74	0x00	0x6B	0xFF
+1.2V2 (FSB_V _{TT}) or V _{BATT}	26	0x93	0x75	0x80	0x6C	0xFF
+1.5V1 (ICH)	28	0x94	0x77	0x00	0x50	0xA4
+1.5V2 (3GIO)	29	0x95	0x76	0x00	0x4C	0xA4

drive outputs. If all eight fans are being used in the system, two fans should be driven in parallel from each PWM output. Figure 42 shows how to drive two fans in parallel using the NDT3055L MOSFET. This information is



Figure 45. Fan with Strong TACH. Pullup to > V_{CC} or Totem-Pole Output, Clamped with Zener Diode and Resistor

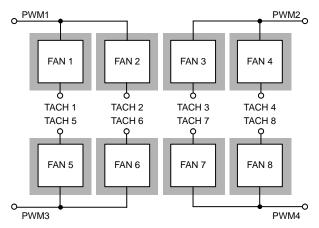


Figure 48. Synchronizing Fan PWM Output and TACH Inputs

Driving and Measuring the Speed of One Fan from One PWM Output

If four single fans are being controlled and measured by the ADT7462, the following configuration should be used. This applies only to 3-wire fans controlled using low frequency PWM with pulse stretching enabled.

Fan 1 is driven by PWM1 and measured using TACH1.

Fan 2 is driven by PWM2 and measured using TACH3. Fan 3 is driven by PWM3 and measured using TACH5. Fan 4 is driven by PWM4 and measured using TACH7.

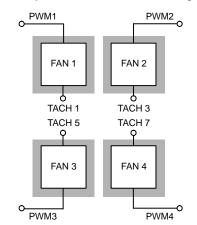


Figure 49. Driving and Measuring the Speed on a Single Fan

The PWM output is pulse stretched until a valid TACH is read on both TACH inputs synchronized to the particular PWM output. If one fan is connected to one PWM output, the PWM output is pulse stretched until the counter has timed out on the disconnected TACH input. In this case, the pulse is stretching longer than necessary in an effort to sense a disconnected fan. The speed of the connected fan may be increased and an audible change in fan speed may be observed. There are two options to prevent the PWM output from being stretched longer than necessary in this case.

 Connect the two synchronized TACH inputs together; for example, if PWM1 is driving a single fan being sensed on TACH1 only, connect TACH1 and TACH2 together.

• Turn off pulse stretching on the unused TACH input; that is, if PWM1 is driving a single fan being sensed on TACH1 only, turn off pulse stretching on TACH2 in Register 0x08. In this register:

Bit 0 controls pulse stretching on TACH1 and TACH5. Bit 1 controls pulse stretching on TACH2 and TACH6. Bit 2 controls pulse stretching on TACH3 and TACH7. Bit 3 controls pulse stretching on TACH4 and TACH8.

Note that the TACH assignments in this register differ from the TACHs synchronized to each PWM output. Therefore, if the intention is to drive and sense four fans, connecting the TACHs together as described in Option 1 allows pulse stretching on all channels.

To enable fan speed measurements four times a second, set the FAST bit (Bit 0) of Configuration Register 2 (0x02). When the FAST bit is set, fan TACH readings are updated every 250 ms.

Fan Speed Measurement Registers

Fan speed measurement involves a 2-register read for each measurement. The low byte should be read first. This causes the high byte to be frozen until both high and low byte registers have been read, preventing erroneous TACH readings. The fan tachometer reading registers report back the number of 11.11 μ s period clocks (90 kHz oscillator) gated to the fan speed counter, from the rising edge of the first fan TACH pulse to the rising edge of the third fan TACH pulse (because two pulses per revolution are being counted). Because the device is essentially measuring the fan TACH period, the higher the count value, the slower the fan is actually running. A 16-bit fan tachometer reading of 0xFFFF indicates either that the fan has stalled or is running

Calculating Fan Speed Assuming a fan with two pulses per revolution (and two pulses per revolution being measured), fan speed is

Fan Speed Control

The ADT7462 controls fan speed using two different modes: automatic and manual.

In automatic fan speed control mode, fan speed is automatically varied with temperature and without CPU intervention, after initial parameters are set up. The advantage of this mode is that if the system hangs, the system is protected from overheating. The automatic fan speed control incorporates a feature called dynamic T_{MIN} calibration. This feature reduces the design effort required to program the automatic fan speed control loop. For more information on how to program the automatic fan speed control loop and dynamic T_{MIN} operation, see the Programming the Automatic Fan Speed Control Loop section.

In manual fan speed control mode, the ADT7462 allows the duty cycle of any PWM output to be manually adjusted. This is useful if the user wants to change fan speed in the software or adjust PWM duty cycle output for test purposes. Bits [7:5] of Register 0x21 to Register 0x24 (PWM configuration registers) control the behavior of each PWM output. Under manual control, each PWM output can be manually updated by writing to Register 0xAA to Register 0xAD (PWM duty cycle registers).

Programming the PWM Current Duty Cycle Registers

The PWM current duty cycle registers are 8-bit registers that allow the PWM duty cycle for each output to be set anywhere from 0% to 100% in steps of 0.39%.

The value to be programmed into the $\ensuremath{\mathsf{PWM}_{\mathsf{MIN}}}$ register is given by:

Value (decimal) = PWM_{MIN}/0.39

- Example 1: For a PWM duty cycle of 50%, Value (decimal) = 50/0.39 = 128 decimal Value = 128 decimal or 0x80
- Example 2: For a PWM duty cycle of 33%, Value (decimal) = 33/0.39 = 85 decimal Value = 84 decimal or 0x54

PWM Duty Cycle Registers

Register 0xAA PWM1 Duty Cycle = 0x00 (0% default) Register 0xAB PWM2 Duty Cycle = 0x00 (0% default) Register 0xAC PWM3 Duty Cycle = 0x00 (0% default) Register 0xAD PWM4 Duty Cycle = 0x00 (0% default)

By reading the PWMx current duty cycle registers, the user can keep track of the current duty cycle on each PWM output, even when the fans are running in automatic fan speed control mode or acoustic enhancement mode.

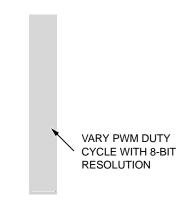


Figure 50. Control PWM Duty Cycle Manually with a Resolution of 0.39%

Programming the Automatic Fan Speed Control Loop

Note that to better understand the automatic fan speed control loop, use of the ADT7462 evaluation board and software is strongly recommended while reading this section.

This section provides the system designer with an understanding of the automatic fan control loop and provides step-by-step guidance on effectively evaluating and selecting critical system parameters. To optimize system characteristics, the designer needs to carefully plan system configuration, including the number of fans, where they are located, and what temperatures are being measured in the particular system.

The mechanical or thermal engineer who is tasked with the system thermal characterization should also be involved at the beginning of the process.

Automatic Fan Control Overview

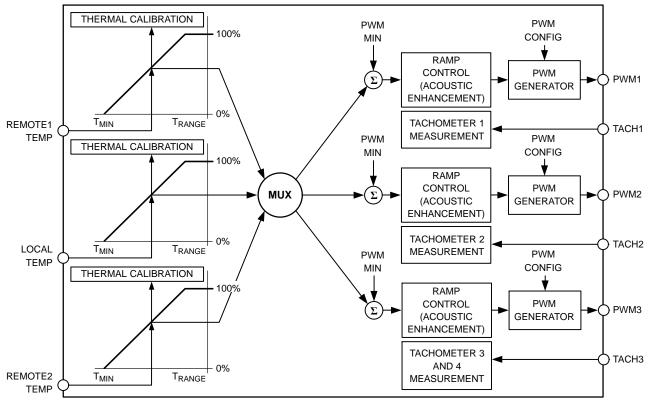
The ADT7462 can automatically control the speed of fans based upon the measured temperature. This is done independently from CPU intervention once initial parameters are set up.

The ADT7462 has a local temperature sensor and up to three remote temperature channels that can be connected to a CPU on-chip thermal diode (available on Intel Pentium class and other CPUs/GPUs). These four temperature channels can be used as the basis for automatic fan speed control to drive fans using pulse-width modulation (PWM).

Automatic fan speed control reduces acoustic noise by optimizing fan speed according to accurately measured temperature. Reducing fan speed can also decrease system current consumption. The automatic fan speed control mode is very flexible, owing to the number of programmable parameters, including T_{MIN} and T_{RANGE} . The T_{MIN} and

T_{RANGE} values for a temperature channel and, therefore, for a given fan, are critical because they define the thermal characteristics of the system. The thermal validation of the system is one of the most important steps in the design process, so these values should be selected carefully.

Figure 51 gives a top-level overview of the automatic fan control circuitry on the ADT7462. From a systems-level perspective, up to four system temperatures can be monitored and used to control four PWM outputs. The four PWM outputs can be used to control up to eight fans. The ADT7462 allows the speed of eight fans to be monitored. The Remote 1 and Remote 2 temperature channels have a thermal calibration block, allowing the designer to individually configure the thermal characteristics of those temperature channels. For example, the CPU fan can be run when CPU temperature increases above 60°C and a chassis fan can be run when the local temperature increases above 45°C. At this stage, the designer has not assigned these thermal calibration settings to a particular fan drive (PWM) channel. The right side of Figure 51 shows controls that are fan-specific. The designer has control over individual parameters such as minimum PWM duty cycle, fan speed failure thresholds, and even ramp control of the PWM outputs. Automatic fan control, then, ultimately allows graceful fan speed changes that are less perceptible to the system user.





Step 1 – Configuring the MUX

First, the user needs to decide how many temperature channels are being measured and how many fans need to be controlled and monitored. When these decisions have been made, the fans can be assigned to particular temperature channels. Not only can fans be assigned to individual channels, but the behavior of the fans is also configurable. For example, fans can be run under automatic fan control; they can be run manually (under software control) or they can be run at the fastest speed calculated by multiple temperature channels. The MUX is the bridge between

Step 2 – T_{MIN} Settings for Thermal Calibration Channels

 T_{MIN} is the temperature at which the fans start to turn on under automatic fan control. The speed at which the fan runs at T_{MIN} is programmed later. The T_{MIN} values chosen are temperature channel-specific; for example, 25°C for ambient channel, 30°C for VRM temperature, and 40°C for processor temperature.

 T_{MIN} is an 8-bit value, either twos complement or Offset 64, that can be programmed in 1°C increments. There is a T_{MIN} register associated with each temperature measurement channel: local, Remote 1, Remote 2, and Remote 3. When the T_{MIN} value is exceeded, the fan turns on and runs at the minimum PWM duty cycle. The fan turns off after the temperature has dropped below $T_{MIN} - T_{HYST}$.

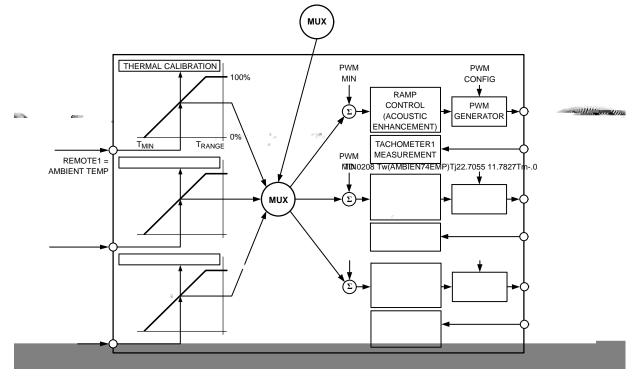


Figure 52. Assigning Temperature Channels to Fan Channels

Programming the $\ensuremath{\mathsf{PWM}_{\mathsf{MIN}}}$ Registers

The PWM_{MIN} registers are 8-bit registers that allow the minimum PWM duty cycle for each output to be configured anywhere from 0% to 100%. This allows the minimum PWM duty cycle to be set in steps of 0.39%.

The value to be programmed into the $\ensuremath{\mathsf{PWM}_{\mathsf{MIN}}}$ register is given by:

Value (decimal) = PWM_{MIN} /0.39

Example 1: For a minimum PWM duty cycle of 50%, Value (decimal) = 50/0.39 = 128 (decimal) Value = 128 (decimal) or 0x80 (hexadecimal)

Example 2: For a minimum PWM duty cycle of 33%, Value (decimal) = 33/0.39 = 85 (decimal) Value = 85 (decimal) or 0x54 (hexadecimal)

PWM_{MIN}MIN

The T_{RANGE} or fan control slope is determined by the following procedure:

- 1. Determine the maximum operating temperature for that channel (for example, 70°C).
- Determine experimentally the fan speed (PWM duty cycle value) that does not exceed the temperature at the worst-case operating points. (For example, 70°C is reached when the fans are running at 50% PWM duty cycle.)
- 3. Determine the slope of the required control loop to meet these requirements.
- 4. Using the ADT7462 evaluation software, this functionality can be graphically programmed and visualized.

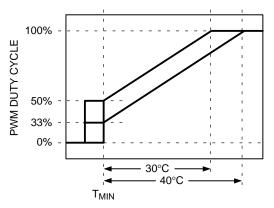


Figure 58. Adjusting PWM_{MIN} Affects T_{RANGE}

 T_{RANGE} is implemented as a slope, which means that as PWM_{MIN} is changed, T_{RANGE} changes, but the actual slope remains the same. The higher the PWM_{MIN} value, the smaller the effective T_{RANGE} ; that is, the fan reaches full speed (100%) at a lower temperature.

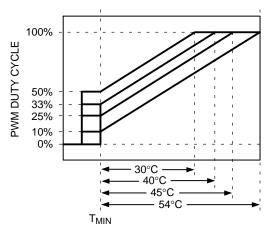


Figure 59. Increasing PWM_{MIN} Changes Effective T_{RANGE}

For a given T_{RANGE} value, the temperature at which the fan runs at full speed for different PWM_{MIN} values can be easily calculated by:

 $T_{MAX} = T_{MIN} + (Max DC - Min DC) \times T_{RANGE}/170$

where:

 T_{MAX} is the temperature at which the fan runs full speed. T_{MIN} is the temperature at which the fan turns on. Max DC is the maximum duty cycle (100%) = 255 decimal. Min DC is equal to PWM

 T_{RANGE} for different PWM_{MIN} values can be calculated using Equation 7.

 $\mathrm{T_{MAX}} = \mathrm{T_{MIN}} + (\mathrm{Max}\ \mathrm{DC} - \mathrm{Min}\ \mathrm{DC}) \times \mathrm{T_{RANGE}}/\mathrm{170} \eqno(eq.\ 7)$

where (Max DC – Min DC) \times T_{RANGE} /170 is the effective T_{RANGE} value.

Figure 60 shows PWM duty cycle vs. temperature for each ${\rm T}$

Note on 4-wire Fans

The control range for 4-wire fans is much wider than that of 2-wire or 3-wire fans. In many cases, 4-wire fans can start with a PWM drive of as little as 20%.

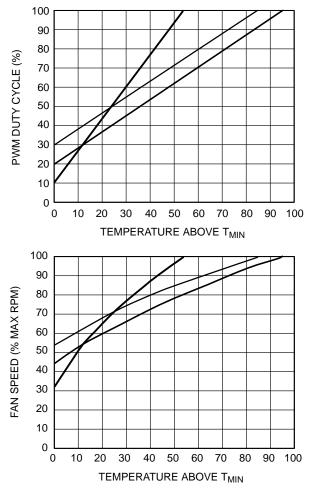


Figure 62. T_{RANGE} and % Fan Speed Slopes for VRM, Ambient, and CPU Temperature Channels

- Step 6 T_{THERM} for Temperature Channels
 - T_{THERM} is the absolute maximum temperature allowed

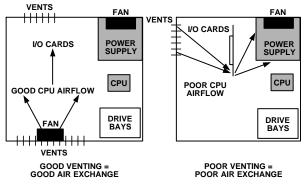


Figure 65. Chassis Airflow Issues

- Worst-Case Processor Power Consumption This data sheet maximum does not necessarily reflect the true processor power consumption. Designing for worst-case CPU power consumption can result in a processor becoming over-cooled (generating excess system noise).
- Worst-Case Peripheral Power Consumption The tendency is to design to data sheet maximums for peripheral components (again over-cooling the system).
- Worst-Case Assembly Every system manufactured is unique because of manufacturing variations. Heat sinks may be loose

Table 28 provides a brief description of each parameter.

Table 28. T_{MIN}

Table 29. CYCLE BIT ASSIGNMENTS

Code	Short Cycle	Duration	Long Cycle	Duration
000	8 cycles 1 sec		16 cycles	2 sec
001	16 cycles	2 sec	32 cycles	4 sec
010	32 cycles	4 sec	64 cycles	8 sec
011	64 cycles	8 sec	128 cycles	16 sec
100	128 cycles	16 sec	256 cycles	32 sec
101	256 cycles	32 sec	512 cycles	64 sec
110	512 cycles	64 sec	1024 cycles	128 sec
111	1024 cycles	128 sec		

Approaches to System Acoustic Enhancement

There are two different approaches to implementing system acoustic enhancement: temperature-centric and fan-centric.

The temperature-centric approach involves smoothing transient temperatures as they are measured by a temperature source (for example, Remote 1 temperature). The temperature values used to calculate the PWM duty cycle values are smoothed, reducing fan speed variation. However, this approach causes an inherent delay in updating fan speed and causes the thermal characteristics of the system to change. It also causes the system fans to stay on longer than necessary, because the fan's reaction is merely delayed. The user has no control over noise from different fans driven by the same temperature source. Consider, for example, a system in which control of a CPU cooler fan (on PWM1) and a chassis fan (on PWM2) uses Remote1 temperature. Because the Remote 1 temperature is smoothed, both fans are updated at exactly the same rate. If the chassis fan is much louder than the CPU fan, there is no way to improve its acoustics without changing the thermal solution of the CPU cooling fan.

The fan-centric approach to system acoustic enhancement controls the PWM duty cycle, driving the fan at a fixed rate (for example, 6%). Each time the PWM duty cycle is updated, it is incremented by a fixed 6%. As a result, the fan ramps smoothly to its newly calculated speed. If the temperature starts to drop, the PWM duty cycle immediately decreases by 6% at every update. Therefore, the fan ramps previous PWM value, the previous PWM duty cycle is decremented by 1, 2, 3, 5, 8, 12, 24, or 48 time slots. Each time the PWM duty cycle is incremented or decremented, its value is stored as the previous PWM duty cycle for the next comparison.

A ramp rate of 1 corresponds to one time slot, which is 1/255 of the PWM period. In enhanced acoustics mode, incrementing or decrementing by 1 changes the PWM output by $1/255 \times 100\%$.

Step 11 – Ramp Rate for Acoustic Enhancement

The optimal ramp rate for acoustic enhancement can be found through system characterization after the thermal optimization has been finished. The effect of each ramp rate should be logged, if possible, to determine the best setting for a given solution.

Enhanced Acoustics Register 1 (0x1A)

Bits [4:2] RR1 select the ramp rate for PWM1.

- 000 = 1 time slot = 35 seconds 001 = 2 time slots = 17.6 seconds 010 = 3 time slots = 17.6 seconds 010 = 3 time slots = 17.8 seconds 101 = 5 time slots = 7 seconds 100 = 8 time slots = 7 seconds 101 = 12 time slots = 3 seconds 110 = 24 time slots = 1.6 seconds 111 = 48 time slots = 0.8 secondsBits [7:5] RR2 select the ramp rate for PWM2. 000 = 1 time slot = 35 seconds 001 = 2 time slot = 17.6 seconds 010 = 3 time slots = 11.8 seconds 011 = 5 time slots = 7 seconds 100 = 8 time slots = 4.4 seconds
 - 101 = 12 time slots = 3 seconds
 - 110 = 24 time slots = 1.6 seconds
 - 111 = 48 time slots = 0.8 seconds

Enhanced Acoustics Register 2 (0x1B)

Bits [4:2] RR3 select the ramp rate for PWM3. 000 = 1 time slot = 35 seconds 001 = 2 time slots = 17.6 seconds 010 = 3 time slots = 11.8 seconds 011 = 5 time slots = 7 seconds 100 = 8 time slots = 4.4 seconds 101 = 12 time slots = 3 seconds 110 = 24 time slots = 1.6 seconds 111 = 48 time slots = 0.8 seconds Bits [7:5] RR4 select the ramp rate for PWM4. 000 = 1 time slot = 35 seconds 001 = 2 time slots = 17.6 seconds 010 = 3 time slots = 11.8 seconds 011 = 5 time slots = 7 seconds 100 = 8 time slots = 4.4 seconds 101 = 12 time slots = 3 seconds 110 = 24 time slots = 1.6 seconds 111 = 48 time slots = 0.8 seconds

Another way to view the ramp rates is to measure the time it takes for the PWM output to ramp up from 0% to 100% duty cycle for an instantaneous change in temperature. This can be tested by putting the ADT7462 into manual mode and changing the PWM output from 0% to 100% PWM duty cycle. The PWM output takes 35 seconds to reach 100% when a ramp rate of one time slot is selected.

Figure 77 shows remote temperature plotted against PWM duty cycle for enhanced acoustics mode. The ramp rate is set to 48, which corresponds to the fastest ramp rate. Assume that a new temperature reading is available every 115 ms. With these settings, it takes approximately 0.76 seconds to go from 33% duty cycle to 100% duty cycle (full speed). Even though the temperature increases very rapidly, the fan ramps up to full speed gradually.

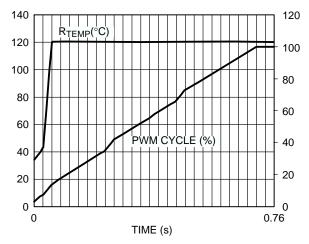


Figure 77. Enhanced Acoustics Mode with Ramp Rate = 48

Figure 78 shows how changing the ramp rate from 48 to 8 affects the control loop. The overall response of the fan is slower. Because the ramp rate is reduced, it takes longer for the fan to achieve full running speed. In this case, it takes approximately 4.4 seconds for the fan to reach full speed.

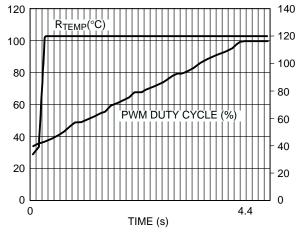
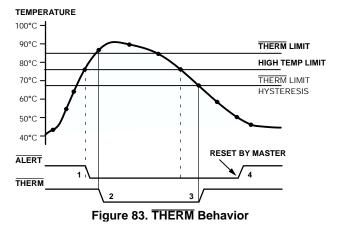


Figure 78. Enhanced Acoustics Mode with Ramp Rate = 8

The freewheeling test procedure is as follows:

is $2/3 \times V_{CCB}$ the correct threshold for an AGTL + signal. The THERM assert bits in Host Thermal Status Register 2 (0xB9) are set to Logic 1 whenever the THERM input is asserted low. The THERM state bits in Host Thermal Status Register 2 (0xB9) indicate that a high-to-low transition has taken place on the THERM pin.



THERM Timer

The ADT7462 can also measure assertion times on the THERM inputs as a percentage of a timer window. The timer window for the THERM1 input is programmed using Bits [4:2] of the THERM configuration register (0x0D). The timer window for the THERM2 input is programmed using Bits [7:5] of the THERM configuration register (0x0D).

When a GPIO pin is configured as an output, the corresponding bit in the GPIO status register becomes read/write. Setting this bit then asserts the GPIO output. (Again, "asserted" can be high or low, depending on the setting of the polarity bit.) The effect of a GPIO status register bit on the ALERT output can be masked by setting the corresponding bit in one of the GPIO mask registers.

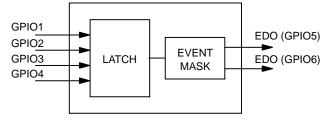
When the pin is configured as an output, the corresponding status bit is automatically masked to prevent the data written to the status bit from causing an interrupt. When configured as inputs, the GPIO pins can be connected to external interrupt sources such as temperature sensors with digital output.

EDO Circuitry

The ADT7462 has the added functionality that the assertion of one of the four GPIOs (GPIO1 to GPIO4) can be used to latch one of the two EDOs high or low. The ADT7462 has two EDO event mask registers (0x37 and 0x38): one mask for each EDO. See Table 33 for an explanation of event mask register functionality.

The polarity of the EDOs is set in the GPIO configuration registers (0x09 and 0x0A).

Setting a polarity bit to 1 in one of the GPIO configuration registers makes the corresponding GPIO pin active high. Clearing the polarity bit to 0 makes it active low.





Bits [7:5] of each event mask register (0x37 and 0x38) allow the EDO output to be driven high or low (depending on the polarity bit of the configuration register) and latched (depending on the EDO latch bit of the configuration register), if the ADT7462 detects an overtemperature, an over/undervoltage, or a fan failure condition.

Table 33. EDO CONTROL (MASK) REGISTER 0X37 AND REGISTER 0X38

Bit 7: Overvoltage/ Undervoltage	Bit 6: THERM	Bit 5: Fan Fail	Bit 3	Bit 2	Bit 1	Bit 0	Behavior: What Drives and Latches Output X (G = GPIO)
0 = Drive Output X	0 = Drive Output X	0 = Drive Output X	0	0	0	0	G4 or G3 or G2 or G1
1 = Ignore Event	1 = Ignore Event	1 = Ignore Event	0	0	0	1	G4 or G3 or G2
			0	0	1	0	G4 or G3 or G1
			0	0	1	1	G4 or G3
			0	1			

VR_HOT Inputs

Pin 25 and Pin 26 can be configured as VR_HOT inputs. These are specific digital signals from the CPU voltage regulator that indicate an overtemperature. On assertion of these inputs, the relevant status bits are set in Thermal Status Register 2 (Host Register 0xB9 or BMC Register 0xC1). Assertion of these inputs can also be used to boost the fans to full speed, thus providing emergency cooling in the event of VR overtemperature. This is set using Bit 3 (VRD1) and Bit 4 (VRD2) of Configuration Register 0x31 to mask the assertion of these inputs from the ALERT output.

SCSI_TERM Inputs

Pin 16 and Pin 20 can be configured as SCSI_TERM inputs. An assertion on the SCSI_TERM is recorded in Bit 4 and Bit 5 of Host Digital Status Register (0xBE) or BMC Digital Status Register (0xC6). There is also an associated mask bit in Register 0x35 to mask the assertion of these inputs from the <u>ALERT</u> output.

Reset I/O

The ADT7462 includes an active low reset pin (Pin 14). The RESET pin can be both a reset input and output. RESET monitors the V_{CC} input to the ADT7462. At powerup, RESET is asserted (pulled low) until 180 ms after the power supply has risen above the supply threshold. A power-on reset initializes all registers to the default values.

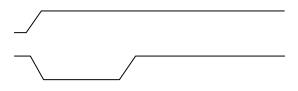


Figure 85. Operation of RESET Output on Powerup

Switching on the V_{CCP1} rail gates the fan's quiet startup counter.

- 3. V_{BATT} is monitored immediately on powerup before the setup complete bit (Register 0x01, Bit 5) is set. The chassis intrusion circuit (CI) is powered from V_{BATT} . If the measured V_{BATT} reading is lower than the lower limit (default = 0x80), the CI circuit is turned off.
- 4. PWM1, PWM2, and PWM4 are not on dedicated pins. Because these pins are shared with inputs, they are allowed to float high on powerup. This means that if a fan is connected to these pins, it spins at full speed on powerup.
- PWM3 is switched off by default (because this is a dedicated pin). If no SMBus communication takes place within 4.6 seconds of the V_{CCP} rail switching on, this PWM drive is driven to full speed. If SMBus communication does take place, this pin behaves as programmed.
- 6. No temperature or voltage (other than V_{CCP1} , Diode 2, and V_{BATT}) is monitored until the setup complete bit (Bit 5) is set in Configuration Register 1 (0x01). This allows the user to program the ADT7462 as required before monitoring of all channels is enabled, thereby not generating false ALERTs. The setup complete bit should not be set

until the device is fully configured for the desired monitoring functions.

The following steps describe how to set up the ADT7462:

- 1. Powerup the device.
- 2. Choose the best-suited easy configuration option for the application, changing pin functions as required.
- 3. Program all appropriate limits for monitored inputs. Program device parameters, fan control parameters, mask bits, and anything else required for the application.
- 4. Set the setup complete bit. Do not set this bit until the device is fully set up.

XOR Tree Test

The ADT7462 includes an XOR tree test mode. This mode is useful for in-circuit test equipment at board-level testing. By applying stimulus to the pins included in the XOR test, it is possible to detect opens or shorts on the system board. Figure 86 shows the signals exercised in the XOR tree test. The XOR tree test is invoked by setting Bit 6 (XOR) of Configuration Register 3 (0x03).

Note that the digital inputs must be selected on multifunctional pins for the XOR tree test mode. Pin 13 is the open-drain output of the XOR tree test.

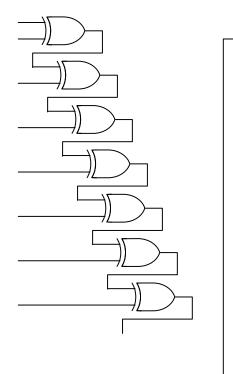


Figure 86. XOR Tree Test

Register Tables

Table 34. REGISTER MAP

Addr	Description	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De- fault	SW Reset	Lock able
0x00	Config 0	R/W	SW ResetR/	WR/W									

3it 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De- fault	SW Reset	Lock able
5	4	3	2	1	0	0x80	Yes	Yes
5	4	3	2	1	0	0x80	Yes	Yes
5	4	3	2	1	0	0x80	Yes	Yes
5	4	3	2	1	0	0x80	Yes	Yes
5	4	3	2	1	0	0xC0	Yes	Yes
R1D	R3	R2	R1	Local0				

Table 34. REGISTER MAP

Addr	Description	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De- fault	SW Reset	Lock able
0x50	Local THERM2/ +1.5V1 (ICH) High	R/W	7	6	5	4	3	2	1	0	0xA4	No	Yes
0x51	Remote 1 THERM2 Limit	R/W	7	6	5	4	3	2	1	0	0xA4	No	Yes
0x52	Remote 2 THERM2 Limit	R/W	7	6	5	4	3	2	1	0	0xA4	No	Yes
0x53	Remote 3 THERM2 Limit	R/W	7	6	5	4	3	2	1	0	0xA4	No	Yes
0x54	Local/Re- mote1 Temp Hyst	R/W	LH	LH	LH	LH	R1H	R1H	R1H	R1H	0x44	No	Yes
0x55	Remote 2/ Remote 3 Temp Hyst	R/W	R2H	R2H	R2H	R2H	R3H	R3H	R3H	R3H	0x44	No	Yes
0x56	Local Offset	R/W	7	6	5	4	3	2	1	0	0x00	No	Yes
0x57	Remote 1 Offset	R/W	7	6	5	4	3	2	1	0	0x00	No	Yes
0x58	Remote 2 Offset	R/W	7	6	5	4	3	2	1	0	0x00	No	Yes
0x59	Remote 3 Offset	R/W	7	6	5	4	3	2	1	0	0x00	No	Yes
0x5A	Remote 1 Operating Point	R/W	7	6	5	4	3	2	1	0	0xA4	Yes	Yes
0x5B	Remote 2 Operating Point	R/W	7	6	5	4	3	2	1	0	0xA4	Yes	Yes
0x5C	Local Temp T _{MIN}	R/W	7	6	5	4	3	2	1	0	0x9A	Yes	Yes
0x5D	Remote 1 Temp T _{MIN}	R/W	7	6	5	4	3	2	1	0	0x9A	Yes	Yes
0x5E	Remote 2 Temp T _{MIN}	R/W	7	6	5	4	3	2	1	0	0x9A	Yes	Yes
0x5F	Remote 3 Temp T _{MIN}	R/W	7	6	5	4	3	2	1	0	0x9A	Yes	Yes
0x60	Local T _{RANGE} / Hyst	R/W	Range	Range	Range	Range	Hys	Hys	Hys	Hys	0xC4	Yes	Yes
0x61	Remote 1 T _{RANGE} / Hyst	R/W	Range	Range	Range	Range	Hys	Hys	Hys	Hys	0xC4	Yes	Yes
0x62	Remote 2 T _{RANGE} / Hyst	R/W	Range	Range	Range	Range	Hys	Hys	Hys	Hys	0xC4	Yes	Yes
0x63	Remote 3 T _{RANGE} / Hyst	R/W	Range	Range	Range	Range	Hys	Hys	Hys	Hys	0xC4	Yes	Yes
0x64	Operating Point Hyst	R/W	Hys	Hys	Hys	Hys	Res	-			-		

Table 34. REGISTER MAP

Addr	Description	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De- fault	SW Reset	Loci able
0xA4	TACH6 Value, LSB	R	7	6	5	4	3	2	1	0	0xFF	No	No
0xA5	TACH6 MSB/+12V 2 Voltage	R	7	6	5	4	3	2	1	0	0xFF	No	No
0xA6	TACH7 Value, LSB	R	7	6	5	4	3	2	1	0	0xFF	No	No
0xA7	TACH7 MSB/+5V Voltage	R	7	6	5	4	3	2	1	0	0xFF	No	No
0xA8	TACH8 Value, LSB	R	7	6	5	4	3	2	1	0	0xFF	No	No
0xA9	TACH8 MSB/+12V 3 Voltage	R	7	6	5	4	3	2	1	0	0xFF	No	No
0xAA	PWM1 Duty Cycle	R/W	7	6	5	4	3	2	1	0	0x00	No	No
0xAB	PWM2 Duty Cycle	R/W	7	6	5	4	3	2	1	0	0x00	No	No
0xAC	PWM3 Duty Cycle	R/W	7	6	5	4	3	2	1	0	0xC0	No	No
0xAD	PWM4 Duty Cycle	R/W	7	6	5	4	3	2	1	0	0x00	No	No
0xAE	THERM1 %On–Time	R	7	6	5	4	3	2	1	0	0x00	No	No
0xAF	THERM2 %On–Time	R	7	6	5	4	3	2	1	0	0x00	No	No
0xB8	Thermal Status 1, Host	R	R3D	R2D	R1D	R3	R2	R1	Local	Res	0x00	Yes	No
0xB9	Thermal Status 2, Host	R	VR2	VR1	T2S	T2A	T2%	T1S	T1A	T1%	0x00	Yes	No
0xBA	Thermal Status 3, Host	R	R3T2	R2T2	R1T2	LT2	R3T1	R2T1	R1T1	LT1	0x00	Yes	No
0xBB	Voltage Status 1, Host	R	Pin 23	+5V	Pin 19	Pin 15	+3.3V	+12V3	+12V2	+12V1	0x00	Yes	No
0xBC	Voltage Status 2, Host	R	+1.5V1 (ICH)	+1.5V2 (3GIO)	Pin 26	Pin 25	Pin 24	Res	Res	Res	0x00	Yes	No
0xBD	Fan Status, Host	R	Fan 8	Fan 7	Fan 6	Fan 5	Fan 4	Fan 3	Fan 2	Fan 1	0x00	Yes	No
0xBE	Digital Status, Host	R	CI	VID	SCSI2	SCSI1	FAN2MAX	Res	Res	Res	0x00	Yes	No
0xBF	GPIO Status, Host	R/W	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	0x00	Yes	No
0xC0	Thermal Status 1, BMC	R	R3D	R2D	R1D	R3	R2	R1	Local	Res	0x00	Yes	No
0xC1	Thermal Status 2, BMC	R	VR2	VR1	T2S	T2A	T2%	T1S	T1A	T1%	0x00	Yes	No
0xC3	Voltage Status 1, BMC	R	Pin 23	+5V	Pin 19	Pin 15	+3.3V						•

Table 34. REGISTER MAP

Addr

De-	SW	Lock
fault	Reset	able

Table 41. REGISTER 0X09 - GPIO CONFIGURATION REGISTER 1 (Note 1)

Bit	Name	R/W	Description
0	GPIO1_P	R/W	This bit sets the polarity of GPIO1. 0 = Default = Active Low. 1= Active High.
1	GPIO1_D	R/W	This bit sets the direction of GPIO1. 0 = Default = Input. 1= Output.
2	GPIO2_P	R/W	This bit sets the polarity of GPIO2. 0 = Default = Active low. 1= Active High.
3	GPIO2_D	R/W	This bit sets the direction of GPIO2. 0 = Default = Input. 1= Output.
4	GPIO3_P	R/W	This bit sets the polarity of GPIO3. 0 = Default = Active Low. 1= Active High.
5	GPIO3_D	R/W	This bit sets the direction of GPIO3. 0 = Default = Input. 1= Output.
6	GPIO4_P	R/W	This bit sets the polarity of GPIO4. 0 = Default = Active Low. 1= Active High.
7	GPIO4_D	R/W	This bit sets the direction of GPIO4. 0 = Default = Input. 1= Output.

1. POR = 0x00, Lock = Y, SW Reset = Y.

Table 42. REGISTER 0X0A - GPIO CONFIGURATION REGISTER 2 (Note 1)

Bit	Name	R/W	Description
0	GPIO5_P	R/W	This bit sets the polarity of GPIO5. 0 = Default = Active Low. 1= Active High.
1	GPIO5_D	R/W	This bit sets the direction of GPIO5. 0 = Default = Input. 1= Output.
2	GPIO6_P	R/W	This bit sets the polarity of GPIO6. 0 = Default = Active Low. 1= Active High.
3	GPIO6_D	R/W	This bit sets the direction of GPIO6. 0 = Default = Input. 1= Output.
4	GPIO7_P	R/W	This bit sets the polarity of GPIO7. 0 = Default = Active Low. 1= Active High.
5	GPIO7_D	R/W	This bit sets the direction of GPIO7. 0 = Default = Input. 1= Output.
6	GPIO8_P	R/W	This bit sets the polarity of GPIO8. 0 = Default = Active Low. 1= Active High.
7	GPIO8_D	R/W	This bit sets the direction of GPIO8. 0 = Default = Input. 1= Output.

1. POR = 0x00, Lock = Y, SW Reset = Y.

Table 43. REGISTER 0X0B – DYNAMIC T_{MIN} CONTROL REGISTER 1 (Note 1)

Bit	Name	R/W	Description
0	Remote 1 En	R/W	Setting this bit to 1 enables dynamic T_{MIN} control for the Remote 1 channel. Default = 0.
1	Remote 2 En	R/W	Setting this bit to 1 enables dynamic T_{MIN} control for the Remote 2 channel. Default = 0.
2	P1R1	R/W	P1R1 = 1 copies the Remote 1 current temperature to the Remote 1 operating point register if THERM1 is asserted externally. This happens only if the current temperature is less than the value in the operating point register. The operating point contains the temperature at which THERM1 is asserted. P1R1 = 0 (Default) ignores any THERM1 assertions on the THERM1 pin. The Remote 1 operating point register reflects its programmed value.
3	P1R2	R/W	P1R2 = 1 copies the Remote 2 current temperature to the Remote 2 operating point register if THERM1 is asserted externally. This happens only if the current temperature is less than the value in the operating point register. The operating point contains the temperature at which THERM1 is asserted. P1R2 = 0 (Default) ignores any THERM1 assertions on the THERM1 pin. The Remote 2 operating point register reflects its programmed value.

Table 46. REGISTER 0X0E - THERM1 CONFIGURATION REGISTER (Note 1)

Bit	Name	R/W	Description
0	THERM1 Timer Enable	R/W	Enables the $\overline{\text{THERM1}}$ timer circuit. Default = 0.
1	THERM1_Local	R/W	Setting the bit to 1 means that the THERM1 pin is asserted low as an output whenever the local temperature exceeds the local THERM1 temperature limit. Default = 0.
2	THERM1_ Remote 1	R/W	Setting the bit to 1 means that the THERM1 pin is asserted low as an output whenever the Remote 1 temperature exceeds the Remote 1 THERM1 temperature limit. Default = 0.
3	THERM1_ Remote 2	R/W	Setting the bit to 1 means that the THERM1 pin is asserted low as an output whenever the Remote 2 temperature exceeds the Remote 2 THERM1 temperature limit. Default = 0.
4	THERM1_ Remote 3	R/W	Setting the bit to 1 means that the THERM1 pin is asserted low as an output whenever the Remote 3 temperature exceeds the Remote 3 THERM1 temperature limit. Default = 0.
[7:5]	Reserved	R	Reserved for future use.

1. POR = 0x00, Lock = Y, SW Reset = Y.

Table 47. REGISTER 0X0F - THERM2 CONFIGURATION REGISTER (Note 1)

Bit	Name	R/W	Description
0	THERM2 Timer Enable	R/W	Enables the $\overline{\text{THERM2}}$ timer circuit. Default = 0.
1	THERM2_Local	R/W	Setting the bit to 1 means that the THERM2 pin is asserted low as an output whenever the local temperature exceeds the local THERM2 temperature limit. Default = 0.
2	THERM2_ Remote 1	R/W	Setting the bit to 1 means that the THERM2 pin is asserted low as an output whenever the Remote 1 temperature exceeds the Remote 1 THERM2 temperature limit. Default = 0.
3	THERM2_ Remote 2	R/W	Setting the bit to 1 means that the THERM2 pin is asserted low as an output whenever the Remote 2 temperature exceeds the Remote 2 THERM2 temperature limit. Default = 0.
4	THERM2_ Remote 3	R/W	Setting the bit to 1 means that the THERM2 pin is asserted low as an output whenever the Remote 3 temperature exceeds the Remote 3 THERM2 temperature limit. Default = 0.
[7:5]	Reserved	R	Reserved for future use.

1. POR = 0x00, Lock = Y, SW Reset = Y.

Table 48. REGISTER 0X10 - PIN CONFIGURATION REGISTER 1 (Note 1)

Bit	Name	R/W	Description	
0	Pin 7	R/W	0 = +12V1; 1 = TACH5 Input. Default = 1.	
1	Pin 4	R/W	0 = GPIO4; 1= TACH4 Input (that is, if the VIDs are not selected). Default = 1.	
2	Pin 3	R/W	0 = GPIO3; 1= TACH3 Input (that is, if the VIDs are not selected). Default = 1.	
3	Pin 2	R/W	0 = GPIO2; 1= TACH2 Input (that is, if the VIDs are not selected). Default = 1.	
4	Pin 1	R/W	0 = GPIO1; 1= TACH1 Input (that is, if the VIDs are not selected). Default = 1.	
5	Diode 3	R/W	1 enables the D3+ and D3– inputs on Pin 19 and Pin 20. 0 enables the voltage measurement input and SCSI_TERM2 input. Default = 1.	
6	Diode 1	R/W	1 enables the D1+ and D1– inputs on Pin 15 and Pin 16. 0 enables the voltage measurement input and SCSI_TERM1 input. Default = 1.	
7	VIDs	R/W	Setting this bit to 1 enables the VIDs on Pin 1 to Pin 4, Pin 28, Pin 31, and Pin 32. Default = 0.	

1. POR = 0x7F, Lock = Y, SW Reset = Y.

Table 52. REGISTER 0X14 – EASY CONFIGURATION OPTIONS (Note 1)

Bit	Name	R/W	Description
0	Easy Option 1 Select	R/W	Setting this bit to 1 enables Easy Option 1.
1	Easy Option 2 Select	R/W	Setting this bit to 1 enables Easy Option 2.
2	Easy Option 3 Select	R/W	Setting this bit to 1 enables Easy Option 3.
3	Easy Option 4 Select	R/W	Setting this bit to 1 enables Easy Option 4.
4	Easy Option 5 Select	R/W	Setting this bit to 1 enables Easy Option 5.
[7:5]	Reserved	R	Reserved for future use.

1. POR = 0x01, Lock = Y, SW Reset = Y.

Table 53. REGISTER 0X16 - EDO/SINGLE CHANNEL ENABLE (Note 1)

Bit	Name	R/W	Description
0	EDO_En1	R/W	Enable EDO on GPIO5. Default = 0.
1	EDO_En2	R/W	Enable EDO on GPIO6. Default = 0.
2	Single–Channel Mode Select	R/W	Setting this bit to 1 places the ADT7462 in single-channel mode. This means that it converts on one channel only. The channel it converts on is set using the channel select bits in this register. Default = 0.
[7:3]	Channel Select	R/W	

Table 56. REGISTER 0X1A -

Table 59. REGISTER 0X1D -

Table 62. REGISTER 0X21, REGISTER 0X22, REGISTER 0X23, REGISTER 0X24 – PWM1, PWM2, PWM3AND PWM4 CONFIGURATION REGISTERS

Bit	Name	R/W	Description	
[2:0]	Spin-Up Timeout	R/W	These bits set the duration of the fan startup timeout and the timeout for the fan freewheeling test. 000 = No Startup Timeout 001 = 100 ms 010 = 250 ms 011 = 400 ms 100 = 667 ms 101 = 1 sec 110 = 2 sec 111 = 32 sec	
3	SLOW	R/W	Setting this bit to 1 makes the ramp rate of the enhance acoustics mode four times longer.	
4	INV	R/W	Setting this bit to 0, the PWM outputs are active low. Setting this bit to 1, the PWM outputs are active high (Default).	
[7:5]	BHVR	R/W	These bits determine which temperature channel controls the fans in the automatic fan speed control loop. 000 = Local Temperature 001 = Remote 1 Temperature 010 = Remote 2 Temperature 011 = Remote 3 Temperature 100 = Off 101 = Maximum Fan Speed Calculated by the Local and Remote 3 TC3 Maxip	

Table 64. REGISTER 0X26

Bit	Name	R/W	Description	
[2:0]	Reserved	R	Reserved for future use.	
3	FAN2MAX	R/W	1 masks ALERTs for the corresponding interrupt status bit. Default = 1.	
4	SCSI1	R/W	1 masks ALERTs for the corresponding interrupt status bit. Default = 1.	
5	SCSI2	R/W	1 masks ALERTs for the corresponding interrupt status bit. Default = 1.	
6	VID Comparison	R/W	1 masks ALERT	

Table 72. REGISTER 0X35 – DIGITAL MASK REGISTER (Note 1)

Table 76. REGISTER 0X3D – DEVICE ID REGISTER (Note 1)

Bit	Name	R/W	Description
[7:0]	Device ID	R	This register contains the device ID (0x62) for the ADT7462.

1. POR = 0x62, SW Reset = N.

Table 77. REGISTER 0X3E – COMPANY ID REGISTER (Note 1)

Bit	Name	R/W	Description			
[7:0]	Company ID	R	This register contains the company ID (0x41) for the ADT7462.			
	POD 0v41 SWI Prost N					

1. POR = 0x41, SW Reset = N.

Table 78. REGISTER 0X3F - REVISION REGISTER (Note 1)

Bit	Name	R/W	Description		
[7:0]	Revision ID	R	This register contains the revision ID (0x04) for the ADT7462.		

1. POR = 0x04, SW Reset = N.

Table 79. TEMPERATURE LIMIT REGISTERS (Note 1)

Register Address R/W

Description

Table 81. REGISTER 0X55 - REMOTE 2/REMOTE 3 TEMPERATURE HYSTERESIS (Note 1)

Bit	Name	R/W	Description	
[3:0]	Remote 3 Hysteresis	R/W	These four bits set the Remote 3 THERM hysteresis value, 1 LSB = 1°C.	
[7:4]	Remote 2 Hysteresis	R/W	These four bits set the Remote 2 THERM hysteresis value, 1 LSB = 1°C. $0000 = 0^{\circ}$ C $0001 = 1^{\circ}$ C $0010 = 2^{\circ}$ C $0011 = 3^{\circ}$ C $0100 = 4^{\circ}$ C (Default) $0101 = 5^{\circ}$ C $0110 = 6^{\circ}$ C $0111 = 7^{\circ}$ C $1000 = 8^{\circ}$ C $1001 = 9^{\circ}$ C $1010 = 10^{\circ}$ C $1011 = 11^{\circ}$ C $1100 = 12^{\circ}$ C $1101 = 13^{\circ}$ C $1110 = 14^{\circ}$ C $1111 = 15^{\circ}$ C	

1. POR = 0x44, Lock = Y, SW Reset = N.

Table 82. OFFSET REGISTERS (Note 1)

Register Address	R/W	Description	POR Default
0x56	R/W	Local offset, resolution = 0.5° C.	0x00
0x57	R/W	Remote 1 offset, resolution = 0.5° C.	0x00
0x58	R/W	Remote 2 offset, resolution = 0.5° C.	0x00
0x59	R/W	Remote 3 offset, resolution = 0.5° C.	0x00

1. Lock = Y, SW Reset = N.

Table 83. OPERATING POINT REGISTERS (Note 1)

Register Address	R/W	Description	POR Default
0x5A	R/W	Remote 1 operating point.	0xA4
0x5B	R/W	Remote 2 operating point.	0xA4

1. Lock = Y, SW Reset = Y.

Table 84. TIMING REGISTERS (Note 1)

Register Address	R/W	Description	POR Default
0x5C	R/W	Local temperature T _{MIN} .	0x9A
0x5D	R/W	Remote 1 temperature T _{MIN} .	0x9A
0x5E	R/W	Remote 2 temperature T _{MIN} .	0x9A
0x5F	R/W	Remote 3 temperature T _{MIN} .	0x9A

1. Lock = Y, SW Reset = Y.

Table 85. T_{RANGE}/HYSTERESIS REGISTERS (Note 1)

Register Address	R/W	Description	POR Default
0x60	R/W	Local T _{RANGE} /Hysteresis	0xC4
0x61	R/W	Remote 1 T _{RANGE} /Hysteresis	0xC4
0x62	R/W	Remote 2 T _{RANGE} /Hysteresis	0xC4
0x63	R/W	Remote 3 T _{RANGE} /Hysteresis	0xC4

1. Lock = Y, SW Reset = Y.

Table 89. TACH LIMIT REGISTERS (Note 1)

Register Address	R/W	Description	POR Default
0x78	R/W	TACH1 limit/VID limit.	0xFF
0x79	R/W	TACH2 limit.	0xFF
0x7A	R/W	TACH3 limit.	0xFF
0x7B	R/W	TACH4 limit.	0xFF
0x7C	R/W	TACH5 limit/+12V1 voltage high limit.	0xFF
0x7D	R/W	TACH6 limit/+12V2 voltage high limit.	0xFF
0x7E	R/W	TACH7 limit/+5V voltage high limit.	0xFF
0x7F	R/W	TACH8 limit/+12V3 voltage high limit.	0xFF

1. Lock = Y, SW Reset = N.

Table 90. THERM TIMER LIMIT REGISTERS (Note 1)

Register Address	R/W	Description	POR Default
0x80	R/W	THERM1 Timer Limit.	0xFF
0x81	R/W	THERM2 Timer Limit.	0xFF

1. Lock = Y, SW Reset = N.

Table 91. TEMPERATURE VALUE REGISTERS (Note 1)

Register Address	R/W	Description	POR Default		
0x8Tm(R/W)TjET1.272 527.187 23Res9688 0 8 192.8126 654.7.403 461.v13 538.129 32.8215ult					

Register Address	R/W	Description	POR Default
0x98	R	TACH1, LSB.	0xFF
0x99	R	TACH1, MSB.	0xFF
0x9A	R	TACH2, LSB.	0xFF
0x9B	R	TACH2, MSB.	0xFF
0x9C	R	TACH3, LSB.	0xFF
0x9D	R	TACH3, MSB.	0xFF
0x9E	R	TACH4, LSB.	0xFF
0x9F	R	TACH4, MSB.	0xFF
0xA2	R	TACH5, LSB.	0xFF
0xA3	R		

Table 94. TACH VALUE REGISTERS (Note 1)

Table 98. REGISTER 0XB9 – HOST THERMAL STATUS REGISTER 2 (Note 1); REGISTER 0XC1 – BMC THERMAL STATUS REGISTER 2 (Note 1)

Bit	Name	R/W	Description	
0	THERM1 %	R	A 1 indicates that THERM1 has been asserted for longer than the programmed THERM1 timer limit.	
1	THERM1 Assert	R	A 1 indicates that THERM1 is asserted.	
2	THERM1 State	R	A 1 indicates that a transition from high to low has taken place on the THERM1 pin.	
3	THERM2 %	R	A 1 indicates that THERM2 has been asserted for longer than the programmed THERM2 timer limit.	
4	THERM2 Assert	R	A 1 indicates that THERM2 is asserted.	
5	THERM2 State	R	A 1 indicates that a transition from high to low has taken place on the THERM2 pin.	
6	VRD1_Assert	R	A 1 indicates that VRD1 is asserted.	
7	VRD2_Assert	R	A 1 indicates that VRD2 is asserted.	

1. POR = 0x00, Lock = N, SW Reset = Y.

Table 99. REGISTER 0XBA - HOST THERMAL STATUS REGISTER 3 (Note 1)

Bit	Name	R/W	Description	
0	Local THERM1	R	A 1 indicates that the local THERM1 limit has been exceeded.	
1	Remote 1 THERM1	R	A 1 indicates that the Remote 1 THERM1 limit has been exceeded.	
2	Remote 2 THERM1	R	A 1 indicates that the Remote 2 THERM1 limit has been exceeded.	
3	Remote 3 THERM1	R	A 1 indicates that the Remote 3 THERM1 limit has been exceeded.	
4	Local THERM2	R	A 1 indicates that the Local THERM2 limit has been exceeded.	
5	Remote 1 THERM2	R	A 1 indicates that the Remote 1 THERM2 limit has been exceeded.	
6	Remote 2 THERM2	R	A 1 indicates that the Remote 2 THERM2 limit has been exceeded.	
7	Remote 3 THERM2	R	A 1 indicates that the Remote 3 THERM2 limit has been exceeded.	

1. POR = 0x00, Lock = N, SW Reset = Y.

Table 100. REGISTER 0XBB – HOST VOLTAGE STATUS REGISTER 1 (Note 1); REGISTER 0XC3 – BMC VOLTAGE REGISTER 1 (Note 1)

Bit	Name	R/W	Description	
0	+12V1	R	A 1 indicates that a +12V1 voltage limit has been tripped.	
1	+12V2	R	A 1 indicates that a +12V2 voltage limit has been tripped.	
2	+12V3	R	A 1 indicates that a +12V3 voltage limit has been tripped.	
3	+3.3V	R	A 1 indicates that a +3.3V voltage limit has been tripped.	
4	Pin 15 Voltage	R	A 1 indicates that a Pin 15 voltage limit has been tripped.	
5	Pin 19 Voltage	R	A 1 indicates that a Pin 19 voltage limit has been tripped.	
6	+5V	R	A 1 indicates that a +5V voltage limit has been tripped.	
7	Pin 23 Voltage	R	A 1 indicates that a Pin 23 voltage limit has been tripped.	

1. POR = 0x00, Lock = N, SW Reset = Y.

Table 101. REGISTER 0XBC – HOST VOLTAGE STATUS REGISTER 2 (Note 1); REGISTER 0XC4 – BMC VOLTAGE STATUS REGISTER 2 (Note 1)

Bit	Name	R/W	Description	
[2:0]	Reserved	R	Reserved for future use.	
3	Pin 24 Voltage	R	A 1 indicates that a Pin 24 voltage limit has been tripped.	
4	Pin 25 Voltage	R	A 1 indicates that a Pin 25 voltage limit has been tripped.	
5	Pin 26 Voltage	R	A 1 indicates that a Pin 26 voltage limit has been tripped.	
6	+1.5V2 (3GIO)	R	A 1 indicates that a +1.5V2 (3GIO) voltage limit has been tripped.	
7	+1.5V1 (ICH)	R	A 1 indicates that a +1.5V1 (ICH) voltage limit has been tripped.	

1. POR = 0x00, Lock = N, SW Reset = Y.

Table 102. REGISTER 0XBD – HOST FAN STATUS REGISTER (Note 1); REGISTER 0XC5 – BMC FAN STATUS REGISTER (Note 1)

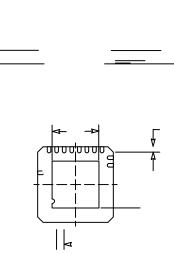
Bit	Name	R/W	Description	
0	Fan 1 Fault	R	A 1 indicates a Fan 1 fault.	
1	Fan 2 Fault	R	A 1 indicates a Fan 2 fault.	
2	Fan 3 Fault	R	A 1 indicates a Fan 3 fault.	
3	Fan 4 Fault	R	A 1 indicates a Fan 4 fault.	
4		-		

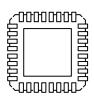
Table 105. ORDERING INFORMATION

Device Number*	Temperature Range	Temperature Range Package Type		Shipping [†]
ADT7462ACPZ-REEL	–40°C to +125°C	32-lead LFCSP_VQ	CP-32-2	5,000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*The "Z" suffix indicates Pb–Free part.

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