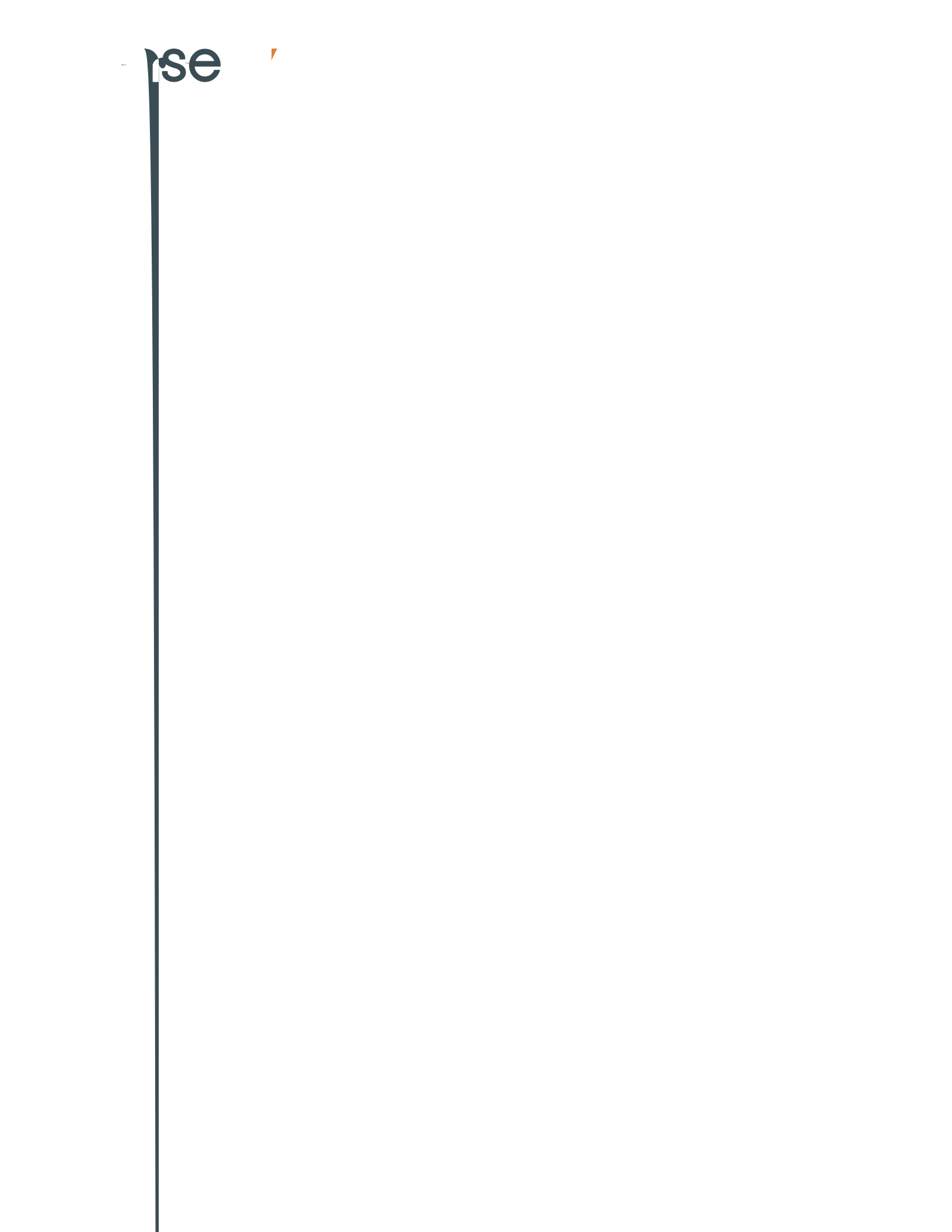

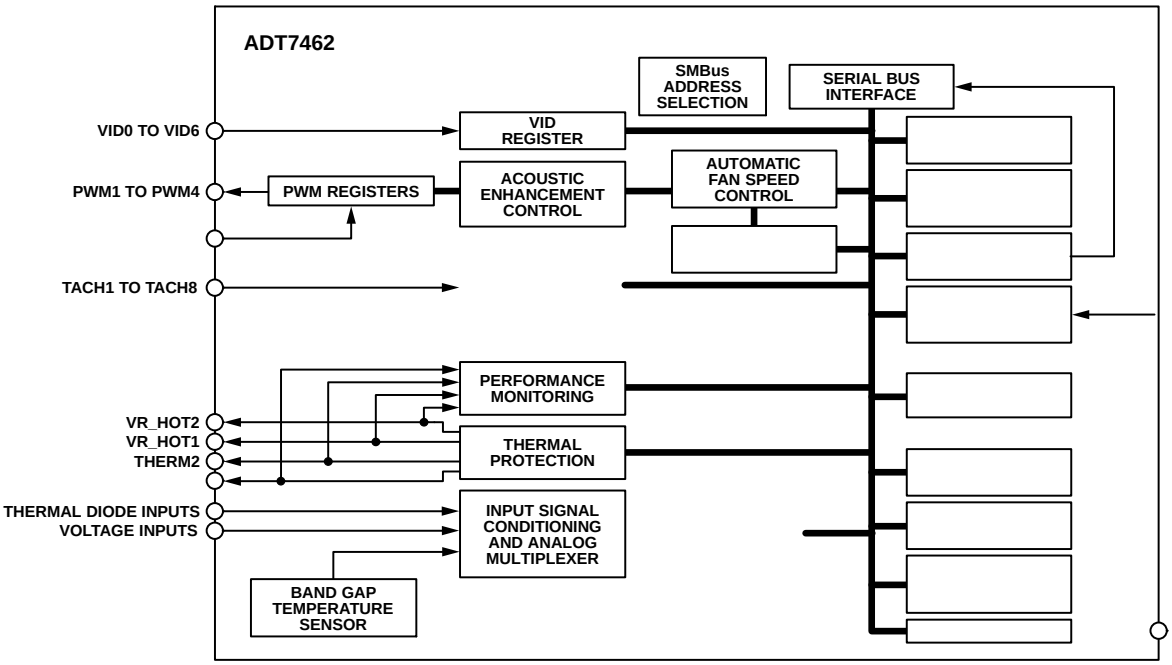


**Figure 1. Functional Block Diagram**

# ADT7462

# ADT7462

**Table 4. ELECTRICAL CHARACTERISTICS** ($T_A = T_{MIN}$ to $T_{MAX}$, $V_{CC} = V_{MIN}$ to $V_{MAX}$, unless otherwise noted.) (Note 1)

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Power Supply** | | | | | |
| Supply Voltage | | 3.0 | 3.3 | 5.5 | V |
| Supply Current, $I_{CC}$ | ADC Active, Interface Inactive (Note 2) | − | 1.5 | 4.0 | mA |

**Table 4. ELECTRICAL CHARACTERISTICS** ($T_A = T_{MIN}$ to $T_{MAX}$, $V_{CC} = V_{MIN}$ to $V_{MAX}$, unless otherwise noted.) (Note 1)

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OPEN-DRAIN SERIAL BUS OUTPUT (SDA)** | | | | | |
| Output Low Voltage, $V_{OL}$ | $I_{OUT}$ = −3 mA, $V_{CC}$ = +3.3 V | − | − | 0.4 | V |
| High Level Output Leakage Current, $I_{OH}$ | $V_{OUT} = V_{CC}$ | − | 0.1 | ±1.0 | μA |

## TYPICAL PERFORMANCE CHARACTERISTICS

Figure 3. Supply Current vs. Supply Voltage

Figure 4. Supply Current vs. Temperature

Figure 5. Local Sensor Temperature Error

Figure 6. Remote Sensor Temperature Error

Figure 7. Temperature Error Measuring Intel Pentium® 4 Processor

Figure 8. ADT7462 Response to Thermal Shock

## TYPICAL PERFORMANCE CHARACTERISTICS (CONT'D)

Figure 9. Remote Temperature Error vs. Resistance (SRC)

Figure 10. Local Temperature Error vs. Power Supply Noise Frequency

Figure 11. Remote Temperature Error vs. Power Supply Noise Frequency

Figure 12. Remote Temperature Error vs. Common-Mode Noise Frequency

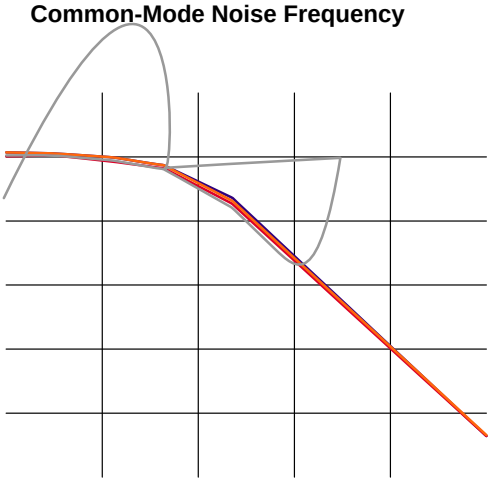

Figure 13. Remote Temperature Error vs. Differential-Mode Noise Frequency

Figure 14. Remote Temperature Error vs. Capacitance Between D+ and D−

## TYPICAL PERFORMANCE CHARACTERISTICS (CONT'D)

**Figure 15. Local Temperature vs. Power-On Reset Timeout**

**Figure 16. Applied Voltage vs. $V_{BATT}$ Reading**

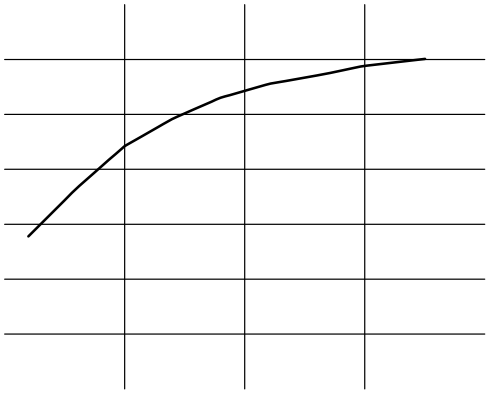

**Figure 17. TACH Accuracy vs. Supply Voltage**

**Figure 18. TACH Accuracy vs. Temperature**

## FUNCTION DESCRIPTION: EASY CONFIGURATION OPTIONS

**Table 5. EASY CONFIGURATION REGISTER SETTINGS**

| Easy Configuration Option | Register 0x14 Setting |
|---|---|
| Option 1 | Bit 0 = 1 |
| Option 2 | Bit 1 = 1 |
| Option 3 | Bit 2 = 1 |
| Option 4 | Bit 3 = 1 |
| Option 5 | Bit 4 = 1 |

### Configuration Option 1

- 
- 
- 
- 
- 

### Configuration Option 2

- 
- 
- 
- 
- 
- 

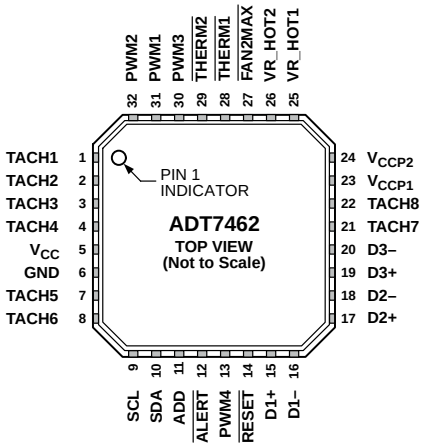


**Figure 20. Configuration Option 2**

**Table 7. CONFIGURATION OPTION 2**

| Pin | Function | Configuration Register | Bit Value |
|---|---|---|---|
| 1† | TACH1 | Pin Configuration Reg 1 | Bit 4 = 1 |
| 2† | TACH2 | Pin Configuration Reg 1 | Bit 3 = 1 |
| 3† | TACH3 | Pin Configuration Reg 1 | Bit 2 = 1 |
| 4† | TACH4 | Pin Configuration Reg 1 | Bit 1 = 1 |
| 7 | TACH5 | Pin Configuration Reg 1 | Bit 0 = 1 |

81 Tf10 0 0 10 69.8457 604.1198 Tm-.00344.385 0 = 1

**Configuration Option 4**

- 
- 

**Serial Bus Interface**

- 

SCL

SDA

A2

R/W

**Figure 24. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register**

# ADT7462

### SMBus Timeout

### Configuration Register 3 (0x03)

## TEMPERATURE AND VOLTAGE MEASUREMENT

### Temperature Measurement

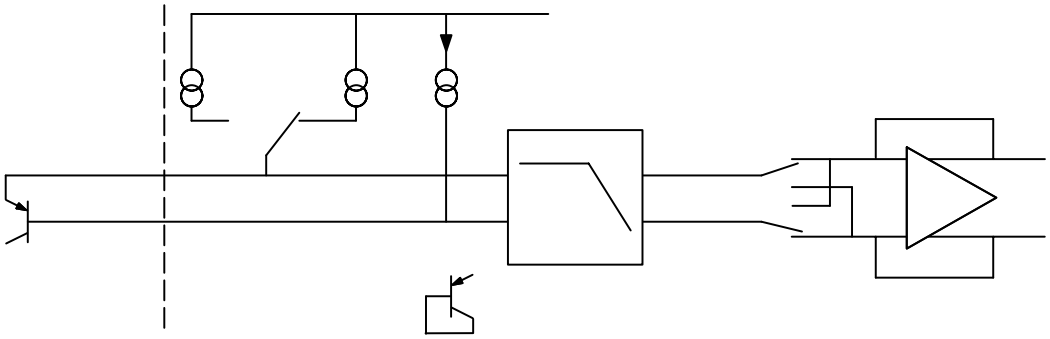

**Figure 33. Input Signal Conditioning**

**Noise Filtering**

–

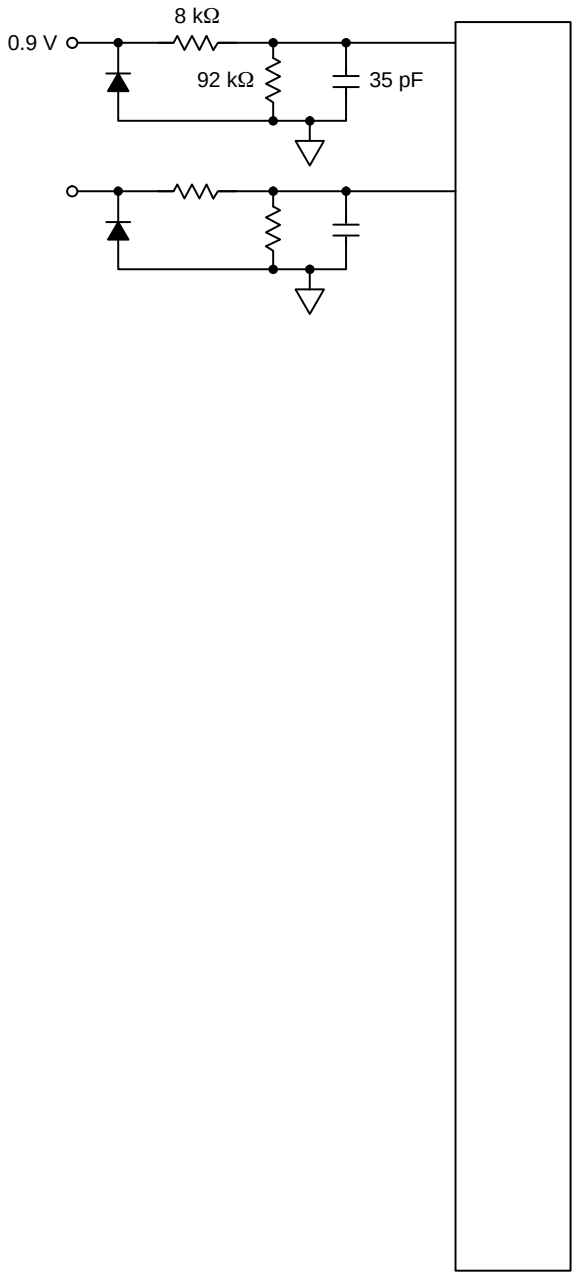


**Figure 36. Voltage Input Structures**

**Table 17. VOLTAGE VALUE AND LIMIT REGISTERS**

| Voltage Value | Pin No. | Value Register Address | Low Limit | | High Limit | |
|---|---|---|---|---|---|---|
| | | | Register | Default | Register | Default |
| +12V1 | 7 | 0xA3 | 0x6D | 0x00 | 0x7C | 0xFF |
| +12V2 | 8 | 0xA5 | 0x6E | 0x00 | 0x7D | 0xFF |
| +3.3V | 13 | 0x96 | 0x70 | 0x00 | 0x68 | 0xFF |
| +1.8V or +2.5V | 15 | 0x8B | 0x45 | 0x40 | 0x49 | 0x95 |
| +1.25V or +0.9V | 19 | 0x8F | 0x47 | 0x40 | 0x4B | 0x95 |
| +5V | 21 | 0xA7 | 0x71 | 0x00 | 0x7E | 0xFF |
| +12V3 | 22 | 0xA9 | 0x6F | 0x00 | 0x7F | 0xFF |
| $V_{CCP1}$, +1.5V, +1.8V, +2.5V | 23 | 0x90 | 0x72 | 0x20 | 0x69 | 0xFF |
| $V_{CCP2}$, +1.5V, +1.8V, +2.5V | 24 | 0x91 | 0x73 | 0x00 | 0x6A | 0xFF |
| +1.2V1 ($G_{BIT}$) or +3.3V | 25 | 0x92 | 0x74 | 0x00 | 0x6B | 0xFF |
| +1.2V2 (FSB_$V_{TT}$) or $V_{BATT}$ | 26 | 0x93 | 0x75 | 0x80 | 0x6C | 0xFF |
| +1.5V1 (ICH) | 28 | 0x94 | 0x77 | 0x00 | 0x50 | 0xA4 |
| +1.5V2 (3GIO) | 29 | 0x95 | 0x76 | 0x00 | 0x4C | 0xA4 |

# ADT7462

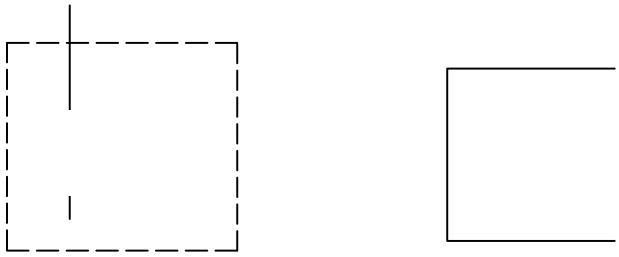

**Figure 45. Fan with Strong TACH. Pullup to > $V_{CC}$ or Totem-Pole Output, Clamped with Zener Diode and Resistor**

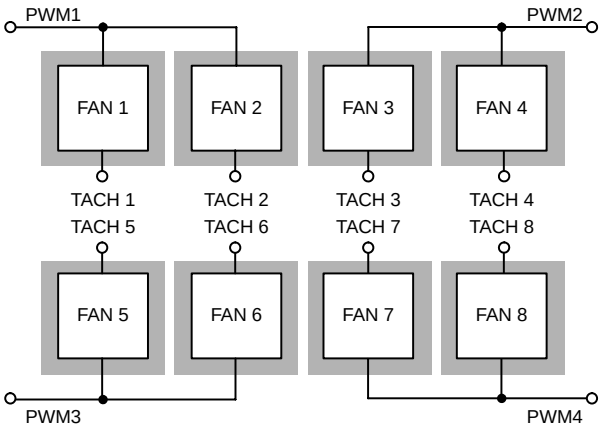


**Figure 48. Synchronizing Fan PWM Output and TACH Inputs**

**Driving and Measuring the Speed of One Fan from One PWM Output**

**Fan Speed Measurement Registers**

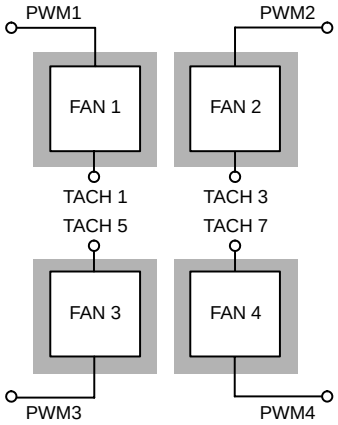


**Figure 49. Driving and Measuring the Speed on a Single Fan**

### Calculating Fan Speed

## Fan Speed Control

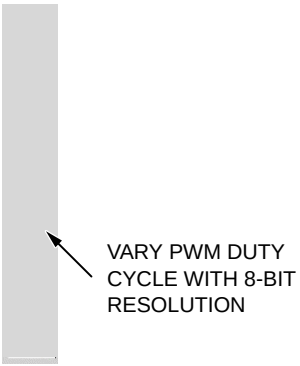


**Figure 50. Control PWM Duty Cycle Manually with a Resolution of 0.39%**

### Programming the Automatic Fan Speed Control Loop

### Programming the PWM Current Duty Cycle Registers

### Automatic Fan Control Overview

### PWM Duty Cycle Registers

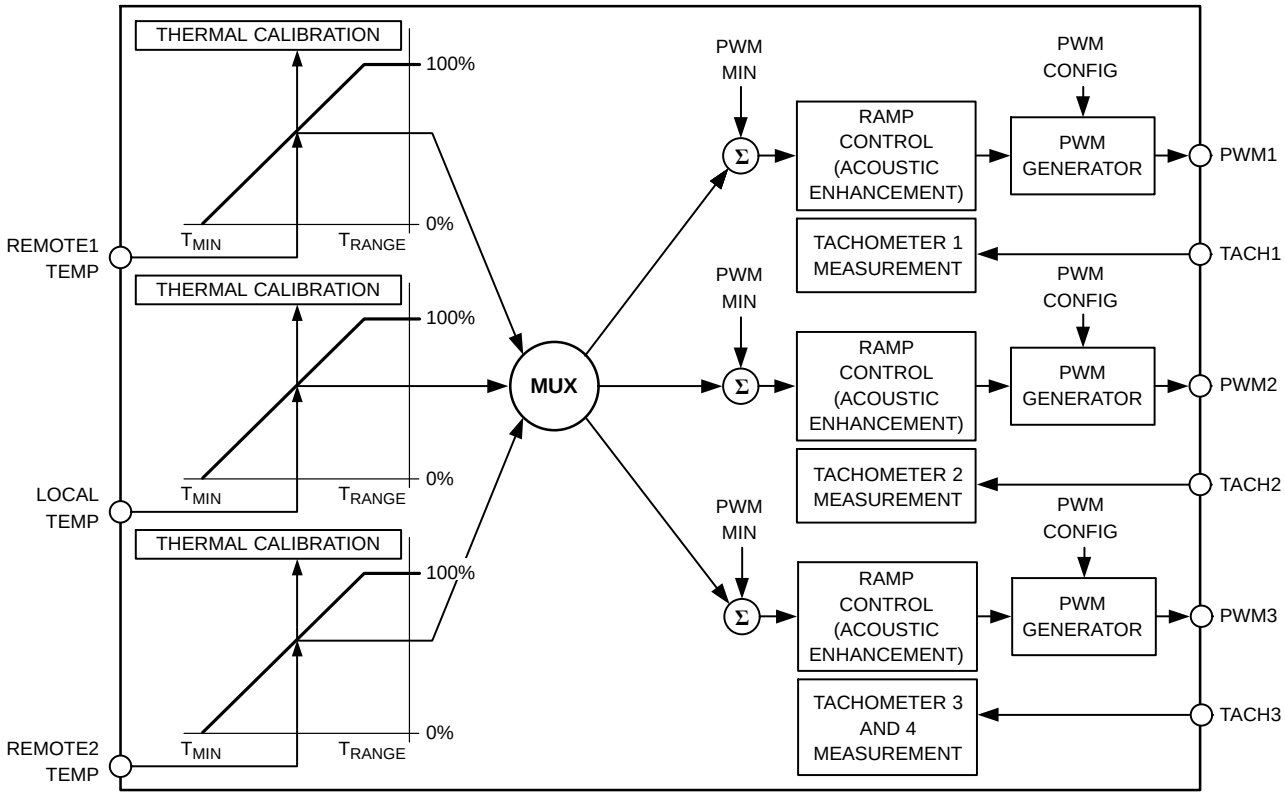


**Figure 51. Automatic Fan Control Block Diagram**

**Step 1 − Configuring the MUX**

### Step 2 − $T_{MIN}$ Settings for Thermal Calibration Channels

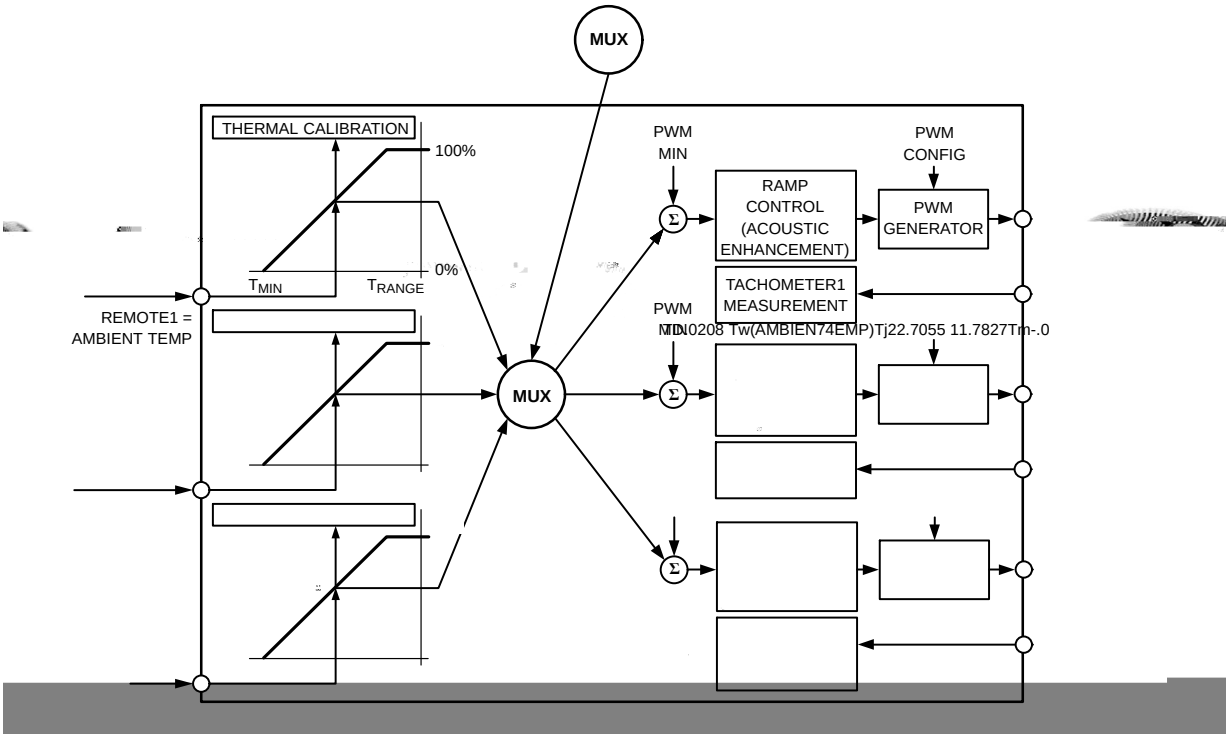


**Figure 52. Assigning Temperature Channels to Fan Channels**

### Programming the $PWM_{MIN}$ Registers

$PWM_{MIN}$MIN

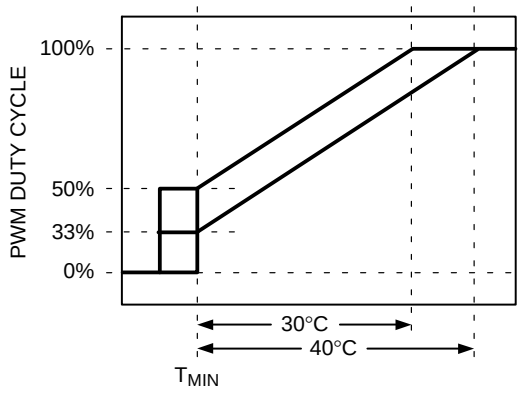


**Figure 58. Adjusting $PWM_{MIN}$ Affects $T_{RANGE}$**

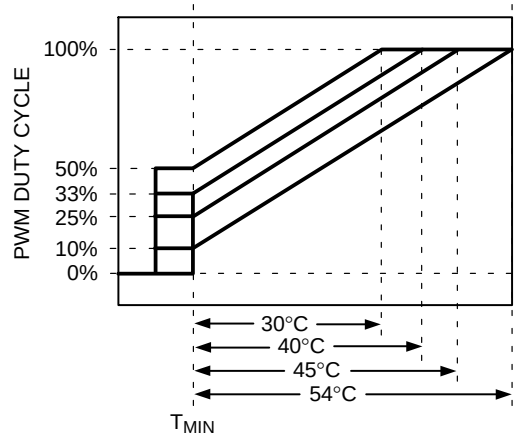


**Figure 59. Increasing $PWM_{MIN}$ Changes Effective $T_{RANGE}$**

$$T_{MAX} = T_{MIN} + (\text{Max DC} - \text{Min DC}) \times T_{RANGE}/170 \quad \text{(eq. 7)}$$

− ×

**Note on 4-wire Fans**

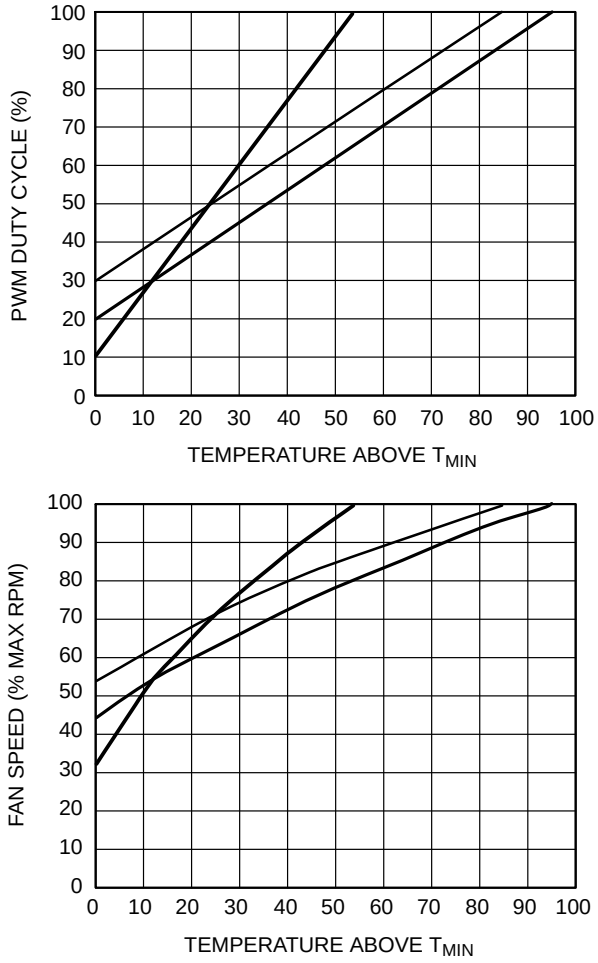


**Figure 62. $T_{RANGE}$ and % Fan Speed Slopes for VRM, Ambient, and CPU Temperature Channels**

**Step 6 − $T_{\overline{THERM}}$ for Temperature Channels**

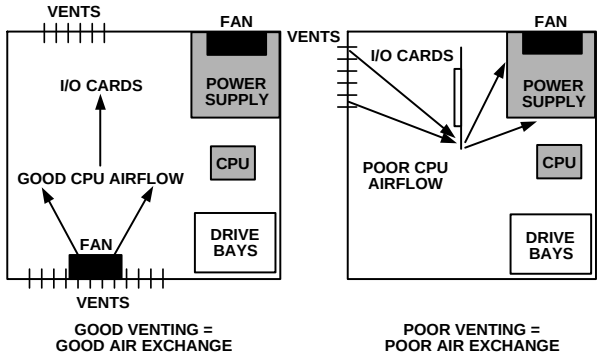


**Figure 65. Chassis Airflow Issues**

- 
- 
- 

**Table 28. $T_{MIN}$**

**Table 29. CYCLE BIT ASSIGNMENTS**

| Code | Short Cycle | Duration | Long Cycle | Duration |
|---|---|---|---|---|
| 000 | 8 cycles | 1 sec | 16 cycles | 2 sec |
| 001 | 16 cycles | 2 sec | 32 cycles | 4 sec |
| 010 | 32 cycles | 4 sec | 64 cycles | 8 sec |
| 011 | 64 cycles | 8 sec | 128 cycles | 16 sec |
| 100 | 128 cycles | 16 sec | 256 cycles | 32 sec |
| 101 | 256 cycles | 32 sec | 512 cycles | 64 sec |
| 110 | 512 cycles | 64 sec | 1024 cycles | 128 sec |
| 111 | 1024 cycles | 128 sec | | |

**Approaches to System Acoustic Enhancement**

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**Step 11 − Ramp Rate for Acoustic Enhancement**

**Enhanced Acoustics Register 1 (0x1A)**

s

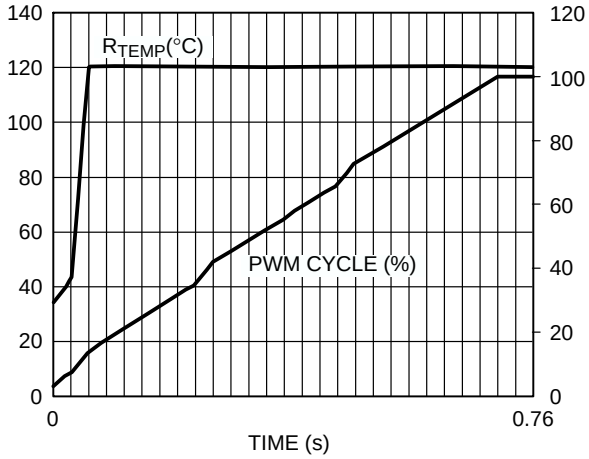


**Figure 77. Enhanced Acoustics Mode with Ramp Rate = 48**

**Enhanced Acoustics Register 2 (0x1B)**

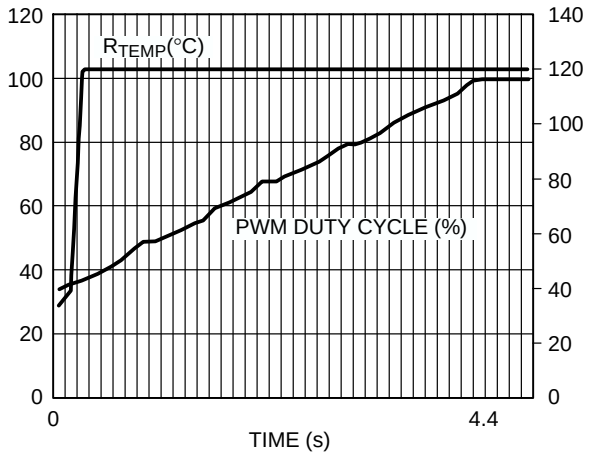


**Figure 78. Enhanced Acoustics Mode with Ramp Rate = 8**

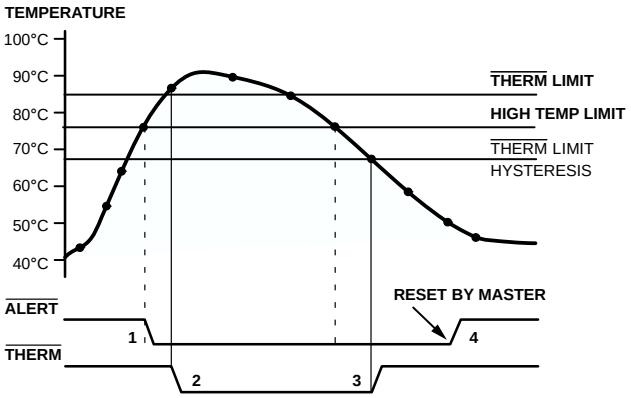


**Figure 83. THERM Behavior**

### THERM Timer

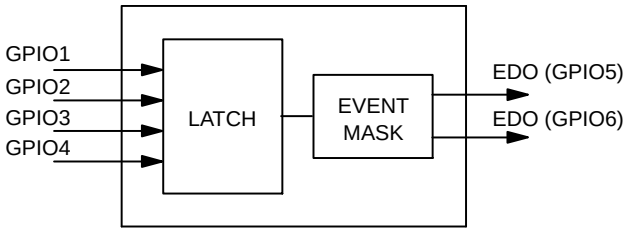


**Figure 84. EDO Circuit**

**EDO Circuitry**

**Table 33. EDO CONTROL (MASK) REGISTER 0X37 AND REGISTER 0X38**

| Bit 7: Overvoltage/ Undervoltage | Bit 6: $\overline{\text{THERM}}$ | Bit 5: Fan Fail | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Behavior: What Drives and Latches Output X (G = GPIO) |
|---|---|---|---|---|---|---|---|
| 0 = Drive Output X | 0 = Drive Output X | 0 = Drive Output X | 0 | 0 | 0 | 0 | G4 or G3 or G2 or G1 |
| 1 = Ignore Event | 1 = Ignore Event | 1 = Ignore Event | 0 | 0 | 0 | 1 | G4 or G3 or G2 |
| | | | 0 | 0 | 1 | 0 | G4 or G3 or G1 |
| | | | 0 | 0 | 1 | 1 | G4 or G3 |
| | | | 0 | 1 | | | |

**VR_HOT Inputs**

**SCSI_TERM Inputs**

**Reset I/O**

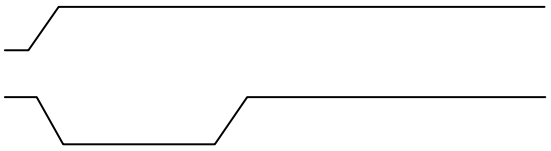

**Figure 85. Operation of $\overline{\text{RESET}}$ Output on Powerup**

**XOR Tree Test**

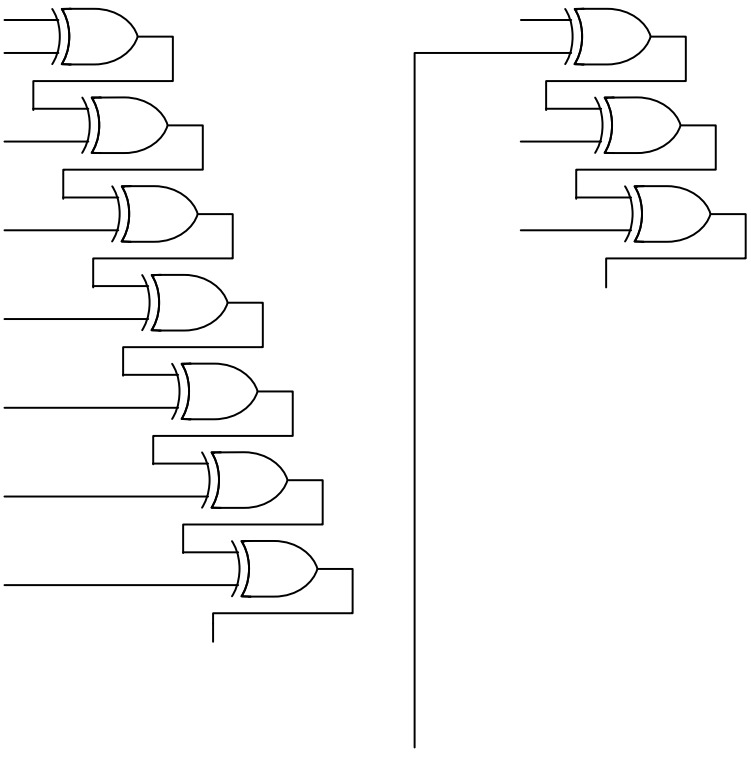

**Figure 86. XOR Tree Test**

## Register Tables

**Table 34. REGISTER MAP**

| Addr | Description | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | De-fault | SW Reset | Lock able |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | Config 0 | R/W | SW Reset | R/W | R/W | | | | | | | | |

| Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | De-fault | SW Reset | Lock able |
|---|---|---|---|---|---|---|---|---|
| 5 | 4 | 3 | 2 | 1 | 0 | 0x80 | Yes | Yes |
| 5 | 4 | 3 | 2 | 1 | 0 | 0x80 | Yes | Yes |
| 5 | 4 | 3 | 2 | 1 | 0 | 0x80 | Yes | Yes |
| 5 | 4 | 3 | 2 | 1 | 0 | 0x80 | Yes | Yes |
| 5 | 4 | 3 | 2 | 1 | 0 | 0xC0 | Yes | Yes |
| R1D | R3 | R2 | R1 | Local0 | | | | |

**Table 34. REGISTER MAP**

| Addr | Description | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | De-fault | SW Reset | Lock able |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x50 | Local $\overline{\text{THERM2}}$/ +1.5V1 (ICH) High | R/W | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0xA4 | No | Yes |
| 0x51 | Remote 1 $\overline{\text{THERM2}}$ Limit | R/W | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0xA4 | No | Yes |
| 0x52 | Remote 2 $\overline{\text{THERM2}}$ Limit | R/W | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0xA4 | No | Yes |
| 0x53 | Remote 3 $\overline{\text{THERM2}}$ Limit | R/W | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0xA4 | No | Yes |
| 0x54 | Local/Re-mote1 Temp Hyst | R/W | LH | LH | LH | LH | R1H | R1H | R1H | R1H | 0x44 | No | Yes |
| 0x55 | Remote 2/ Remote 3 Temp Hyst | R/W | R2H | R2H | R2H | R2H | R3H | R3H | R3H | R3H | 0x44 | No | Yes |
| 0x56 | Local Offset | R/W | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x00 | No | Yes |
| 0x57 | Remote 1 Offset | R/W | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x00 | No | Yes |
| 0x58 | Remote 2 Offset | R/W | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x00 | No | Yes |
| 0x59 | Remote 3 Offset | R/W | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x00 | No | Yes |
| 0x5A | Remote 1 Operating Point | R/W | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0xA4 | Yes | Yes |
| 0x5B | Remote 2 Operating Point | R/W | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0xA4 | Yes | Yes |
| 0x5C | Local Temp $T_{MIN}$ | R/W | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x9A | Yes | Yes |
| 0x5D | Remote 1 Temp $T_{MIN}$ | R/W | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x9A | Yes | Yes |
| 0x5E | Remote 2 Temp $T_{MIN}$ | R/W | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x9A | Yes | Yes |
| 0x5F | Remote 3 Temp $T_{MIN}$ | R/W | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x9A | Yes | Yes |
| 0x60 | Local $T_{RANGE}$/ Hyst | R/W | Range | Range | Range | Range | Hys | Hys | Hys | Hys | 0xC4 | Yes | Yes |
| 0x61 | Remote 1 $T_{RANGE}$/ Hyst | R/W | Range | Range | Range | Range | Hys | Hys | Hys | Hys | 0xC4 | Yes | Yes |
| 0x62 | Remote 2 $T_{RANGE}$/ Hyst | R/W | Range | Range | Range | Range | Hys | Hys | Hys | Hys | 0xC4 | Yes | Yes |
| 0x63 | Remote 3 $T_{RANGE}$/ Hyst | R/W | Range | Range | Range | Range | Hys | Hys | Hys | Hys | 0xC4 | Yes | Yes |
| 0x64 | Operating Point Hyst | R/W | Hys | Hys | Hys | Hys | Res | | | | | | |

# ADT7462

**Table 34. REGISTER MAP**

| Addr | Description | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | De-fault | SW Reset | Lock able |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0xA4 | TACH6 Value, LSB | R | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0xFF | No | No |
| 0xA5 | TACH6 MSB/+12V 2 Voltage | R | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0xFF | No | No |
| 0xA6 | TACH7 Value, LSB | R | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0xFF | No | No |
| 0xA7 | TACH7 MSB/+5V Voltage | R | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0xFF | No | No |
| 0xA8 | TACH8 Value, LSB | R | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0xFF | No | No |
| 0xA9 | TACH8 MSB/+12V 3 Voltage | R | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0xFF | No | No |
| 0xAA | PWM1 Duty Cycle | R/W | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x00 | No | No |
| 0xAB | PWM2 Duty Cycle | R/W | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x00 | No | No |
| 0xAC | PWM3 Duty Cycle | R/W | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0xC0 | No | No |
| 0xAD | PWM4 Duty Cycle | R/W | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x00 | No | No |
| 0xAE | $\overline{\text{THERM1}}$ %On−Time | R | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x00 | No | No |
| 0xAF | $\overline{\text{THERM2}}$ %On−Time | R | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0x00 | No | No |
| 0xB8 | Thermal Status 1, Host | R | R3D | R2D | R1D | R3 | R2 | R1 | Local | Res | 0x00 | Yes | No |
| 0xB9 | Thermal Status 2, Host | R | VR2 | VR1 | T2S | T2A | T2% | T1S | T1A | T1% | 0x00 | Yes | No |
| 0xBA | Thermal Status 3, Host | R | R3T2 | R2T2 | R1T2 | LT2 | R3T1 | R2T1 | R1T1 | LT1 | 0x00 | Yes | No |
| 0xBB | Voltage Status 1, Host | R | Pin 23 | +5V | Pin 19 | Pin 15 | +3.3V | +12V3 | +12V2 | +12V1 | 0x00 | Yes | No |
| 0xBC | Voltage Status 2, Host | R | +1.5V1 (ICH) | +1.5V2 (3GIO) | Pin 26 | Pin 25 | Pin 24 | Res | Res | Res | 0x00 | Yes | No |
| 0xBD | Fan Status, Host | R | Fan 8 | Fan 7 | Fan 6 | Fan 5 | Fan 4 | Fan 3 | Fan 2 | Fan 1 | 0x00 | Yes | No |
| 0xBE | Digital Status, Host | R | CI | VID | SCSI2 | SCSI1 | $\overline{\text{FAN2MAX}}$ | Res | Res | Res | 0x00 | Yes | No |
| 0xBF | GPIO Status, Host | R/W | GPIO8 | GPIO7 | GPIO6 | GPIO5 | GPIO4 | GPIO3 | GPIO2 | GPIO1 | 0x00 | Yes | No |
| 0xC0 | Thermal Status 1, BMC | R | R3D | R2D | R1D | R3 | R2 | R1 | Local | Res | 0x00 | Yes | No |
| 0xC1 | Thermal Status 2, BMC | R | VR2 | VR1 | T2S | T2A | T2% | T1S | T1A | T1% | 0x00 | Yes | No |
| 0xC3 | Voltage Status 1, BMC | R | Pin 23 | +5V | Pin 19 | Pin 15 | +3.3V | | | | | | |

**Table 34. REGISTER MAP**

| Addr | | | | | | | | | Default | SW Reset | Lockable |
|---|---|---|---|---|---|---|---|---|---|---|---|

**Table 41. REGISTER 0X09 − GPIO CONFIGURATION REGISTER 1** (Note 1)

| Bit | Name | R/W | Description |
|---|---|---|---|
| 0 | GPIO1_P | R/W | This bit sets the polarity of GPIO1. 0 = Default = Active Low. 1= Active High. |
| 1 | GPIO1_D | R/W | This bit sets the direction of GPIO1. 0 = Default = Input. 1= Output. |
| 2 | GPIO2_P | R/W | This bit sets the polarity of GPIO2. 0 = Default = Active low. 1= Active High. |
| 3 | GPIO2_D | R/W | This bit sets the direction of GPIO2. 0 = Default = Input. 1= Output. |
| 4 | GPIO3_P | R/W | This bit sets the polarity of GPIO3. 0 = Default = Active Low. 1= Active High. |
| 5 | GPIO3_D | R/W | This bit sets the direction of GPIO3. 0 = Default = Input. 1= Output. |
| 6 | GPIO4_P | R/W | This bit sets the polarity of GPIO4. 0 = Default = Active Low. 1= Active High. |
| 7 | GPIO4_D | R/W | This bit sets the direction of GPIO4. 0 = Default = Input. 1= Output. |

1. POR = 0x00, Lock = Y, SW Reset = Y.

**Table 42. REGISTER 0X0A − GPIO CONFIGURATION REGISTER 2** (Note 1)

| Bit | Name | R/W | Description |
|---|---|---|---|
| 0 | GPIO5_P | R/W | This bit sets the polarity of GPIO5. 0 = Default = Active Low. 1= Active High. |
| 1 | GPIO5_D | R/W | This bit sets the direction of GPIO5. 0 = Default = Input. 1= Output. |
| 2 | GPIO6_P | R/W | This bit sets the polarity of GPIO6. 0 = Default = Active Low. 1= Active High. |
| 3 | GPIO6_D | R/W | This bit sets the direction of GPIO6. 0 = Default = Input. 1= Output. |
| 4 | GPIO7_P | R/W | This bit sets the polarity of GPIO7. 0 = Default = Active Low. 1= Active High. |
| 5 | GPIO7_D | R/W | This bit sets the direction of GPIO7. 0 = Default = Input. 1= Output. |
| 6 | GPIO8_P | R/W | This bit sets the polarity of GPIO8. 0 = Default = Active Low. 1= Active High. |
| 7 | GPIO8_D | R/W | This bit sets the direction of GPIO8. 0 = Default = Input. 1= Output. |

1. POR = 0x00, Lock = Y, SW Reset = Y.

**Table 43. REGISTER 0X0B − DYNAMIC $T_{MIN}$ CONTROL REGISTER 1** (Note 1)

| Bit | Name | R/W | Description |
|---|---|---|---|
| 0 | Remote 1 En | R/W | Setting this bit to 1 enables dynamic $T_{MIN}$ control for the Remote 1 channel. Default = 0. |
| 1 | Remote 2 En | R/W | Setting this bit to 1 enables dynamic $T_{MIN}$ control for the Remote 2 channel. Default = 0. |
| 2 | P1R1 | R/W | P1R1 = 1 copies the Remote 1 current temperature to the Remote 1 operating point register if $\overline{\text{THERM1}}$ is asserted externally. This happens only if the current temperature is less than the value in the operating point register. The operating point contains the temperature at which $\overline{\text{THERM1}}$ is asserted. P1R1 = 0 (Default) ignores any $\overline{\text{THERM1}}$ assertions on the $\overline{\text{THERM1}}$ pin. The Remote 1 operating point register reflects its programmed value. |
| 3 | P1R2 | R/W | P1R2 = 1 copies the Remote 2 current temperature to the Remote 2 operating point register if $\overline{\text{THERM1}}$ is asserted externally. This happens only if the current temperature is less than the value in the operating point register. The operating point contains the temperature at which $\overline{\text{THERM1}}$ is asserted. P1R2 = 0 (Default) ignores any $\overline{\text{THERM1}}$ assertions on the $\overline{\text{THERM1}}$ pin. The Remote 2 operating point register reflects its programmed value. |

**Table 46. REGISTER 0X0E − $\overline{\text{THERM1}}$ CONFIGURATION REGISTER** (Note 1)

| Bit | Name | R/W | Description |
|---|---|---|---|
| 0 | $\overline{\text{THERM1}}$ Timer Enable | R/W | Enables the $\overline{\text{THERM1}}$ timer circuit. Default = 0. |
| 1 | $\overline{\text{THERM1}}$_Local | R/W | Setting the bit to 1 means that the $\overline{\text{THERM1}}$ pin is asserted low as an output whenever the local temperature exceeds the local $\overline{\text{THERM1}}$ temperature limit. Default = 0. |
| 2 | $\overline{\text{THERM1}}$_ Remote 1 | R/W | Setting the bit to 1 means that the $\overline{\text{THERM1}}$ pin is asserted low as an output whenever the Remote 1 temperature exceeds the Remote 1 $\overline{\text{THERM1}}$ temperature limit. Default = 0. |
| 3 | $\overline{\text{THERM1}}$_ Remote 2 | R/W | Setting the bit to 1 means that the $\overline{\text{THERM1}}$ pin is asserted low as an output whenever the Remote 2 temperature exceeds the Remote 2 $\overline{\text{THERM1}}$ temperature limit. Default = 0. |
| 4 | $\overline{\text{THERM1}}$_ Remote 3 | R/W | Setting the bit to 1 means that the $\overline{\text{THERM1}}$ pin is asserted low as an output whenever the Remote 3 temperature exceeds the Remote 3 $\overline{\text{THERM1}}$ temperature limit. Default = 0. |
| [7:5] | Reserved | R | Reserved for future use. |

1. POR = 0x00, Lock = Y, SW Reset = Y.

**Table 47. REGISTER 0X0F − $\overline{\text{THERM2}}$ CONFIGURATION REGISTER** (Note 1)

| Bit | Name | R/W | Description |
|---|---|---|---|
| 0 | $\overline{\text{THERM2}}$ Timer Enable | R/W | Enables the $\overline{\text{THERM2}}$ timer circuit. Default = 0. |
| 1 | $\overline{\text{THERM2}}$_Local | R/W | Setting the bit to 1 means that the $\overline{\text{THERM2}}$ pin is asserted low as an output whenever the local temperature exceeds the local $\overline{\text{THERM2}}$ temperature limit. Default = 0. |
| 2 | $\overline{\text{THERM2}}$_ Remote 1 | R/W | Setting the bit to 1 means that the $\overline{\text{THERM2}}$ pin is asserted low as an output whenever the Remote 1 temperature exceeds the Remote 1 $\overline{\text{THERM2}}$ temperature limit. Default = 0. |
| 3 | $\overline{\text{THERM2}}$_ Remote 2 | R/W | Setting the bit to 1 means that the $\overline{\text{THERM2}}$ pin is asserted low as an output whenever the Remote 2 temperature exceeds the Remote 2 $\overline{\text{THERM2}}$ temperature limit. Default = 0. |
| 4 | $\overline{\text{THERM2}}$_ Remote 3 | R/W | Setting the bit to 1 means that the $\overline{\text{THERM2}}$ pin is asserted low as an output whenever the Remote 3 temperature exceeds the Remote 3 $\overline{\text{THERM2}}$ temperature limit. Default = 0. |
| [7:5] | Reserved | R | Reserved for future use. |

1. POR = 0x00, Lock = Y, SW Reset = Y.

**Table 48. REGISTER 0X10 − PIN CONFIGURATION REGISTER 1** (Note 1)

| Bit | Name | R/W | Description |
|---|---|---|---|
| 0 | Pin 7 | R/W | 0 = +12V1; 1 = TACH5 Input. Default = 1. |
| 1 | Pin 4 | R/W | 0 = GPIO4; 1= TACH4 Input (that is, if the VIDs are not selected). Default = 1. |
| 2 | Pin 3 | R/W | 0 = GPIO3; 1= TACH3 Input (that is, if the VIDs are not selected). Default = 1. |
| 3 | Pin 2 | R/W | 0 = GPIO2; 1= TACH2 Input (that is, if the VIDs are not selected). Default = 1. |
| 4 | Pin 1 | R/W | 0 = GPIO1; 1= TACH1 Input (that is, if the VIDs are not selected). Default = 1. |
| 5 | Diode 3 | R/W | 1 enables the D3+ and D3− inputs on Pin 19 and Pin 20. 0 enables the voltage measurement input and SCSI_TERM2 input. Default = 1. |
| 6 | Diode 1 | R/W | 1 enables the D1+ and D1− inputs on Pin 15 and Pin 16. 0 enables the voltage measurement input and SCSI_TERM1 input. Default = 1. |
| 7 | VIDs | R/W | Setting this bit to 1 enables the VIDs on Pin 1 to Pin 4, Pin 28, Pin 31, and Pin 32. Default = 0. |

1. POR = 0x7F, Lock = Y, SW Reset = Y.

**Table 52. REGISTER 0X14 − EASY CONFIGURATION OPTIONS** (Note 1)

| Bit | Name | R/W | Description |
|---|---|---|---|
| 0 | Easy Option 1 Select | R/W | Setting this bit to 1 enables Easy Option 1. |
| 1 | Easy Option 2 Select | R/W | Setting this bit to 1 enables Easy Option 2. |
| 2 | Easy Option 3 Select | R/W | Setting this bit to 1 enables Easy Option 3. |
| 3 | Easy Option 4 Select | R/W | Setting this bit to 1 enables Easy Option 4. |
| 4 | Easy Option 5 Select | R/W | Setting this bit to 1 enables Easy Option 5. |
| [7:5] | Reserved | R | Reserved for future use. |

1. POR = 0x01, Lock = Y, SW Reset = Y.

**Table 53. REGISTER 0X16 − EDO/SINGLE CHANNEL ENABLE** (Note 1)

| Bit | Name | R/W | Description |
|---|---|---|---|
| 0 | EDO_En1 | R/W | Enable EDO on GPIO5. Default = 0. |
| 1 | EDO_En2 | R/W | Enable EDO on GPIO6. Default = 0. |
| 2 | Single−Channel Mode Select | R/W | Setting this bit to 1 places the ADT7462 in single-channel mode. This means that it converts on one channel only. The channel it converts on is set using the channel select bits in this register. Default = 0. |
| [7:3] | Channel Select | R/W | |

**Table 56. REGISTER 0X1A −**

**Table 59. REGISTER 0X1D −**

**Table 62. REGISTER 0X21, REGISTER 0X22, REGISTER 0X23, REGISTER 0X24 − PWM1, PWM2, PWM3 AND PWM4 CONFIGURATION REGISTERS**

| Bit | Name | R/W | Description |
|---|---|---|---|
| [2:0] | Spin-Up Timeout | R/W | These bits set the duration of the fan startup timeout and the timeout for the fan freewheeling test.<br>000 = No Startup Timeout<br>001 = 100 ms<br>010 = 250 ms<br>011 = 400 ms<br>100 = 667 ms<br>101 = 1 sec<br>110 = 2 sec<br>111 = 32 sec |
| 3 | SLOW | R/W | Setting this bit to 1 makes the ramp rate of the enhance acoustics mode four times longer. |
| 4 | INV | R/W | Setting this bit to 0, the PWM outputs are active low. Setting this bit to 1, the PWM outputs are active high (Default). |
| [7:5] | BHVR | R/W | These bits determine which temperature channel controls the fans in the automatic fan speed control loop.<br>000 = Local Temperature<br>001 = Remote 1 Temperature<br>010 = Remote 2 Temperature<br>011 = Remote 3 Temperature<br>100 = Off<br>101 = Maximum Fan Speed Calculated by the Local and Remote 3 TC3 Maxip |

**Table 64. REGISTER 0X26**

**Table 72. REGISTER 0X35 − DIGITAL MASK REGISTER** (Note 1)

| Bit | Name | R/W | Description |
|---|---|---|---|
| [2:0] | Reserved | R | Reserved for future use. |
| 3 | $\overline{\text{FAN2MAX}}$ | R/W | 1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit. Default = 1. |
| 4 | SCSI1 | R/W | 1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit. Default = 1. |
| 5 | SCSI2 | R/W | 1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit. Default = 1. |
| 6 | VID Comparison | R/W | 1 masks $\overline{\text{ALERT}}$ |

**Table 76. REGISTER 0X3D − DEVICE ID REGISTER** (Note 1)

| Bit | Name | R/W | Description |
|---|---|---|---|
| [7:0] | Device ID | R | This register contains the device ID (0x62) for the ADT7462. |

1. POR = 0x62, SW Reset = N.

**Table 77. REGISTER 0X3E − COMPANY ID REGISTER** (Note 1)

| Bit | Name | R/W | Description |
|---|---|---|---|
| [7:0] | Company ID | R | This register contains the company ID (0x41) for the ADT7462. |

1. POR = 0x41, SW Reset = N.

**Table 78. REGISTER 0X3F − REVISION REGISTER** (Note 1)

| Bit | Name | R/W | Description |
|---|---|---|---|
| [7:0] | Revision ID | R | This register contains the revision ID (0x04) for the ADT7462. |

1. POR = 0x04, SW Reset = N.

**Table 79. TEMPERATURE LIMIT REGISTERS** (Note 1)

| Register Address | R/W | Description |
|---|---|---|

**Table 81. REGISTER 0X55 − REMOTE 2/REMOTE 3 TEMPERATURE HYSTERESIS** (Note 1)

| Bit | Name | R/W | Description |
|---|---|---|---|
| [3:0] | Remote 3 Hysteresis | R/W | These four bits set the Remote 3 $\overline{\text{THERM}}$ hysteresis value, 1 LSB = 1°C. |
| [7:4] | Remote 2 Hysteresis | R/W | These four bits set the Remote 2 $\overline{\text{THERM}}$ hysteresis value, 1 LSB = 1°C.<br>0000 = 0°C 0001 = 1°C<br>0010 = 2°C 0011 = 3°C<br>0100 = 4°C (Default) 0101 = 5°C<br>0110 = 6°C 0111 = 7°C<br>1000 = 8°C 1001 = 9°C<br>1010 = 10°C 1011 = 11°C<br>1100 = 12°C 1101 = 13°C<br>1110 = 14°C 1111 = 15°C |

1. POR = 0x44, Lock = Y, SW Reset = N.

**Table 82. OFFSET REGISTERS** (Note 1)

| Register Address | R/W | Description | POR Default |
|---|---|---|---|
| 0x56 | R/W | Local offset, resolution = 0.5°C. | 0x00 |
| 0x57 | R/W | Remote 1 offset, resolution = 0.5°C. | 0x00 |
| 0x58 | R/W | Remote 2 offset, resolution = 0.5°C. | 0x00 |
| 0x59 | R/W | Remote 3 offset, resolution = 0.5°C. | 0x00 |

1. Lock = Y, SW Reset = N.

**Table 83. OPERATING POINT REGISTERS** (Note 1)

| Register Address | R/W | Description | POR Default |
|---|---|---|---|
| 0x5A | R/W | Remote 1 operating point. | 0xA4 |
| 0x5B | R/W | Remote 2 operating point. | 0xA4 |

1. Lock = Y, SW Reset = Y.

**Table 84. TIMING REGISTERS** (Note 1)

| Register Address | R/W | Description | POR Default |
|---|---|---|---|
| 0x5C | R/W | Local temperature $T_{MIN}$. | 0x9A |
| 0x5D | R/W | Remote 1 temperature $T_{MIN}$. | 0x9A |
| 0x5E | R/W | Remote 2 temperature $T_{MIN}$. | 0x9A |
| 0x5F | R/W | Remote 3 temperature $T_{MIN}$. | 0x9A |

1. Lock = Y, SW Reset = Y.

**Table 85. $T_{RANGE}$/HYSTERESIS REGISTERS** (Note 1)

| Register Address | R/W | Description | POR Default |
|---|---|---|---|
| 0x60 | R/W | Local $T_{RANGE}$/Hysteresis | 0xC4 |
| 0x61 | R/W | Remote 1 $T_{RANGE}$/Hysteresis | 0xC4 |
| 0x62 | R/W | Remote 2 $T_{RANGE}$/Hysteresis | 0xC4 |
| 0x63 | R/W | Remote 3 $T_{RANGE}$/Hysteresis | 0xC4 |

1. Lock = Y, SW Reset = Y.

**Table 89. TACH LIMIT REGISTERS** (Note 1)

| Register Address | R/W | Description | POR Default |
|---|---|---|---|
| 0x78 | R/W | TACH1 limit/VID limit. | 0xFF |
| 0x79 | R/W | TACH2 limit. | 0xFF |
| 0x7A | R/W | TACH3 limit. | 0xFF |
| 0x7B | R/W | TACH4 limit. | 0xFF |
| 0x7C | R/W | TACH5 limit/+12V1 voltage high limit. | 0xFF |
| 0x7D | R/W | TACH6 limit/+12V2 voltage high limit. | 0xFF |
| 0x7E | R/W | TACH7 limit/+5V voltage high limit. | 0xFF |
| 0x7F | R/W | TACH8 limit/+12V3 voltage high limit. | 0xFF |

1. Lock = Y, SW Reset = N.

**Table 90. $\overline{\text{THERM}}$ TIMER LIMIT REGISTERS** (Note 1)

| Register Address | R/W | Description | POR Default |
|---|---|---|---|
| 0x80 | R/W | $\overline{\text{THERM1}}$ Timer Limit. | 0xFF |
| 0x81 | R/W | $\overline{\text{THERM2}}$ Timer Limit. | 0xFF |

1. Lock = Y, SW Reset = N.

**Table 91. TEMPERATURE VALUE REGISTERS** (Note 1)

| Register Address | R/W | Description | POR Default |
|---|---|---|---|

0x8Tm(R/W)TjET1.272 527.187 23Res9688 0 8 192.8126 654.7.403 461.v13 538.129 32.8215ult

**Table 94. TACH VALUE REGISTERS** (Note 1)

| Register Address | R/W | Description | POR Default |
|---|---|---|---|
| 0x98 | R | TACH1, LSB. | 0xFF |
| 0x99 | R | TACH1, MSB. | 0xFF |
| 0x9A | R | TACH2, LSB. | 0xFF |
| 0x9B | R | TACH2, MSB. | 0xFF |
| 0x9C | R | TACH3, LSB. | 0xFF |
| 0x9D | R | TACH3, MSB. | 0xFF |
| 0x9E | R | TACH4, LSB. | 0xFF |
| 0x9F | R | TACH4, MSB. | 0xFF |
| 0xA2 | R | TACH5, LSB. | 0xFF |
| 0xA3 | R | | |

**Table 98. REGISTER 0XB9 − HOST THERMAL STATUS REGISTER 2** (Note 1)**;**
**REGISTER 0XC1 − BMC THERMAL STATUS REGISTER 2** (Note 1)

| Bit | Name | R/W | Description |
|---|---|---|---|
| 0 | $\overline{\text{THERM1}}$ % | R | A 1 indicates that $\overline{\text{THERM1}}$ has been asserted for longer than the programmed $\overline{\text{THERM1}}$ timer limit. |
| 1 | $\overline{\text{THERM1}}$ Assert | R | A 1 indicates that $\overline{\text{THERM1}}$ is asserted. |
| 2 | $\overline{\text{THERM1}}$ State | R | A 1 indicates that a transition from high to low has taken place on the $\overline{\text{THERM1}}$ pin. |
| 3 | $\overline{\text{THERM2}}$ % | R | A 1 indicates that $\overline{\text{THERM2}}$ has been asserted for longer than the programmed $\overline{\text{THERM2}}$ timer limit. |
| 4 | $\overline{\text{THERM2}}$ Assert | R | A 1 indicates that $\overline{\text{THERM2}}$ is asserted. |
| 5 | $\overline{\text{THERM2}}$ State | R | A 1 indicates that a transition from high to low has taken place on the $\overline{\text{THERM2}}$ pin. |
| 6 | VRD1_Assert | R | A 1 indicates that VRD1 is asserted. |
| 7 | VRD2_Assert | R | A 1 indicates that VRD2 is asserted. |

1. POR = 0x00, Lock = N, SW Reset = Y.

**Table 99. REGISTER 0XBA − HOST THERMAL STATUS REGISTER 3** (Note 1)

| Bit | Name | R/W | Description |
|---|---|---|---|
| 0 | Local $\overline{\text{THERM1}}$ | R | A 1 indicates that the local $\overline{\text{THERM1}}$ limit has been exceeded. |
| 1 | Remote 1 $\overline{\text{THERM1}}$ | R | A 1 indicates that the Remote 1 $\overline{\text{THERM1}}$ limit has been exceeded. |
| 2 | Remote 2 $\overline{\text{THERM1}}$ | R | A 1 indicates that the Remote 2 $\overline{\text{THERM1}}$ limit has been exceeded. |
| 3 | Remote 3 $\overline{\text{THERM1}}$ | R | A 1 indicates that the Remote 3 $\overline{\text{THERM1}}$ limit has been exceeded. |
| 4 | Local $\overline{\text{THERM2}}$ | R | A 1 indicates that the Local $\overline{\text{THERM2}}$ limit has been exceeded. |
| 5 | Remote 1 $\overline{\text{THERM2}}$ | R | A 1 indicates that the Remote 1 $\overline{\text{THERM2}}$ limit has been exceeded. |
| 6 | Remote 2 $\overline{\text{THERM2}}$ | R | A 1 indicates that the Remote 2 $\overline{\text{THERM2}}$ limit has been exceeded. |
| 7 | Remote 3 $\overline{\text{THERM2}}$ | R | A 1 indicates that the Remote 3 $\overline{\text{THERM2}}$ limit has been exceeded. |

1. POR = 0x00, Lock = N, SW Reset = Y.

**Table 100. REGISTER 0XBB − HOST VOLTAGE STATUS REGISTER 1** (Note 1)**;**
**REGISTER 0XC3 − BMC VOLTAGE REGISTER 1** (Note 1)

| Bit | Name | R/W | Description |
|---|---|---|---|
| 0 | +12V1 | R | A 1 indicates that a +12V1 voltage limit has been tripped. |
| 1 | +12V2 | R | A 1 indicates that a +12V2 voltage limit has been tripped. |
| 2 | +12V3 | R | A 1 indicates that a +12V3 voltage limit has been tripped. |
| 3 | +3.3V | R | A 1 indicates that a +3.3V voltage limit has been tripped. |
| 4 | Pin 15 Voltage | R | A 1 indicates that a Pin 15 voltage limit has been tripped. |
| 5 | Pin 19 Voltage | R | A 1 indicates that a Pin 19 voltage limit has been tripped. |
| 6 | +5V | R | A 1 indicates that a +5V voltage limit has been tripped. |
| 7 | Pin 23 Voltage | R | A 1 indicates that a Pin 23 voltage limit has been tripped. |

1. POR = 0x00, Lock = N, SW Reset = Y.

**Table 101. REGISTER 0XBC − HOST VOLTAGE STATUS REGISTER 2** (Note 1)**;**
**REGISTER 0XC4 − BMC VOLTAGE STATUS REGISTER 2** (Note 1)

| Bit | Name | R/W | Description |
|---|---|---|---|
| [2:0] | Reserved | R | Reserved for future use. |
| 3 | Pin 24 Voltage | R | A 1 indicates that a Pin 24 voltage limit has been tripped. |
| 4 | Pin 25 Voltage | R | A 1 indicates that a Pin 25 voltage limit has been tripped. |
| 5 | Pin 26 Voltage | R | A 1 indicates that a Pin 26 voltage limit has been tripped. |
| 6 | +1.5V2 (3GIO) | R | A 1 indicates that a +1.5V2 (3GIO) voltage limit has been tripped. |
| 7 | +1.5V1 (ICH) | R | A 1 indicates that a +1.5V1 (ICH) voltage limit has been tripped. |

1. POR = 0x00, Lock = N, SW Reset = Y.

**Table 102. REGISTER 0XBD − HOST FAN STATUS REGISTER** (Note 1)**;**
**REGISTER 0XC5 − BMC FAN STATUS REGISTER** (Note 1)

| Bit | Name | R/W | Description |
|---|---|---|---|
| 0 | Fan 1 Fault | R | A 1 indicates a Fan 1 fault. |
| 1 | Fan 2 Fault | R | A 1 indicates a Fan 2 fault. |
| 2 | Fan 3 Fault | R | A 1 indicates a Fan 3 fault. |
| 3 | Fan 4 Fault | R | A 1 indicates a Fan 4 fault. |
| 4 | | | |

**Table 105. ORDERING INFORMATION**

| Device Number* | Temperature Range | Package Type | Package Option | Shipping† |
|---|---|---|---|---|
| ADT7462ACPZ−REEL | −40°C to +125°C | 32-lead LFCSP_VQ | CP−32−2 | 5,000 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*The “Z” suffix indicates Pb−Free part.