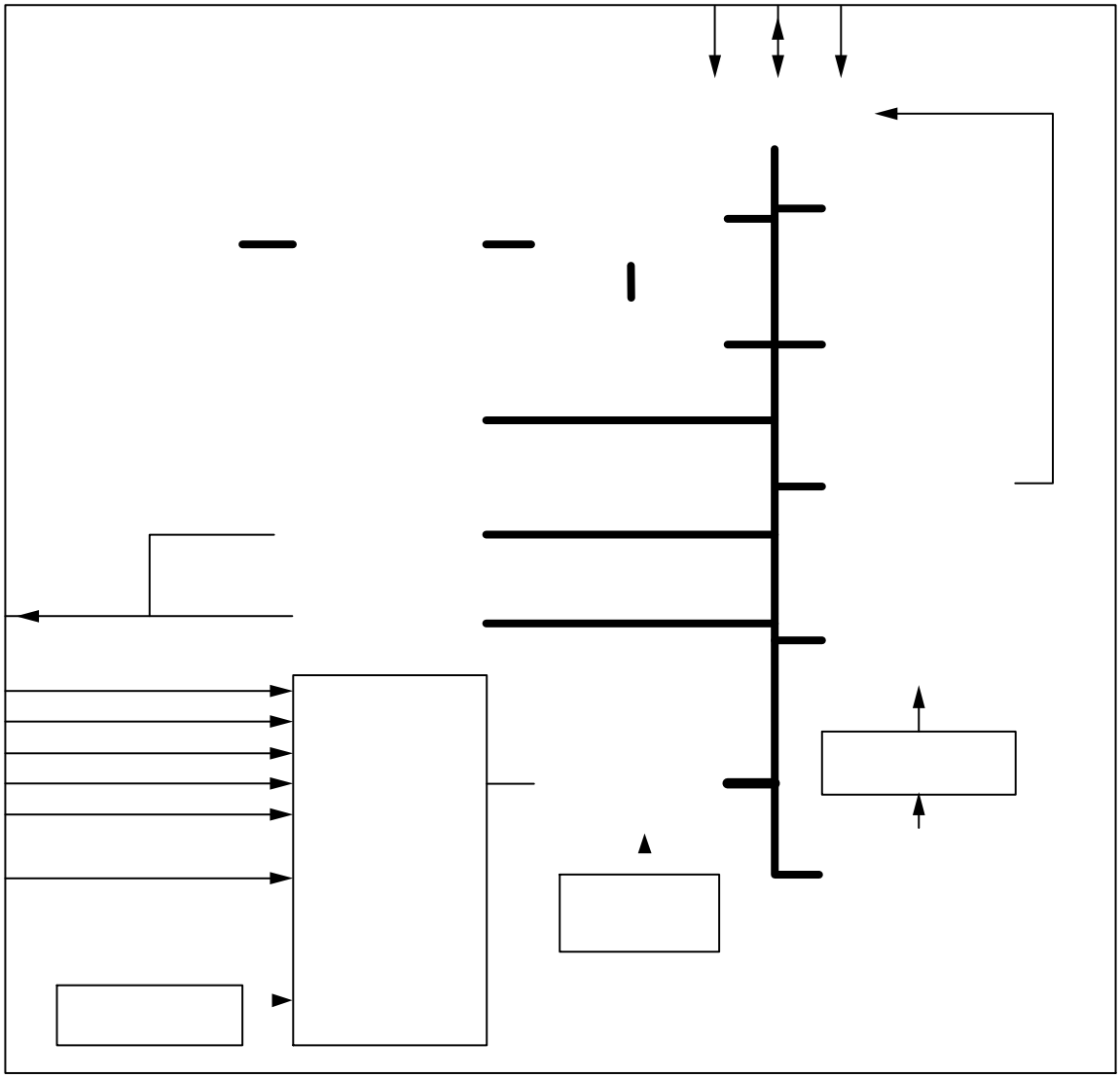


Figure 1. Functional Block Diagram

Table 4. ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted.) (Notes 1, 2, 3, 4)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG−TO−DIGITAL CONVERTER (INCLUDING MUX AND ATTENUATORS)					
Conversion Time (Local Temperature)	Averaging Enabled	−	12.09	13.50	ms
Conversion Time (Remote Temperature)	Averaging Enabled	−	25.59	28	

Table 4. ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted.) (Notes 1, 2, 3, 4)

Parameter	Min	Typ	Max	Unit

TYPICAL PERFORMANCE CHARACTERISTICS (CONT'D)

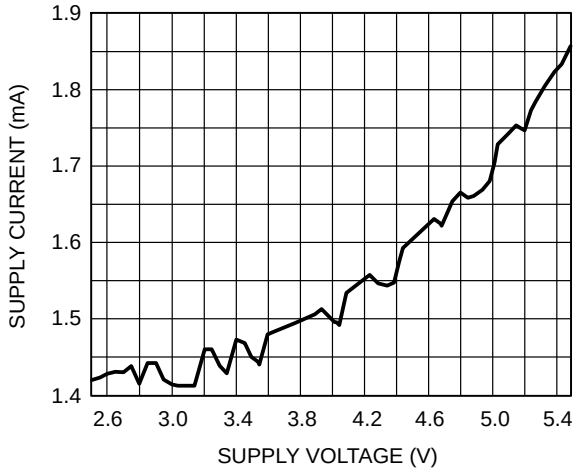


Figure 9. Supply Current vs. Supply Voltage

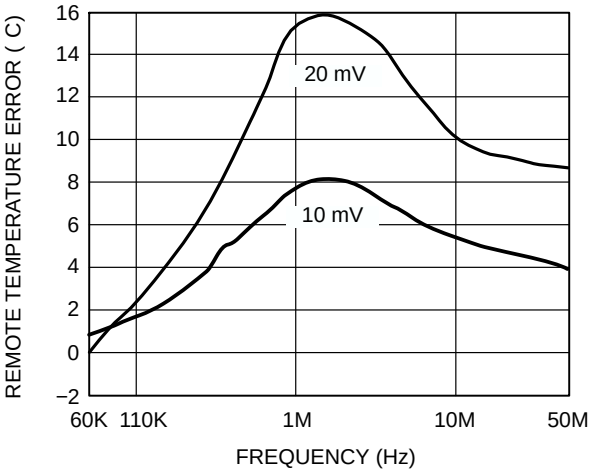


Figure 10. Remote Temperature Error vs. Differential−Mode Noise Frequency

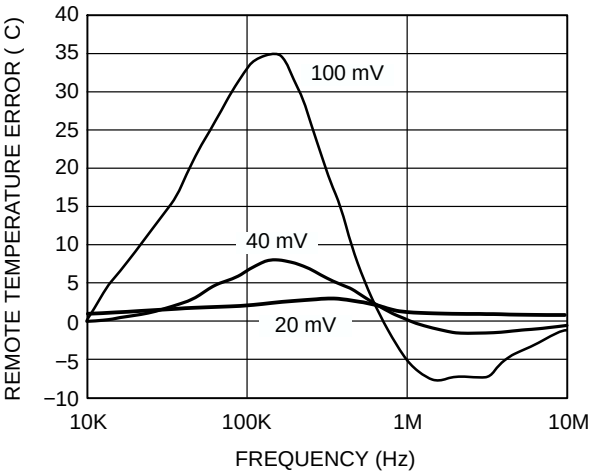


Figure 11. Remote Temperature Error vs. Common−Mode Noise Frequency

FUNCTIONAL DESCRIPTION

General Description

ĭ ĭ

Measurement Inputs

ĭ

ĭ

ĭ

ĭ

T_{RANGE} Registers

ĭ ĭ

Operating Point Registers

Enhance Acoustics Registers

RECOMMENDED IMPLEMENTATION

SERIAL BUS INTERFACE

ĭ

ĭ

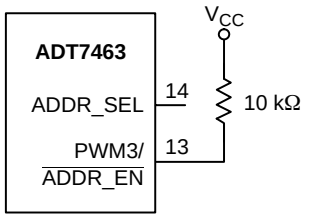
ĭ

ĭ

ĭ ĭ

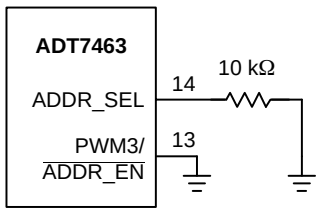
Table 5. ADDRESS SELECT MODE

Pin 13 State	Pin 14 State	Address
0	Low (10 kΩ to GND)	0101100 (0x2C)
0	High (10 kΩ Pull−up)	0101101 (0x2D)
1	Don't Care	0101110 (0x2E) (Default)



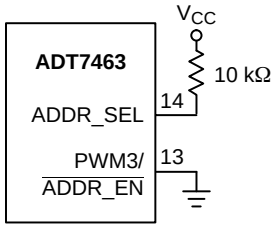
ADDRESS = 0x2E

Figure 13. Default SMBus Address = 0x2E



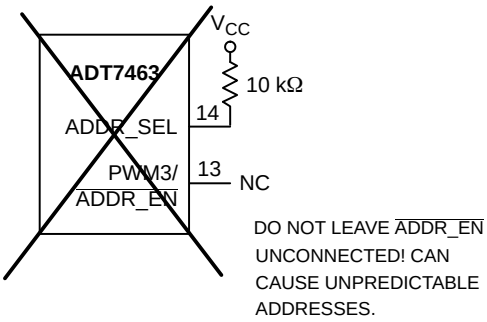
ADDRESS = 0x2C

Figure 14. SMBus Address = 0x2C (Pin 14 = 0)



ADDRESS = 0x2D

Figure 15. SMBus Address = 0x2D (Pin 14 = 1)



CARE SHOULD BE TAKEN TO ENSURE THAT PIN 13 (PWM3/ADDR_EN) IS EITHER TIED HIGH OR LOW. LEAVING PIN 13 FLOATING COULD CAUSE THE ADT7463 TO POWERUP WITH AN UNEXPECTED ADDRESS.

NOTE THAT IF THE ADT7463 IS PLACED INTO ADDRESS SELECT MODE, PINS 13 AND 14 CAN BE USED AS THE ALTERNATE FUNCTIONS (PWM3, TACH4/THERM) ONLY IF THE CORRECT CIRCUIT IS MUXED IN AT THE CORRECT TIME.

Figure 16. Unpredictable SMBus Address if Pin 13 is Unconnected

ĭ ĭ

ĭ

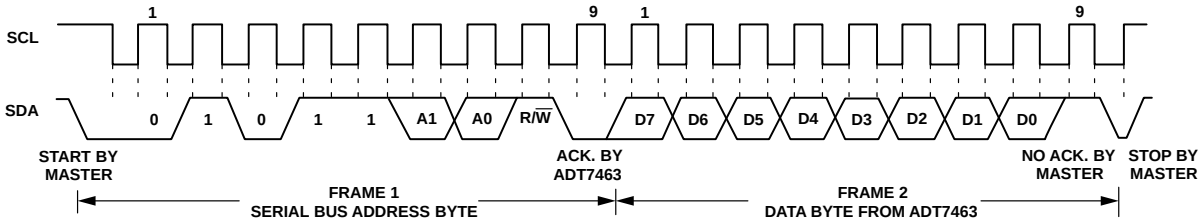


Figure 19. Reading Data from a Previously Selected Register

NOTES:

1. It is possible to *read* a data byte from a data register without first writing to the address pointer register if the address pointer register is already at the correct value. However, it is not possible to *write* data to a register without writing to the address pointer register because the first data byte of a write is always written to the address pointer register.
2. In Figures 17 to 19, the serial bus address is shown as the default value 01011(A1)(A0), where A1 and A0 are set by the address select mode function previously defined.
3. In addition to supporting the Send Byte and Receive Byte protocols, the ADT7463 also supports the Read Byte protocol (see System Management Bus specifications Rev. 2.0 for more information)
4. If it is required to perform se.
   4

ADT7463 READ OPERATIONS

Receive Byte

Table 6. CONFIGURATION REGISTER 1 (REG. 0X40)

Bit	Description

ĭ

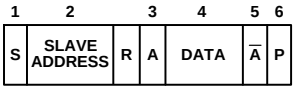


Figure 22. Single Byte Read from a Register

ALERT RESPONSE ADDRESS

SMBUS TIMEOUT

Table 12. 10−BIT A/D OUTPUT CODE VS. V_{IN}

Input Voltage					A/D Output	
+12V_{IN}	**+5V_{IN}**	**V_{CC} (3.3V_{IN})** (Note 6)	**+2.5V_{IN}**	**+V_{CCP}**	**Decimal**	**Binary (10 Bits)**
<0.0156	<0.0065	<0.0042	<0.0032	<0.00293	0	00000000 00
0.0156–0.0312	0.0065–0.0130	0.0042–0.0085	0.0032–0.0065	0.0293–0.0058	1	00000000 01
0.0312–0.0469	0.0130–0.0195	0.0085–0.0128	0.0065–0.0097	0.0058–0.0087	2	00000000 10
0.0469–0.0625	0.0195–0.0260	0.0128–0.0171	0.0097–0.0130	0.0087–0.0117	3	00000000 11
0.0625–0.0781	0.0260–0.0325	0.0171–0.0214	0.0130–0.0162	0.0117–0.0146	4	00000001 00
0.0781–0.0937	0.0325–0.0390	0.0214–0.0257	0.0162–0.0195	0.0146–0.0175	5	00000001 01
0.0937–0.1093	0.0390–0.0455	0.0257–0.0300	0.0195–0.0227	0.0175–0.0205	6	00000001 10
0.1093–0.1250	0.0455–0.0521	0.0300–0.0343	0.0227–0.0260	0.0205–0.0234	7	00000001 11
0.1250–0.14060	0.0521–0.0586	0.0343–0.0386	0.0260–0.0292	0.0234–0.0263	8	00000010 00
4.0000–4.0156	1.6675–1.6740	1.1000–1.1042	0.8325–0.8357	0.7500–0.7529	256 (1/4 Scale)	01000000 00
8.0000–8.0156	3.3300–3.3415	2.2000–2.2042	1.6650–1.6682	1.5000–1.5029	512 (1/2 Scale)	10000000 00
12.0000–12.0156	5.0025–5.0090	3.3000–3.3042	2.4975–2.5007	2.2500–2.2529	768 (3/4 Scale)	11000000 00
15.8281–15.8437	6.5983–6.6048	4.3527–4.3570	3.2942–3.2974	2.9677–2.9707	1013	11111101 01
15.8437–15.8593	6.6048–6.6113	4.3570–4.3613	3.2974–3.3007	2.9707–2.9736	1014	11111101 10
15.8593–15.8750	6.6113–6.6178	4.3613–4.3656	3.3007–3.3039	2.9736–2.9765	1015	11111101 11
15.8750–15.8906	6.6178–6.6244	4.3656–4.3699	3.3039–3.3072	2.9765–2.9794	1016	11111110 00
15.8906–15.9062	6.6244–6.6309	4.3699–4.3742	3.3072–3.3104	2.9794–2.9824	1017	11111110 01
15.9062–15.9218	6.6309–6.6374	4.3742–4.3785	3.3104–3.3137	2.9824–2.9853	1018	11111110 10
15.9218–15.9375	6.6374–6.4390	4.3785–4.3828	3.3137–3.3169	2.9853–2.9882	1019	11111110 11
15.9375–15.9531	6.6439–6.6504	4.3828–4.3871	3.3169–3.3202	2.9882–2.9912	1020	11111111 00
15.9531–15.9687	6.6504–6.6569	4.3871–4.3914	3.3202–3.3234	2.9912–2.9941	1021	11111111 01
15.9687–15.9843	6.6569–6.6634	4.3914–4.3957	3.3234–3.3267	2.9941–2.9970	1022	11111111 10
>15.9843	>6.6634	>4.3957	>3.3267	>2.9970	1023	11111111 11

6. The V_{CC} output codes listed assume that V_{CC} is 3.3 V. If V_{CC} input is reconfigured for 5 V operation (by setting Bit 7 of Configuration Register 1), then the V_{CC} output codes are the same as for the +5V_{IN} column.

VID CODE CHANGE DETECT FUNCTION

μ

Table 13. STATUS REGISTER (REG. 0X42)

Bit	Description
<0> 12V/VC	0: If Pin 21 is configured as VID5, then a Logic 0 denotes no change in VID code within last 11 μs. 1: If Pin 21 is configured as VID5, then a Logic 1 means that a change has occurred on the VID code inputs within the last 11 μs. An $\overline{\text{SMBALERT}}$ generates if this function is enabled.

ADDITIONAL ADC FUNCTIONS FOR VOLTAGE MEASUREMENT

Turn−off Averaging

—

ADDITIONAL ADC FUNCTIONS FOR TEMPERATURE MEASUREMENT

Turn−off Averaging

Single−channel ADC Conversions

ĭ

Table 21. CONFIGURATION REGISTER 2 (REG. 0X73)

Bit	Description
<4>	1: Averaging Off
<6>	1: Single−channel Convert Mode

Table 22. TACH1 MINIMUM HIGH BYTE (REG. 0X55)

Bit	Description	
<7:5>	Selects ADC Channel for Single−channel Convert Mode	
	Value	Channel Selected
	101	Remote 1 Temp
	110	Local Temp
	111	Remote 2 Temp

LIMITS, STATUS REGISTERS, AND INTERRUPTS

Limit Values

ĭ ĭ

ĭ ĭ

8−bit Limits

ĭ

Table 23. VOLTAGE LIMIT REGISTERS

Register	Description	Default
0x44	2.5 V Low Limit	0x00
0x45	2.5 V High Limit	0xFF
0x46	V_{CCP} Low Limit	0x00
0x47	V_{CCP} High Limit	0xFF
0x48	V_{CC} Low Limit	0x00
0x49	V_{CC} High Limit	0xFF
0x4A	5 V Low Limit	0x00
0x4B	5 V High Limit	0xFF
0x4C	12 V Low Limit	0x00
0x4D	12 V High Limit	0xFF

Table 24. TEMPERATURE LIMIT REGISTERS

Register	Description	Default
0x4E	Remote 1 Temperature Low Limit	0x81
0x4F	Remote 1 Temperature High Limit	0x7F
0x6A	Remote 1 $\overline{\text{THERM}}$ Limit	0x64
0x50	Local Temperature Low Limit	0x81
0x51	Local Temperature High Limit	0x7F
0x6B	Local $\overline{\text{THERM}}$ Limit	0x64
0x52	Remote 2 Temperature Low Limit	0x81
0x53	Remote 2 Temperature High Limit	0x7F
0x6C	Remote 2 $\overline{\text{THERM}}$ Limit	0x64

Table 25. $\overline{\text{THERM}}$ LIMIT REGISTERS

Register	Description	Default

ADT7463

Analog Monitoring Cycle Time

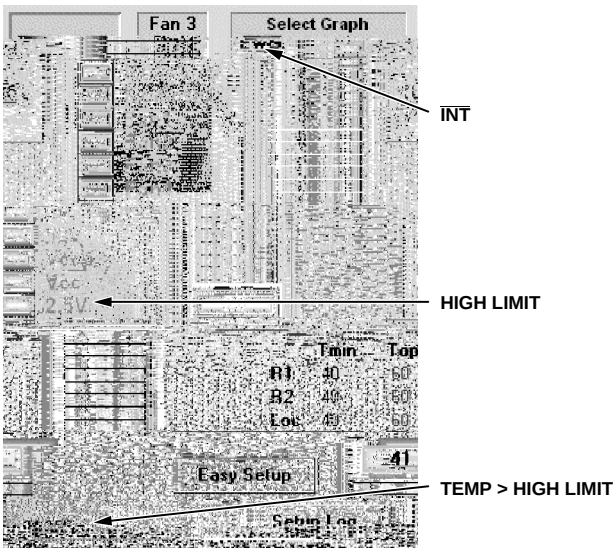


Figure 31. Temperature > High Limit: $\overline{\text{INT}}$ Occurs

$\overline{\text{SMBALERT}}$ Interrupt Behavior

ĭ ĭ

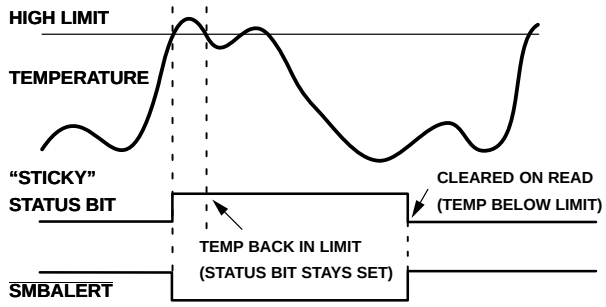


Figure 34. $\overline{\text{SMBALERT}}$ and Status Bit Behavior

ĭ ĭ

ĭ ĭ

Handling $\overline{\text{SMBALERT}}$ Interrupts

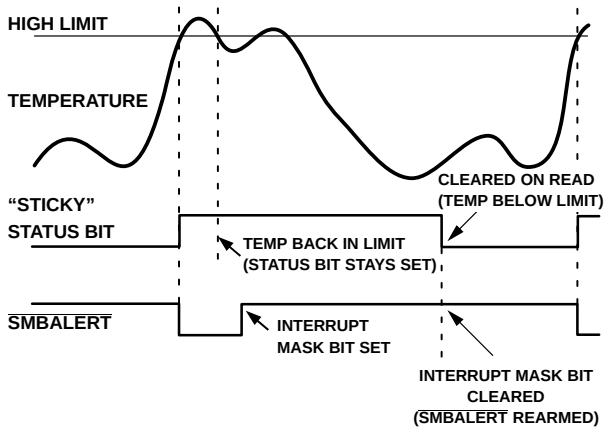


Figure 35. How Masking the Interrupt Source Affects $\overline{\text{SMBALERT}}$ Output

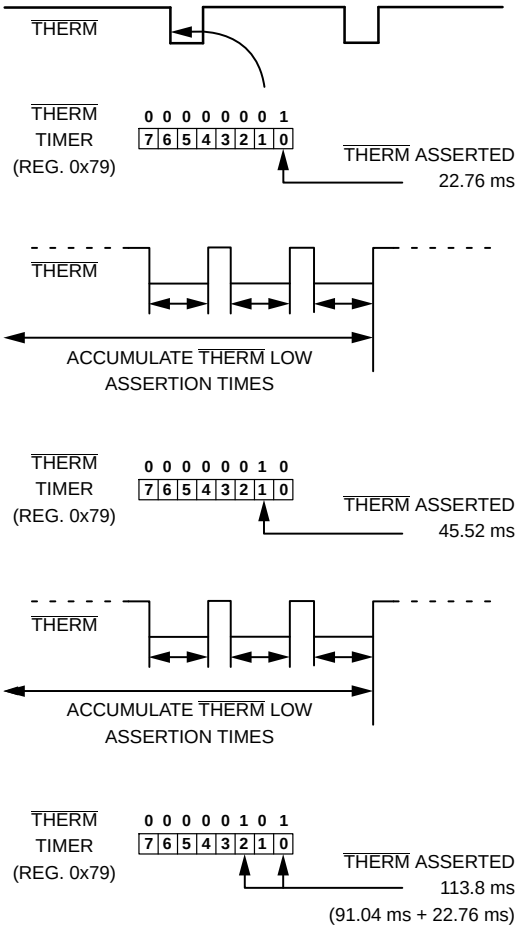


Figure 37. Understanding the THERM Timer

Generating SMBALERT Interrupts from THERM Events

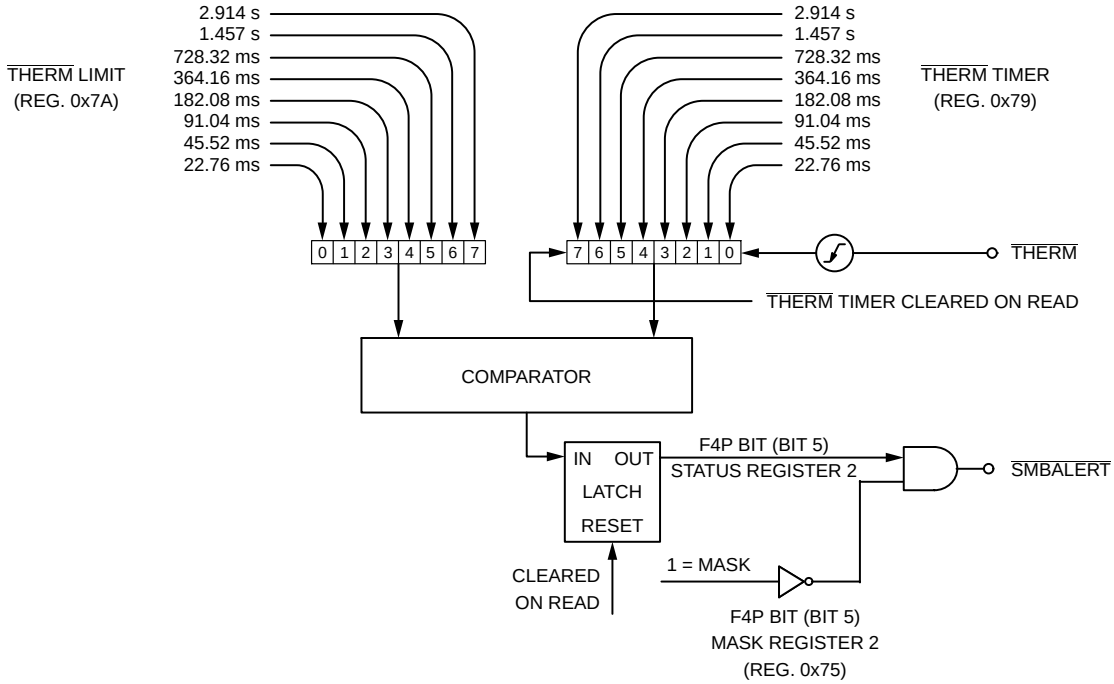


Figure 38. Functional Diagram of the ADT7463 THERM Monitoring Circuitry

Table 33. SYNC: ENHANCE ACOUSTICS REGISTER 1 (REG. 0X62)

Bit	Mnemonic	Description
<4>	SYNC	1 Synchronizes TACH2, TACH3, and TACH4 to PWM2.

Driving 2−wire Fans

ĭ

ĭ

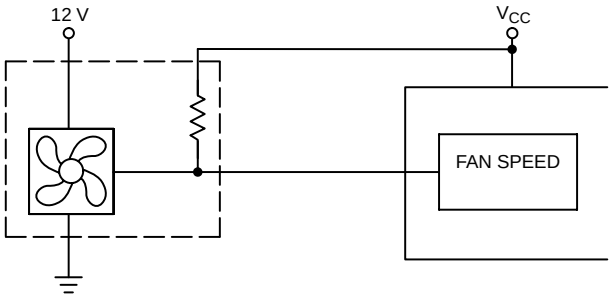


Figure 47. Fan with TACH Pull−up to V_{CC}

ĭ

ĭ

Table 34. FAN SPEED MEASUREMENT REGISTERS

Register	Description	Default
0x28	TACH1 Low Byte	0x00
0x29	TACH1 High Byte	0x00
0x2A	TACH2 Low Byte	0x00
0x2B	TACH2 High Byte	0x00
0x2C	TACH3 Low Byte	0x00
0x2D	TACH3 High Byte	0x00
0x2E	TACH4 Low Byte	0x00
0x2F	TACH4 High Byte	0x00

Reading Fan Speed from the ADT7463

ĭ

Table 36. FAN PULSES PER REVOLUTION REGISTER (REG. 0X7B)

Bit	Mnemonic	Description
<1:0>	FAN1 Default	2 Pulses per Revolution
<3:2>	FAN2 Default	2 Pulses per Revolution
<5:4>	FAN3 Default	2 Pulses per Revolution
<7:6>	FAN4 Default	2 Pulses per Revolution

Table 37. FAN PULSES PER REVOLUTION REGISTER BIT VALUES

Value	Description
00	1 Pulse per Revolution
01	2 Pulses per Revolution
10	3 Pulses per Revolution
11	4 Pulses per Revolution

2–

XOR TREE TEST MODE

ĭ ĭ

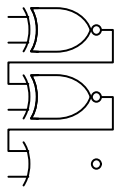


Figure 53. XOR Tree Test

Table 45. ADT7463 REGISTERS

Addr	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Lockable
0x32	R/W	PWM3 Current Duty Cycle	7	6	5	4	3	2	1	0	0xFF	
0x33	R/W	Remote 1 Operating Point	7	6	5	4	3	2	1	0	0x64	YES
0x34	R/W	Local Temp Operating Point	7	6	5	4	3	2	1	0	0x64	YES
0x35	R/W	Remote 2 Operating Point	7	6	5	4	3	2	1	0	0x64	YES
0x36	R/W	Dynamic T_{MIN} Control Reg 1	R2T	LT	R1T	PHTR2	PHTL	PHTR1	V_{CCP}LO	CYR2	0x00	YES
0x37												

Table 45. ADT7463 REGISTERS

Addr	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Lockable
0x59	R/W	TACH3 Minimum High Byte	15	14	13	12	11	10	9	8	0xFF	
0x5A	R/W	TACH4 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	
0x5B	R/W	TACH4 Minimum High Byte	15	14	13	12	11	10				

Table 45. ADT7463 REGISTERS

Addr	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Lockable
0x7A	R/W	$\overline{\text{THERM}}$ Limit Reg.										
0x7B	R/W	Fan Pulses per Revolution	FAN4									

Table 49. CURRENT PWM DUTY CYCLE REGISTERS (POWER−ON DEFAULT = 0XFF) (Note 12)

Register Address	R/W	Description
0x30	R/W	PWM1 Current Duty Cycle (0% to 100% Duty Cycle = 0x00 to 0xFF).
0x31	R/W	PWM2 Current Duty Cycle (0% to 100% Duty Cycle = 0x00 to 0xFF).
0x32	R/W	PWM3 Current Duty Cycle (0% to 100% Duty Cycle = 0x00 to 0xFF).

12. These registers reflect the PWM duty cycle driving each fan at any given time. When in automatic fan speed control mode, the ADT7463 reports the PWM duty cycles back through these registers. The PWM duty cycle values vary according to temperature in automatic fan speed control mode. During fan startup, these registers report back 0x00. In software mode, the PWM duty cycle outputs can be set to any duty cycle value by writing to these registers.

Table 50. OPERATING POINT REGISTERS (POWER−ON DEFAULT = 0X64) (Note 13)

Register Address	R/W	Description
0x33	R/W	Remote 1 Operating Point Register (Default = 100 C)
0x34	R/W	Local Temp Operating Point Register (Default = 100 C)
0x35	R/W	Remote 2 Operating Point Register (Default = 100 C)

13. These

Table 51. REGISTER 0X36 − DYNAMIC T_{MIN} CONTROL REGISTER 1 (POWER−ON DEFAULT = 0X00) (Note 14)

Bit	Name	R/W	Description
<0>	CYR2	R/W	MSB of 3−bit Remote 2 Cycle Value. The other two bits of the code reside in Dynamic T_{MIN} Control Register 2 (Reg. 0x37). These three bits define the delay time between making subsequent T_{MIN} adjustments in the control loop, in terms of number of monitoring cycles. The system has associated thermal time constants that need to be found to optimize the response of fans and the control loop.
<1>	V_{CCP}LO	R/W	V_{CCP}LO = 1. When the power is supplied from 3.3 V STANDBY and the core voltage (V_{CCP}) drops below its V_{CCP} low limit value (Reg. 0x46), the following occurs: Status Bit 1 in Status Register 1 gets set $\overline{\text{SMBALERT}}$ gets generated if enabled $\overline{\text{PROCHOT}}$ monitoring is disabled Dynamic T_{MIN} control is disabled The device is prevented from entering shutdown Everything re

Table 52. REGISTER 0X37 − DYNAMIC T_{MIN} CONTROL REGISTER 2 (POWER−ON DEFAULT = 0X00) (Note 15)

Bit	Name	R/W	Description
<2:0>	CYR1	R/W	3−bit Remote 1 Cycle Value. These three bits define the delay time between making subsequent T_{MIN} adjustments in the control loop for the Remote 1 channel, in terms of number of monitoring

Table 53. REGISTER 0X40 − CONFIGURATION REGISTER 1 (POWER−ON DEFAULT = 0X00)

Bit	Name	R/W	Description
<0>	STRT	R/W	Logic 1 enables monitoring and PWM control outputs based on the limit settings programmed. Logic 0 disables monitoring and PWM control based on the default power−up limit settings. Note that the limit values programmed are preserved even if a Logic 0 is written to this bit and the default settings are enabled. This bit becomes read−only and cannot be changed once Bit 1 (LOCK bit) has been written. All limit registers should be programmed by BIOS before setting this bit to 1. (Lockable.)
<1>	LOCK	Write Once	Logic 1 locks all limit values to their current settings. Once this bit is set, all lockable registers become read−only and cannot be modified until the ADT7463 is powered down and powered up again. This prevents rogue programs such as viruses from modifying critical system limit settings. (Lockable.)
<2>	RDY	Read−only	This bit is set to 1 by the ADT7463 to indicate that the device is fully powered−up and ready to begin systems monitoring.
<3>	FSPD	R/W	When set to 1, all fans run at full speed. Power−on default = 0. (This bit cannot be locked.)
<4>	V I	R/W	BIOS should set this bit to a 1 when the ADT7463 is configured to measure current from an ADI ADOPT™ VRM controller and measure the CPU's core voltage. This allows monitoring software to display CPU watts usage. (Lockable.)
<5>	FSPDIS	R/W	Logic 1 disables fan spin−up for two TACH pulses. Instead, the PWM outputs go high for the entire fan spin−up timeout selected.
<6>	TODIS	R/W	When set to 1, the SMBus timeout feature is disabled. This allows the ADT7463 to be used with SMBus controllers that cannot handle SMBus timeouts. (Lockable.)
<7>	V_{CC}	R/W	When set to 1, the ADT7463 rescales its V_{CC} pin to measure a 5.0 V supply. When set to 0, the ADT7463 measures V_{CC} as a 3.3 V supply. (Lockable.)

Table 54. REGISTER 0X41 − INTERRUPT STATUS REGISTER 1 (POWER−ON DEFAULT = 0X00)

Bit	Name	R/W	Description
<0>	2.5V	Read−only	A 1 indicates that the 2.5 V high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<1>	V_{CCP}	Read−only	A 1 indicates the V_{CCP} high or low limit has been exceeded. This bit gets cleared on a read of the status register only if the error condition has subsided.
<2>	V_{CC}	Read−only	A 1 indicates that the V_{CC} high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<3>	5V	Read−only	A 1 indicates the 5 V high or low limit has been exceeded. This bit gets cleared on a read of the status register only if the error condition has subsided.
<4>	R1T	Read−only	A 1 indicates that the Remote 1 Low or High temperature limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<5>	LT	Read−only	A 1 indicates the Local Low or High temperature limit has been exceeded. This bit is cleared on a read of the Status Register only if the error condition has subsided.
<6>	R2T	Read−only	A 1 indicates that the Remote 2 Low or High temperature limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<7>	OOL	Read−only	A 1 indicates that an out−of−limit event has been latched in Status Register 2. This bit is a logical OR of all status bits in Status Register 2. Software can test this bit in isolation to determine whether any of the voltage, temperature, or fan speed readings represented by Status Register 2 are out−of−limit. This saves the need to read Status Register 2 every interrupt or polling cycle.

Table 55. REGISTER 0X42 − INTERRUPT STATUS REGISTER 2 (POWER−ON DEFAULT = 0X00)

Bit	Name	R/W	Description
<0>	12V/VC	Read−only	A one indicates the 12 V high or low limit has been exceeded. This bit gets cleared on a read of the status register only if the error condition has subsided. If Pin 21 is configured as VID5, this bit is the VID change bit. This bit gets set when the levels on VID0 to VID5 are different than they were 11 μs previously. This can be used to generate an $\overline{\text{SMBALERT}}$ whenever the VID code changes.
<1>	OVT	Read−only	A 1 indicates that one of the $\overline{\text{THERM}}$ overtemperature limits has been exceeded. This bit is cleared on a read of the status register when the temperature drops below $\overline{\text{THERM}}$ − T_{HYST}.
<2>	FAN1	Read−only	A 1 indicates that Fan 1 has dropped below minimum speed or has stalled. This bit is NOT set

Table 58. TEMPERATURE LIMIT REGISTERS (Note 18)

Register Address	R/W	Description (Note 19)	Power−On Default
0x4E	R/W	Remote 1 Temperature Low Limit	0x81
0x4F	R/W	Remote 1 Temperature High Limit	0x7F
0x50	R/W	Local Temperature Low Limit	0x81
0x51	R/W	Local Temperature High Limit	0x7F
0x52	R/W	Remote 2 Temperature Low Limit	0x81
0x53	R/W	Remote 2 Temperature High Limit	0x7F

18. Exceeding any of these temperature limits by 1 C causes the appropriate status bit to be set in the Interrupt Status Register. Setting the Configuration Register 1 Lock bit has no effect on these registers.
19. High limits: an interrupt is generated when a value exceeds its high limit (> comparison); Low limits: an interrupt is generated when a value is equal to or below its low limit (comparison).

Table 59. FAN TACHOMETER LIMIT REGISTERS (POWER−ON DEFAULT = 0XFF) (Note 20)

Register Address	R/W	Description
0x54	R/W	TACH1 Minimum Low Byte
0x55	R/W	TACH1 Minimum High Byte
0x56	R/W	TACH2 Minimum Low Byte
0x57	R/W	TACH2 Minimum High Byte
0x58	R/W	TACH3 Minimum Low Byte
0x59	R/W	TACH3 Minimum High Byte
0x5A	R/W	TACH4 Minimum Low Byte
0x5B	R/W	TACH4 Minimum High Byte

20. Exceeding any of the TACH limit registers by 1 indicates that the fan is running too slowly or has stalled. The appropriate status bit is set in Interrupt Status Register 2 to indicate the fan failure. Setting the Configuration Register 1 Lock bit has no effect on these registers.

Table 60. PWM CONFIGURATION REGISTERS (POWER−ON DEFAULT = 0X62) (Note 21)

Register Address	R/W	Description
0x5C	R/W	PWM1 Configuration
0x5D	R/W	PWM2 Configuration
0x5E		

ADT7463

Table 64. REGISTER 0X62 − ENHANCED ACOUSTICS REGISTER 1 (POWER−ON DEFAULT = 0X00) (Note 23)

Bit	Name	R/W	Description
<2:0>	ACOU	R/W	These bits select the ramp rate applied to the PWM1 output. Instead of PWM1 jumping instantaneously to its newly calculated speed, PWM1 ramps gracefully at the rate determined by these bits. This feature enhances the acoustics of the fan being driven by the PWM1 output. **Time Slot Increase** — **Time for 33% to 100%** 000 = 1 — 35 sec 001 = 2 — 17.6 sec 010 = 3 — 11.8 sec 011 = 4 — 7 sec 100 = 8 — 4.4 sec 101 = 12 — 3 sec 110 = 24 — 1.6 sec 111 = 48 — 0.8 sec
<3>	EN1	R/W	When this bit is 1, acoustic enhancement is enabled on PWM1 output.
<4>	SYNC	R/W	SYNC = 1 synchronizes fan speed measurements on TACH2, TACH3, and TACH4 to PWM3. This allows up to three fans to be driven from PWM3 output and their speeds to be measured. SYNC = 0, only TACH3 and TACH4 are synchronized to PWM3 output.
<5>	MIN1	R/W	When the ADT7463 is in automatic fan control mode, this bit defines whether PWM1 is off (0% duty cycle) or at PWM1 minimum duty cycle when the controlling temperature is below its T_{MIN} − Hysteresis value. 0 = 0% Duty Cycle below T_{MIN} − Hysteresis 1 = PWM1 Minimum Duty Cycle below T_{MIN} − Hysteresis
<6>	MIN2	R/W	When the ADT7463 is in automatic fan speed control mode, this bit defines whether PWM2 is off (0% duty cycle) or at PWM2 minimum duty cycle when the controlling temperature is below its T_{MIN} − Hysteresis value. 0 = 0% Duty Cycle below T_{MIN} − Hysteresis 1 = PWM2 Minimum Duty Cycle below T_{MIN} − Hysteresis
<7>	MIN3	R/W	When the ADT7463 is in automatic fan speed control mode, this bit defines whether PWM3 is off (0% duty cycle) or at PWM3 minimum duty cycle when the controlling temperature is below its T_{MIN}− Hysteresis value. 0 = 0% Duty Cycle below T_{MIN} − Hysteresis 1 = PWM3 Minimum Duty Cycle below T_{MIN} − Hysteresis

23. This register becomes read−only when the Configuration Register 1 Lock bit is set to 1. Further attempts to write to this register have no effect.

Table 65. REGISTER 0X63 − ENHANCED ACOUSTICS REGISTER 2 (POWER−ON DEFAULT = 0X00) (Note 24)

Bit	Name	R/W	Description
<2:0>	ACOU3	R/W	These bits select the ramp rate applied to the PWM3 output. Instead of PWM3 jumping instantaneously to its newly calculated speed, PWM3 ramps gracefully at the rate determined by these bits. This effect enhances the acoustics of the fan being driven by the PWM3 output. **Time Slot Increase** — **Time for 33% to 100%** 000 = 1 — 35 sec 001 = 2 — 17.6 sec 010 = 3 — 11.8 sec 011 = 4 — 7 sec 100 = 8 — 4.4 sec 101 = 12 — 3 sec 110 = 24 — 1.6 sec 111 = 48 — 0.8 sec
<3>	EN3	R/W	When this bit is 1, acoustic enhancement is enabled on PWM3 output.
<6:4>	ACOU2	R/W	These bits select the ramp rate applied to the PWM2 output. Instead of PWM2 jumping instantaneously to its newly calculated speed, PWM2 ramps gracefully at the rate determined by these bits. This effect enhances the acoustics of the fans being driven by the PWM2 output. **Time Slot Increase** — **Time for 33% to 100%** 000 = 1 — 35 sec 001 = 2 — 17.6 sec 010 = 3 — 11.8 sec 011 = 4 — 7 sec 100 = 8 — 4.4 sec 101 = 12 — 3 sec 110 = 24 — 1.6 sec 111 = 48 — 0.8 sec
<7>	EN2	R/W	When this bit is 1, acoustic enhancement is enabled on PWM2 output.

24. This register becomes read−only when the Configuration Register 1 Lock bit is set to 1. Further attempts to write to this register have no effect.

Table 66. PWM MIN DUTY CYCLE REGISTERS (Note 25)

Register Address	R/W	Description	Power−On Default
0x64	R/W	PWM1 Min Duty Cycle	0x80 (50% Duty Cycle)
0x65	R/W	PWM2 Min Duty Cycle	0x80 (50% Duty Cycle)
0x66	R/W	PWM3 Min Duty Cycle	0x80 (50% Duty Cycle)

25. These registers become read−only when the ADT7463 is in automatic fan control mode.

Table 67. PWM MIN DUTY CYCLE REGISTER BITS

Bit	Name	R/W	Description
<7:0>	PWM Duty Cycle	R/W	These bits define the PWM_{MIN} duty cycle for PWMx. 0x00 = 0% Duty Cycle (Fan Off) 0x40 = 25% Duty Cycle 0x80 = 50% Duty Cycle 0xFF = 100% Duty Cycle (Fan Full Speed)

Table 68. T_{MIN} REGISTERS (Note 26)

Register Address	R/W	**Description** (Note 27)	Power−On Default
0x67	R/W	Remote 1 Temperature T_{MIN}	0x5A (90 C)
0x68	R/W	Local Temperature T_{MIN}	0x5A (90 C)
0x69	R/W	Remote 2 Temperature T_{MIN}	0x5A (90 C)

Table 75. REGISTER 0X73 − CONFIGURATION REGISTER 2 (POWER−ON DEFAULT = 0X00) (Note 36)

Bit	Name	R/W	Description
0	AIN1	R/W	AIN1 = 0, Speed of 3−wire fans measured using the TACH output from the fan. AIN1 = 1, Pin 11 is reconfigured to measure the speed of 2−wire fans using an external sensing resistor and coupling capacitor. AIN voltage threshold is set via Configuration Register 4 (Reg. 0x7D).
1	AIN2	R/W	AIN2 = 0, Speed of 3−wire fans measured using the TACH output from the fan. AIN2 = 1, Pin 12 is reconfigured to measure the speed of 2−wire fans using an external sensing resistor and coupling capacitor. AIN voltage threshold is set via Configuration Register 4 (Reg. 0x7D).
2	AIN3	R/W	AIN3 = 0, Speed of 3−wire fans measured using the TACH output from the fan. AIN3 = 1, Pin 9 is reconfigured to measure the speed of 2−wire fans using an external sensing resistor and coupling capacitor. AIN voltage threshold is set via Configuration Register 4 (Reg. 0x7D).
3	AIN4	R/W	AIN4 = 0, Speed of 3−wire fans measured using the TACH output from the fan. AIN4 = 1, Pin 14 is reconfigured to measure the speed of 2−wire fans using an external sensing resistor and coupling capacitor. AIN voltage threshold is set via Configuration Register 4 (Reg. 0x7D).
4	AVG	R/W	AVG = 1, Averaging on the temperature and voltage measurements is turned off. This allows measurements on each channel to be made much faster.
5	ATTN	R/W	ATTN = 1, the ADT7463 removes the attenuators from the 2.5 V, V_{CCP}, 5 V, and 12 V inputs. The inputs can be used for other functions such as connecting up external sensors.
6	CONV	R/W	CONV = 1, the ADT7463 is put into a single−channel ADC conversion mode. In this mode, the ADT7463 can be made to read continuously from one input only, for example, Remote 1 temperature. It is also possible to start ADC conversions using an external clock on Pin 11 by setting Bit 2 of Test Register 2 (Reg. 0x7F). This mode could be useful if, for example, users wanted to characterize/profile CPU temperature quickly. The appropriate ADC channel is selected by writing to Bits <7:5> of TACH1 min high byte register (Reg. 0x55). **Bits <7:5> Reg. 0x55 — Channel Selected** 000 — 2.5V 001 — V_{CCP} 010 — V_{CC} (3.3V) 011 — 5V 100 — 12V 101 — Remote 1 Temp 110 — Local Temp 111 — Remote 2 Temp
7	SHDN	R/W	SHDN = 1, ADT7463 goes into shutdown mode. All PWM outputs assert low (or high depending, on state of INV bit) to switch off all fans. The PWM current duty cycle registers read 0x00 to indicate that the fans are not being driven.

36. This register becomes read−only when the Configuration Register 1 Lock bit is set to 1. Further attempts to write to this register have no effect.

Table 76. REGISTER 0X74 − INTERRUPT MASK REGISTER 1 (POWER−ON DEFAULT <7:0> = 0X00)

Bit	Name	R/W	Description
0	2.5V	R/W	A 1 masks $\overline{\text{SMBALERT}}$ for out−of−limit conditions on the 2.5 V channel.
1	V_{CCP}	R/W	A 1 masks $\overline{\text{SMBALERT}}$ for out−of−limit conditions on the V_{CCP} channel.
2	V_{CC}	R/W	A 1 masks $\overline{\text{SMBALERT}}$ for out−of−limit conditions on the V_{CC} channel.
3	5V	R/W	A 1 masks $\overline{\text{SMBALERT}}$ for out−of−limit conditions on the 5 V channel.

Table 77. REGISTER 0X75 − INTERRUPT MASK REGISTER 2 (POWER−ON DEFAULT = 0X00)

Bit	Name	R/W	Description
0			

Table 81. REGISTER 0X79 − $\overline{\text{THERM}}$ STATUS REGISTER (POWER−

Table 84. REGISTER 0X7D − CONFIGURATION REGISTER 4 (POWER−ON DEFAULT = 0X00) (Note 40)

Bit	Name	R/W	Description
<0>	AL2.5V	R/W	AL2.5V = 1, Pin 14 (2.5 V/$\overline{\text{SMBALERT}}$) is configured as an $\overline{\text{SMBALERT}}$ interrupt output to indicate out−of−limit error conditions. AL2.5V = 0, Pin 14 (2.5 V/$\overline{\text{SMBALERT}}$) is configured as a 2.5 V measurement input.
<1>	TH5V	R/W	TH5V = 1, Pin 20 (5V/$\overline{\text{THERM}}$) is configured as $\overline{\text{THERM}}$ pin. For $\overline{\text{THERM}}$ Monitoring, Bit 1 ($\overline{\text{THERM}}$ Timer) of Configuration Register 3 must also be set. TH5V = 0, Pin 20 (5V/$\overline{\text{THERM}}$) is configured as 5 V measurement input.
<3:2>	AINL	R/W	These two bits define the input threshold for 2−wire fan speed measurements: 00 = 20 mV 01 = 40 mV 10 = 80 mV 11 = 130 mV
<7:4>	RES		Unused.

40. This register becomes read−only when the Configuration Register 1 Lock bit is set to 1. Further attempts to write to this register have no effect.

Table 85. REGISTER 0X7E − MANUFACTURER'S TEST REGISTER 1 (POWER−ON DEFAULT = 0X00)

Bit	Name	R/W	Description
<7:0>	RES	Read−only	Manufacturer's Test Register. These bits are reserved for manufacturer's test purposes and should NOT be written to under normal operation.

Table 86. REGISTER 0X7F − MANUFACTURER'S TEST REGISTER 2 (POWER−ON DEFAULT = 0X00)

Bit	Name	R/W	Description
<7:0>	RES	Read−only	Manufacturer's Test Register. These bits are reserved for manufacturer's test purposes and should NOT be written to under normal operation.

Table 87. ORDERING INFORMATION

Device Number	Temperature Range	Package Type	Package Option	Shipping†
ADT7463ARQZ-REEL	−40 C to +120 C	24−lead QSOP	RQ−24	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*The "Z" suffix indicates Pb−Free part.

Pentium is a registered trademark of Intel Corporation.

QSOP24 NB
CASE 492B−01
ISSUE A

DATE 06 MAY 2008

SCALE 2:1