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Table 4. ELECTRICAL CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX} , unless otherwise noted.) (Notes 1, 2, 3, 4)

Parameter	Test Conditions/Comments	Min	Тур	Мах	Unit
ANALOG-TO-DIGITAL CONVERTER (INCLUDING MUX AND ATTENUATORS)					
Conversion Time (Local Temperature)	Averaging Enabled	-	12.09	13.50	ms
Conversion Time (Remote Temperature)	Averaging Enabled	-	25.59	28	

Parameter	Min	Тур	Max	Unit
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TYPICAL PERFORMANCE CHARACTERISTICS (CONT'D)



Figure 9. Supply Current vs. Supply Voltage



Figure 10. Remote Temperature Error vs. Differential–Mode Noise Frequency





FUNCTIONAL DESCRIPTION

General Description

The ADT7463 is a complete systems monitor and multiple fan controller for any system requiring monitoring and cooling. The device communicates with the system via a serial system management bus. The serial bus controller has an optional address line for device selection (Pin 14), a serial data line for reading and writing addresses and data (Pin 1), and an input line for the serial clock (Pin 2). All control and programming functions of the ADT7463 are performed over the serial bus. In addition, two of the pins can be reconfigured as an SMBALERT output to indicate out of limit conditions.

Measurement Inputs

The device has six measurement inputs, four for voltage and two for temperature. It can also measure its own supply voltage and can measure ambient temperature with its on chip temperature sensor.

Pins 20 through 23 are analog inputs with on chip attenuators, configured to monitor 5 V, 12 V, 2.5 V, and the processor core voltage (2.25 V input), respectively.

Power is supplied to the chip via Pin 4, and the system also monitors V_{CC} through this pin. In PCs, this pin is normally connected to a 3.3 V standby supply. This pin can, however, be connected to a 5 V supply and monitor it without overranging.

Remote temperature sensing is provided by the D1 and D2 inputs, to which diode connected, external temperature sensing transistors, such as a 2N3904 or CPU thermal diode, may be connected.

T_{RANGE} Registers

These registers program the temperature to fan speed control slope in automatic fan speed control mode for each PWM output.

Operating Point Registers

These registers define the target operating temperatures for each thermal zone when running under dynamic T_{MIN} control. This function allows the cooling solution to adjust dynamically in response to measured temperature and system performance.

Enhance Acoustics Registers

These registers allow each PWM output controlling fan to be tweaked to enhance the system's acoustics.

RECOMMENDED IMPLEMENTATION

SERIAL BUS INTERFACE

Control of the ADT7463 is carried out using the serial system management bus (SMBus). The ADT7463 is connected to this bus as a slave device, under the control of a master controller.

The ADT7463 has a 7 bit serial bus address. When the device is powered up with Pin 13 (PWM3/ ADDRESS ENABLE) high, the ADT7463 has a default SMBus address of 0101110 or 0x2E. The read/write bit must be added to get the 8 bit address. If more than one ADT7463 is used in a system, then each ADT7463 should be placed in address select mode by strapping Pin 13 low on power up. The logic state of Pin 14 then determines the device's SMBus address. The logic of these pins is sampled upon power up.

The device address is sampled and latched on the first valid SMBus transaction, more precisely on the low to high transition at the beginning of the 8th SCL pulse, when the serial bus address byte matches the selected slave address. The selected slave address is chosen using the address enable/address select pins. Any attempted changes in the address will have no effect after this.

Table 5. ADDRESS SELECT MODE

Pin 13 State	Pin 14 State	Address
0	Low (10 k Ω to GND)	0101100 (0x2C)
0	High (10 k Ω Pull–up)	0101101 (0x2D)
1	Don't Care	0101110 (0x2E) (Default)



ADDRESS = 0x2E

Figure 13. Default SMBus Address = 0x2E



ADDRESS = 0x2C

Figure 14. SMBus Address = 0x2C (Pin 14 = 0)



ADDRESS = 0x2D

Figure 15. SMBus Address = 0x2D (Pin 14 = 1)



CARE SHOULD BE TAKEN TO ENSURE THAT PIN 13 (PWM3/ADDR_EN) IS EITHER TIED HIGH OR LOW. LEAVING PIN 13 FLOATING COULD CAUSE THE ADT7463 TO POWERUP WITH AN UNEXPECTED ADDRESS.

NOTE THAT IF THE ADT7463 IS PLACED INTO ADDRESS SELECT MODE, PINS 13 AND 14 CAN BE USED AS THE ALTERNATE FUNCTIONS (PWM3, TACH4/THERM) ONLY IF THE CORRECT CIRCUIT IS MUXED IN AT THE CORRECT TIME.

Figure 16. Unpredictable SMBus Address if Pin 13 is Unconnected

The ability to make hardwired changes to the SMBus slave address allows the user to avoid conflicts with other devices sharing the same serial bus, for example, if more than one ADT7463 is used in a system.

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, defined as a high to low transition on the serial data line SDA while the serial clock line SCL remains high. This indicates that an address/data stream will follow. All slave peripherals connected to the serial bus respond to the START condition and shift in the next eight bits, consisting of a 7 bit address (MSB first) plus a R/W bit, which determines the direction of the data transfer, i.e., whether data will be written to or read from the slave device.

The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the Acknowledge Bit. All

other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/\overline{W} bit is a 0, then the master writes to the slave device. If the R/\overline{W} bit is a 1, the master reads from the slave device.

2. Data is sent over the serial bus in sequences of nine clock pulses, eight bits of data followed by an Acknowledge Bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low to high transition when the clock is high may be interpreted as a STOP signal. The number of data bytes that can be





When reading data from a register, there are two possibilities:

1. If the ADT7463's address pointer register value is unknown or not the desired value, it is first necessary to set it to the correct value before data can be read from the desired data register. This is done by performing a write to the ADT7463 as before, however, only the data byte is sent and this contains the register address. This is shown in Figure 18.

A read operation is then performed consisting of the serial bus address, R/W bit set to 1, followed by the data byte read from the data register. This is shown in Figure 19.

2. If the address pointer register is already at the desired address, data can be read from the corresponding data register without first writing to the address pointer register, so Figure 18 can be omitted.

NOTES:

- It is possible to *read* a data byte from a data register without first writing to the address pointer register if the address pointer register is already at the correct value. However, it is not possible to *write* data to a register without writing to the address pointer register because the first data byte of a write is always written to the address pointer register.
- In Figures 17 to 19, the serial bus address is shown as the default value 01011(A1)(A0), where A1 and A0 are set by the address select mode function previously defined.
- In addition to supporting the Send Byte and Receive Byte protocols, the ADT7463 also supports the Read Byte protocol (see System Management Bus specifications Rev. 2.0 for more information).
- 4. If it is required to perform se.

4

ADT7463 READ OPERATIONS

The ADT7463 uses the following SMBus read protocols.

Receive Byte

This is useful when repeatedly reading a single register. The register address needs to have been set up previously. In this operation, the master device receives a single byte from a slave device as follows:

- 1. The master device asserts a start condition on SDA
- 2. The master sends the 7 bit slave address followed by the read bit (high)
- 3. The addressed slave device asserts ACK on SDA
- 4. The master receives a data byte
- 5. The master asserts NO ACK on SDA
- 6. The master asserts a stop condition on SDA and the transaction ends

In the ADT7463, the receive byte protocol is used to read a single byte of data from a register whose address has previously been set by a send byte or write byte operation.



Figure 22. Single Byte Read from a Register

ALERT RESPONSE ADDRESS

Alert response address (ARA) is a feature of SMBus devices that allows an interrupting device to identify itself to the host when multiple devices exist on the same bus.

The SMBALERT output can be used as an interrupt output or can be used as an SMBALERT. One or more outputs can be connected to a common SMBALERT line connected to the master. If a device's SMBALERT line goes low, the following procedure occurs:

- 1. SMBALERT is pulled low
- Master initiates a read operation and sends the alert response address (ARA = 0001 100). This is a general call address that must not be used as a specific device address
- 3. The device whose SMBALERT output is low responds to the alert response address, and the master reads its device address. The address of the device is now known and it can be interrogated in the usual way
- 4. If more than one device's SMBALERT output is low, the one with the lowest device address will have priority in accordance with normal SMBus arbitration
- 5. Once the ADT7463 has responded to the alert response address, the master must read the status registers and the SMBALERT will only be cleared if the error condition has gone away

SMBUS TIMEOUT

The ADT7463 includes an SMBus timeout feature. If there is no SMBus activity for 35 ms, the ADT7463 assumes

that the bus is locked and releases the bus. This prevents the device from locking or holding the SMBus expecting data. Some SMBus controllers cannot handle the SMBus timeout feature, so it can be disabled.

Table 6. CONFIGURATION REGISTER 1 (REG. 0X40)

Bit	Description

Input Voltage				A/D Output		
+12V _{IN}	+5V _{IN}	V _{CC} (3.3V _{IN}) (Note 6)	+2.5V _{IN}	+V _{CCP}	Decimal	Binary (10 Bits)
<0.0156	<0.0065	<0.0042	<0.0032	<0.00293	0	00000000 00
0.0156-0.0312	0.0065–0.0130	0.0042-0.0085	0.0032-0.0065	0.0293-0.0058	1	0000000 01
0.0312-0.0469	0.0130-0.0195	0.0085-0.0128	0.0065-0.0097	0.0058-0.0087	2	00000000 10
0.0469–0.0625	0.0195–0.0260	0.0128-0.0171	0.0097–0.0130	0.0087–0.0117	3	00000000 11
0.0625-0.0781	0.0260-0.0325	0.0171-0.0214	0.0130-0.0162	0.0117–0.0146	4	0000001 00
0.0781-0.0937	0.0325-0.0390	0.0214-0.0257	0.0162-0.0195	0.0146–0.0175	5	0000001 01
0.0937–0.1093	0.0390-0.0455	0.0257-0.0300	0.0195-0.0227	0.0175–0.0205	6	00000001 10
0.1093–0.1250	0.0455-0.0521	0.0300-0.0343	0.0227-0.0260	0.0205–0.0234	7	00000001 11
0.1250–0.14060	0.0521–0.0586	0.0343–0.0386	0.0260–0.0292	0.0234–0.0263	8	00000010 00
4.0000-4.0156	1.6675–1.6740	1.1000–1.1042	0.8325–0.8357	0.7500–0.7529	256 (1/4 Scale)	0100000 00
8.0000-8.0156	3.3300–3.3415	2.2000–2.2042	1.6650–1.6682	1.5000–1.5029	512 (1/2 Scale)	1000000 00
12.0000–12.0156	5.0025–5.0090	3.3000–3.3042	2.4975–2.5007	2.2500–2.2529	768 (3/4 Scale)	11000000 00
15.8281–15.8437	6.5983–6.6048	4.3527-4.3570	3.2942-3.2974	2.9677–2.9707	1013	11111101 01
15.8437–15.8593	6.6048–6.6113	4.3570-4.3613	3.2974–3.3007	2.9707–2.9736	1014	11111101 10
15.8593-15.8750	6.6113–6.6178	4.3613-4.3656	3.3007–3.3039	2.9736–2.9765	1015	11111101 11
15.8750-15.8906	6.6178–6.6244	4.3656-4.3699	3.3039–3.3072	2.9765–2.9794	1016	11111110 00
15.8906-15.9062	6.6244–6.6309	4.3699–4.3742	3.3072-3.3104	2.9794–2.9824	1017	11111110 01
15.9062-15.9218	6.6309–6.6374	4.3742-4.3785	3.3104–3.3137	2.9824–2.9853	1018	11111110 10
15.9218–15.9375	6.6374–6.4390	4.3785-4.3828	3.3137–3.3169	2.9853–2.9882	1019	11111110 11
15.9375–15.9531	6.6439–6.6504	4.3828-4.3871	3.3169–3.3202	2.9882–2.9912	1020	11111111 00
15.9531–15.9687	6.6504–6.6569	4.3871–4.3914	3.3202-3.3234	2.9912–2.9941	1021	11111111 01
15.9687–15.9843	6.6569–6.6634	4.3914–4.3957	3.3234–3.3267	2.9941–2.9970	1022	11111111 10
>15.9843	>6.6634	>4.3957	>3.3267	>2.9970	1023	11111111 11

Table 12. 10-BIT A/D OUTPUT CODE VS. VIN

6. The V_{CC} output codes listed assume that V_{CC} is 3.3 V. If V_{CC} input is reconfigured for 5 V operation (by setting Bit 7 of Configuration Register 1), then the V_{CC} output codes are the same as for the +5V_{IN} column.

VID CODE CHANGE DETECT FUNCTION

The ADT7463 has a VID code change detect function. When Pin 21 is configured as the VID5 input, VID code changes can be detected and reported back by the ADT7463. Bit 0 of Status Register 2 (Reg. 0x42) is the 12V/VC bit and denotes a VID change when set. The VID code change bit gets set when the logic states on the VID inputs are different than they were 11 μ s previously. The change of VID code can be used to generate an SMBALERT interrupt. If an SMBALERT interrupt is not required, Bit 0 of Interrupt Mask Register 2 (Reg. 0x75), when set, prevents SMBALERTs from occurring on VID code changes.

Table 13. STATUS REGISTER (REG. 0X42)

Bit	Description
<0> 12V/VC	0: If Pin 21 is configured as VID5, then a Logic 0 denotes no change in VID code within last 11 μ s.
	1: If Pin 21 is configured as VID5, then a Logic 1 means that a change has occurred on the VID code inputs within the last 11 μ s. An SMBALERT generates if this function is enabled.

ADDITIONAL ADC FUNCTIONS FOR VOLTAGE MEASUREMENT

A number of other functions are available on the ADT7463 to offer the systems designer increased flexibility, including:

Turn-off Averaging

Figure 24 shows the input signal conditioning used to measure the output of a remote temperature sensor. This figure shows the external sensor as a substrate transistor,

provided for temperature monitoring on some microprocessors. It could equally well be a discrete transistor, such as a 2N3904.

ADDITIONAL ADC FUNCTIONS FOR TEMPERATURE MEASUREMENT

A number of other functions are available on the ADT7463 to offer the systems designer increased flexibility.

Turn-off Averaging

For each temperature measurement read from a value register, 16 readings have actually been made internally and the results averaged before being placed into the value register. Sometimes it may be necessary to take a very fast measurement, e.g., of CPU temperature. Setting Bit 4 of Configuration Register 2 (Reg. 0x73) turns averaging off. This takes a reading every 13 ms. The measurement itself takes 4 ms.

Single-channel ADC Conversions

Setting Bit 6 of Configuration Register 2 (Reg. 0x73) places the ADT7463 into single channel ADC conversion mode. In this mode, the ADT7463 can be made to read a single temperature channel only. If the internal ADT7463 clock is used, the selected input is read every 1.4 ms. The appropriate ADC channel is selected by writing to Bits <7:5> of TACH1 Minimum High Byte Register (0x55).

Table 21. CONFIGURATION REGISTER 2 (REG. 0X73)

Bit	Description
<4>	1: Averaging Off
<6>	1: Single-channel Convert Mode

Table 22. TACH1 MINIMUM HIGH BYTE (REG. 0X55)

Bit	Description			
<7:5>	Selects ADC Single-channel	Selects ADC Channel for Single-channel Convert Mode		
	Value	Channel Selected		
	101	Remote 1 Temp		
	110	Local Temp		
	111	Remote 2 Temp		

LIMITS, STATUS REGISTERS, AND INTERRUPTS

Limit Values

Associated with each measurement channel on the ADT7463 are high and low limits. These can form the basis of system status monitoring: a status bit can be set for any out of limit condition and detected by polling the device. Alternatively, SMBALERT interrupts can be generated to flag a processor or microcontroller of out of limit conditions.

8-bit Limits

The following is a list of 8 bit limits on the ADT7463.

Table 23. VOLTAGE LIMIT REGISTERS

Register	Description	Default
0x44	2.5 V Low Limit	0x00
0x45	2.5 V High Limit	0xFF
0x46	V _{CCP} Low Limit	0x00
0x47	V _{CCP} High Limit	0xFF
0x48	V _{CC} Low Limit	0x00
0x49	V _{CC} High Limit	0xFF
0x4A	5 V Low Limit	0x00
0x4B	5 V High Limit	0xFF
0x4C	12 V Low Limit	0x00
0x4D	12 V High Limit	0xFF

Table 24. TEMPERATURE LIMIT REGISTERS

Register	Description	Default
0x4E	Remote 1 Temperature Low Limit	0x81
0x4F	Remote 1 Temperature High Limit	0x7F
0x6A	Remote 1 THERM Limit	0x64
0x50	Local Temperature Low Limit	0x81
0x51	Local Temperature High Limit	0x7F
0x6B	Local THERM Limit	0x64
0x52	Remote 2 Temperature Low Limit	0x81
0x53	Remote 2 Temperature High Limit	0x7F
0x6C	Remote 2 THERM Limit	0x64

Description

Table 25. THERM LIMIT REGISTERS

Register

Default



Figure 31. Temperature > High Limit: INT Occurs

Analog Monitoring Cycle Time

The analog monitoring cycle begins when a 1 is written to the start bit (Bit 0) of Configuration Register 1 (Reg. 0x40). The ADC measures each analog input in turn and as each measurement is completed, the result is automatically stored in the appropriate value register. This round robin monitoring cycle continues unless disabled by writing a 0 to Bit 0 of Configuration Register 1.

Because the ADC is normally left to free run in this manner, the time taken to monitor all the analog inputs is normally not of interest, since the most recently measured value of any input can be read out at any time.

For applications where the monitoring cycle time is important, it is easily calculated.

The total number of channels measured is: Four Dedicated Supply Voltage Inputs $3.3~\rm V_{\rm STBY}$

SMBALERT Interrupt Behavior

The ADT7463 can be polled for status, or an <u>SMBALERT</u> interrupt can be generated for out of limit conditions. It is important to note how the <u>SMBALERT</u> output and status bits behave when writing Interrupt Handler software.



Figure 34. SMBALERT and Status Bit Behavior

Figure 34 shows how the SMBALERT output and "sticky" status bits behave. Once a limit is exceeded, the corresponding status bit gets set to 1. The status bit remains set until the error condition subsides and the status register gets read. The status bits are referred to as sticky since they remain set until read by software. This ensures that an out of limit event cannot be missed if software is polling the device periodically. Note that the SMBALERT output remains low for the entire duration that a reading is out of limit and until the status register has been read. This has implications on how software handles the interrupt.

Handling SMBALERT Interrupts

To prevent the system from being tied up servicing interrupts, it is recommend to handle the SMBALERT interrupt as follows:

- 1. Detect the SMBALERT assertion.
- 2. Enter the interrupt handler.
- 3. Read the status registers to identify the interrupt source.



 Mask the interrupt source by setting the appropriate mask bit in the interrupt mask registers (Reg. 0x74, 0x75). 5. Take the appropriate action for a given interrupt source.



Figure 37. Understanding the THERM Timer

When using the THERM timer, be aware of the following: After a THERM timer read (Reg. 0x79):

- 1. The contents of the timer get cleared on read.
- 2. The F4P bit (Bit 5) of Status Register 2 needs to be cleared (assuming the THERM limit has been exceeded).

If the THERM timer is read during a THERM assertion, then the following will happen:

- 1. The contents of the timer are cleared.
- 2. Bit 0 of the THERM timer is set to 1 (since a THERM assertion is occurring).
- 3. The THERM timer increments from zero.
- 4. If the THERM limit (Reg. 0x7A) = 0x00, then the F4P bit gets set.

Generating SMBALERT Interrupts from THERM Events

The ADT7463 can generate SMBALERTs when a programmable THERM limit has been exceeded. This allows the systems designer to ignore brief, infrequent THERM assertions, while capturing longer THERM events. Register 0x7A is the THERM Limit Register. This 8 bit register allows a limit from 0 seconds (first THERM assertion) to 5.825 seconds to be set before an SMBALERT is generated. The THERM timer value is compared with the contents of the THERM limit register. If the THERM timer value exceeds the THERM limit value, then the F4P bit (Bit 5) of Status Register 2 gets set, and an SMBALERT is generated. Note that the F4P bit (Bit 5) of Mask Register 2 (Reg. 0x75) masks out SMBALERTs if this bit is set to 1, although the F4P bit of Interrupt Status Register 2 still gets set if the THERM limit is exceeded.



Figure 38. Functional Diagram of the ADT7463 THERM Monitoring Circuitry

PWM3 so PWM3 can drive 2 fans. Alternatively, PWM2 can be programmed to synchronize TACH2, TACH3, and TACH4 to the PWM2 output. This allows PWM2 to drive two or three fans. In this case, the drive circuitry looks the same as shown in Figures 42 and 43. The SYNC bit in Register 0x62 enables this function.

Table 33. SYNC: ENHANCE ACOUSTICS REGISTER 1 (REG. 0X62)

Bit	Mnemonic	Description
<4>	SYNC	1 Synchronizes TACH2, TACH3, and TACH4 to PWM2.

Driving 2-wire Fans Figure 44 shows how a 2 The maximum input signal range is $0 \vee to 5 \vee V$, even where \vee_{CC} is less than 5 \vee . In the event that these inputs are supplied from fan outputs that exceed $0 \vee to 5 \vee$, either resistive attenuation of the fan signal or diode clamping must be included to keep inputs within an acceptable range.

Figures 47 to 50 show circuits for most common fan TACH outputs.

If the fan TACH output has a resistive pull up to V_{CC} , it can be connected directly to the fan input, as shown in Figure 47.



Figure 47. Fan with TACH Pull-up to V_{CC}

allowing one, two (default), three, or four TACH pulses to be counted.

The fan tachometer readings are 16 bit values consisting of a 2 byte read from the ADT7463.

Register	Description	Default
0x28	TACH1 Low Byte	0x00
0x29	TACH1 High Byte	0x00
0x2A	TACH2 Low Byte	0x00
0x2B	TACH2 High Byte	0x00
0x2C	TACH3 Low Byte	0x00
0x2D	TACH3 High Byte	0x00
0x2E	TACH4 Low Byte	0x00
0x2F	TACH4 High Byte	0x00

Reading Fan Speed from the ADT7463

If fan speeds are being measured, this involves a

2 register read for each measurement. The low byte should

be read first. This causes the high byte to be frozen until both

high and low byte registers have been read from. This0001 Tc.209 ubeen read from. Thissssy2e8 0 0 8 49071 Ite

the lowest ripple determines the correct pulses/revolution value.

Table 36. FAN PULSES PER REVOLUTION REGISTER (REG. 0X7B)

Bit	Mnemonic	Description
<1:0>	FAN1 Default	2 Pulses per Revolution
<3:2>	FAN2 Default	2 Pulses per Revolution
<5:4>	FAN3 Default	2 Pulses per Revolution
<7:6>	FAN4 Default	2 Pulses per Revolution

Table 37. FAN PULSES PER REVOLUTION REGISTER BIT VALUES

Value	Description
00	1 Pulse per Revolution
01	2 Pulses per Revolution
10	3 Pulses per Revolution
11	4 Pulses per Revolution

and without CPU intervention, once initial parameters are set up. The advantage of this is in the case of the system hanging, the user is guaranteed that the system is protected from overheating. The automatic fan speed control incorporates a feature called dynamic $T_{\rm MIN}$ calibration. This feature reduces the design effort required to program the automatic

XOR TREE TEST MODE

The ADT7463 includes an XOR Tree Test Mode. This mode is useful for in circuit test equipment at board level testing. By applying stimulus to the pins included in the XOR Tree, it is possible to detect opens or shorts on the system board. Figure 53 shows the signals that are exercised in the XOR Tree Test Mode.



Figure 53. XOR Tree Test

Table 45. ADT7463 REGISTERS

Addr	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Defaul t	Locka ble
0x32	R/W	PWM3 Current Duty Cycle	7	6	5	4	3	2	1	0	0xFF	
0x33	R/W	Remote 1 Operating Point	7	6	5	4	3	2	1	0	0x64	YES
0x34	R/W	Local Temp Operating Point	7	6	5	4	3	2	1	0	0x64	YES
0x35	R/W	Remote 2 Operating Point	7	6	5	4	3	2	1	0	0x64	YES
0x36	R/W	Dynamic T _{MIN} Control Reg 1	R2T	LT	R1T	PHTR2	PHTL	PHTR1	V _{CCP} LO	CYR2	0x00	YES

0x37

Table 45. ADT7463 REGISTERS

Addr	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Defaul t	Locka ble
0x59	R/W	TACH3 Minimum High Byte	15	14	13	12	11	10	9	8	0xFF	
0x5A	R/W	TACH4 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	
0x5B	R/W	TACH4 Minimum High Byte	15	14	13	12	11	10				

Table 45. ADT7463 REGISTERS

Addr	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Defaul t	Locka ble	
0x7A	R/W	THERM Limit Reg.											
0x7B	R/W	Fan Pulses per Revolution	FAN4										

Table 49. CURRENT PWM DUTY CYCLE REGISTERS (POWER-ON DEFAULT = 0XFF) (Note 12)

Register Address	R/W	Description
0x30	R/W	PWM1 Current Duty Cycle (0% to 100% Duty Cycle = 0x00 to 0xFF).
0x31	R/W	PWM2 Current Duty Cycle (0% to 100% Duty Cycle = 0x00 to 0xFF).
0x32	R/W	PWM3 Current Duty Cycle (0% to 100% Duty Cycle = 0x00 to 0xFF).

12. These registers reflect the PWM duty cycle driving each fan at any given time. When in automatic fan speed control mode, the ADT7463 reports the PWM duty cycles back through these registers. The PWM duty cycle values vary according to temperature in automatic fan speed control mode. During fan startup, these registers report back 0x00. In software mode, the PWM duty cycle outputs can be set to any duty cycle value by writing to these registers.

Table 50. OPERATING POINT REGISTERS (POWER-ON DEFAULT = 0X64) (Note 13)

Register Address	R/W	Description
0x33	R/W	Remote 1 Operating Point Register (Default = 100 C)
0x34	R/W	Local Temp Operating Point Register (Default = 100 C)
0x35	R/W	Remote 2 Operating Point Register (Default = 100 C)

13. These

Table 51. REGISTER 0X36 – DYNAMIC T_{MIN} CONTROL REGISTER 1 (POWER–ON DEFAULT = 0X00) (Note 14)

Bit	Name	R/W	Description
<0>	CYR2	R/W	MSB of 3–bit Remote 2 Cycle Value. The other two bits of the code reside in Dynamic T_{MIN} Control Register 2 (Reg. 0x37). These three bits define the delay time between making subsequent T_{MIN} adjustments in the control loop, in terms of number of monitoring cycles. The system has associated thermal time constants that need to be found to optimize the response of fans and the control loop.
<1>	V _{CCP} LO	R/W	$\label{eq:V_CCP} V_{CCP} LO = 1. When the power is supplied from 3.3 V STANDBY and the core voltage (V_{CCP}) drops below its V_{CCP} low limit value (Reg. 0x46), the following occurs: Status Bit 1 in Status Register 1 gets set SMBALERT gets generated if enabled PROCHOT monitoring is disabled Dynamic T_{MIN} control is disabled The device is prevented from entering shutdown Everything re$

Table 52. REGISTER 0X37 – DYNAMIC T_{MIN} CONTROL REGISTER 2 (POWER–ON DEFAULT = 0X00) (Note 15)

<2:0> CYR1 R/W 3-bit Remote 1 Cycle Value. These three bits define the delay time between making T _{MIN} adjustments in the control loop for the Remote 1 channel, in terms of number of the Remote 1 channel.	g subsequent of monitoring

Table 53. REGISTER 0X40 - CONFIGURATION REGISTER 1 (POWER-ON DEFAULT = 0X00)

Bit	Name	R/W	Description
<0>	STRT	R/W	Logic 1 enables monitoring and PWM control outputs based on the limit settings programmed. Logic 0 disables monitoring and PWM control based on the default power–up limit settings. Note that the limit values programmed are preserved even if a Logic 0 is written to this bit and the default settings are enabled. This bit becomes read–only and cannot be changed once Bit 1 (LOCK bit) has been written. All limit registers should be programmed by BIOS before setting this bit to 1. (Lockable.)
<1>	LOCK	Write Once	Logic 1 locks all limit values to their current settings. Once this bit is set, all lockable registers become read–only and cannot be modified until the ADT7463 is powered down and powered up again. This prevents rogue programs such as viruses from modifying critical system limit settings. (Lockable.)
<2>	RDY	Read-only	This bit is set to 1 by the ADT7463 to indicate that the device is fully powered–up and ready to begin systems monitoring.
<3>	FSPD	R/W	When set to 1, all fans run at full speed. Power-on default = 0. (This bit cannot be locked.)
<4>	VI	R/W	BIOS should set this bit to a 1 when the ADT7463 is configured to measure current from an ADI ADOPT [™] VRM controller and measure the CPU's core voltage. This allows monitoring software to display CPU watts usage. (Lockable.)
<5>	FSPDIS	R/W	Logic 1 disables fan spin-up for two TACH pulses. Instead, the PWM outputs go high for the entire fan spin-up timeout selected.
<6>	TODIS	R/W	When set to 1, the SMBus timeout feature is disabled. This allows the ADT7463 to be used with SMBus controllers that cannot handle SMBus timeouts. (Lockable.)
<7>	V _{cc}	R/W	When set to 1, the ADT7463 rescales its V_{CC} pin to measure a 5.0 V supply. When set to 0, the ADT7463 measures V_{CC} as a 3.3 V supply. (Lockable.)

Table 54. REGISTER 0X41 - INTERRUPT STATUS REGISTER 1 (POWER-ON DEFAULT = 0X00)

Bit	Name	R/W	Description
<0>	2.5V	Read-only	A 1 indicates that the 2.5 V high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<1>	V _{CCP}	Read-only	A 1 indicates the V_{CCP} high or low limit has been exceeded. This bit gets cleared on a read of the status register only if the error condition has subsided.
<2>	V _{CC}	Read-only	A 1 indicates that the V_{CC} high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<3>	5V	Read-only	A 1 indicates the 5 V high or low limit has been exceeded. This bit gets cleared on a read of the status register only if the error condition has subsided.
<4>	R1T	Read-only	A 1 indicates that the Remote 1 Low or High temperature limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<5>	LT	Read-only	A 1 indicates the Local Low or High temperature limit has been exceeded. This bit is cleared on a read of the Status Register only if the error condition has subsided.
<6>	R2T	Read-only	A 1 indicates that the Remote 2 Low or High temperature limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<7>	OOL	Read-only	A 1 indicates that an out–of–limit event has been latched in Status Register 2. This bit is a logical OR of all status bits in Status Register 2. Software can test this bit in isolation to determine whether any of the voltage, temperature, or fan speed readings represented by Status Register 2 are out–of–limit. This saves the need to read Status Register 2 every interrupt or polling cycle.

Table 55. REGISTER 0X42 – INTERRUPT STATUS REGISTER 2 (POWER–ON DEFAULT = 0X00)

Bit	Name	R/W	Description
<0>	12V/VC	Read-only	A one indicates the 12 V high or low limit has been exceeded. This bit gets cleared on a read of the status register only if the error condition has subsided. If Pin 21 is configured as VID5, this bit is the VID change bit. This bit gets set when the levels on VID0 to VID5 are different than they were 11 μs previously. This can be used to generate an SMBALERT whenever the VID code changes.
<1>	OVT	Read-only	A 1 indicates that one of the THERM overtemperature limits has been exceeded. This bit is cleared on a read of the status register when the temperature drops below THERM – T_{HYST} .
<2>	FAN1	Read-only	A 1 indicates that Fan 1 has dropped below minimum speed or has stalled. This bit is NOT set

Table 58. TEMPERATURE LIMIT REGISTERS (Note 18)

Register Address	R/W	Description (Note 19)	Power-On Default
0x4E	R/W	Remote 1 Temperature Low Limit	0x81
0x4F	R/W	Remote 1 Temperature High Limit	0x7F
0x50	R/W	Local Temperature Low Limit	0x81
0x51	R/W	Local Temperature High Limit	0x7F
0x52	R/W	Remote 2 Temperature Low Limit	0x81
0x53	R/W	Remote 2 Temperature High Limit	0x7F

18. Exceeding any of these temperature limits by 1 C causes the appropriate status bit to be set in the Interrupt Status Register. Setting the Configuration Register 1 Lock bit has no effect on these registers.

19. High limits: an interrupt is generated when a value exceeds its high limit (> comparison); Low limits: an interrupt is generated when a value is equal to or below its low limit (comparison).

Table 59. FAN TACHOMETER LIMIT REGISTERS (POWER-ON DEFAULT = 0XFF) (Note 20)

Register Address	R/W	Description
0x54	R/W	TACH1 Minimum Low Byte
0x55	R/W	TACH1 Minimum High Byte
0x56	R/W	TACH2 Minimum Low Byte
0x57	R/W	TACH2 Minimum High Byte
0x58	R/W	TACH3 Minimum Low Byte
0x59	R/W	TACH3 Minimum High Byte
0x5A	R/W	TACH4 Minimum Low Byte
0x5B	R/W	TACH4 Minimum High Byte

20. Exceeding any of the TACH limit registers by 1 indicates that the fan is running too slowly or has stalled. The appropriate status bit is set in Interrupt Status Register 2 to indicate the fan failure. Setting the Configuration Register 1 Lock bit has no effect on these registers.

Table 60. PWM CONFIGURATION REGISTERS (POWER-ON DEFAULT = 0X62) (Note 21)

Register Address	R/W	Description
0x5C	R/W	PWM1 Configuration
0x5D	R/W	PWM2 Configuration
0x5E	ſ	

Table 64. REGISTER 0X62 - ENHANCED ACOUSTICS REGISTER 1 (POWER-ON DEFAULT = 0X00) (Note 23)

Bit	Name	R/W	Description	
<2:0>	ACOU	R/W	These bits select the ramp rate applied to the PWM1 output. Instead of PWM1 jumping instantaneously to its newly calculated speed, PWM1 ramps gracefully at the rate determined by these bits. This feature enhances the acoustics of the fan being driven by the PWM1 output.	
			Time Slot IncreaseTime for 33% to 100%000 = 135 sec001 = 217.6 sec010 = 311.8 sec011 = 47 sec100 = 84.4 sec101 = 123 sec110 = 241.6 sec111 = 480.8 sec	
<3>	EN1	R/W	When this bit is 1, acoustic enhancement is enabled on PWM1 output.	
<4>	SYNC	R/W	SYNC = 1 synchronizes fan speed measurements on TACH2, TACH3, and TACH4 to PWM3. This allows up to three fans to be driven from PWM3 output and their speeds to be measured. SYNC = 0, only TACH3 and TACH4 are synchronized to PWM3 output.	
<5>	MIN1	R/W	When the ADT7463 is in automatic fan control mode, this bit defines whether PWM1 is off (0% duty cycle) or at PWM1 minimum duty cycle when the controlling temperature is below its T_{MIN} – Hysteresis value. 0 = 0% Duty Cycle below T_{MIN} – Hysteresis 1 = PWM1 Minimum Duty Cycle below T_{MIN} – Hysteresis	
<6>	MIN2	R/W	When the ADT7463 is in automatic fan speed control mode, this bit defines whether PWM2 is off (0% duty cycle) or at PWM2 minimum duty cycle when the controlling temperature is below its T_{MIN} – Hysteresis value. 0 = 0% Duty Cycle below T_{MIN} – Hysteresis 1 = PWM2 Minimum Duty Cycle below T_{MIN} – Hysteresis	
<7>	MIN3	R/W	When the ADT7463 is in automatic fan speed control mode, this bit defines whether PWM3 is off (0% duty cycle) or at PWM3 minimum duty cycle when the controlling temperature is below its T_{MIN} - Hysteresis value. 0 = 0% Duty Cycle below T_{MIN} - Hysteresis 1 = PWM3 Minimum Duty Cycle below T_{MIN} - Hysteresis	

23. This register becomes read-only when the Configuration Register 1 Lock bit is set to 1. Further attempts to write to this register have no effect.

Table 65. REGISTER 0X63 - ENHANCED ACOUSTICS REGISTER 2 (POWER-ON DEFAULT = 0X00) (Note 24)

Bit	Name	R/W	Description
<2:0>	ACOU3	R/W	These bits select the ramp rate applied to the PWM3 output. Instead of PWM3 jumping instantaneously to its newly calculated speed, PWM3 ramps gracefully at the rate determined by these bits. This effect enhances the acoustics of the fan being driven by the PWM3 output.
			Time Slot IncreaseTime for 33% to 100%000 = 135 sec001 = 217.6 sec010 = 311.8 sec011 = 47 sec100 = 84.4 sec101 = 123 sec110 = 241.6 sec111 = 480.8 sec
<3>	EN3	R/W	When this bit is 1, acoustic enhancement is enabled on PWM3 output.
<6:4>	ACOU2	R/W	These bits select the ramp rate applied to the PWM2 output. Instead of PWM2 jumping instantaneously to its newly calculated speed, PWM2 ramps gracefully at the rate determined by these bits. This effect enhances the acoustics of the fans being driven by the PWM2 output.Time Slot IncreaseTime for 33% to 100% $000 = 1$ 35 sec $001 = 2$ 17.6 sec $011 = 3$ 11.8 sec $011 = 4$ 7 sec $100 = 8$ 4.4 sec $101 = 12$ 3 sec $111 = 48$ 0.8 sec
<7>	EN2	R/W	When this bit is 1, acoustic enhancement is enabled on PWM2 output.

24. This register becomes read-only when the Configuration Register 1 Lock bit is set to 1. Further attempts to write to this register have no effect.

Table 66. PWM MIN DUTY CYCLE REGISTERS (Note 25)

Register Address	R/W	Description	Power-On Default
0x64	R/W	PWM1 Min Duty Cycle	0x80 (50% Duty Cycle)
0x65	R/W	PWM2 Min Duty Cycle	0x80 (50% Duty Cycle)
0x66	R/W	PWM3 Min Duty Cycle	0x80 (50% Duty Cycle)

25. These registers become read–only when the ADT7463 is in automatic fan control mode.

Table 67. PWM MIN DUTY CYCLE REGISTER BITS

Bit	Name	R/W	Description
<7:0>	PWM Duty Cycle	R/W	These bits define the PWM _{MIN} duty cycle for PWMx. 0x00 = 0% Duty Cycle (Fan Off) 0x40 = 25% Duty Cycle 0x80 = 50% Duty Cycle 0xFF = 100% Duty Cycle (Fan Full Speed)

Table 68. T_{MIN} REGISTERS (Note 26)

Register Address	R/W	Description (Note 27)	Power-On Default
0x67	R/W	Remote 1 Temperature T _{MIN}	0x5A (90 C)
0x68	R/W	Local Temperature T _{MIN}	0x5A (90 C)
0x69	R/W	Remote 2 Temperature T _{MIN}	0x5A (90 C)

Table 75. REGISTER 0X73 - CONFIGURATION REGISTER 2 (POWER-ON DEFAULT = 0X00) (Note 36)

Bit	Name	R/W	Description
0	AIN1	R/W	AIN1 = 0, Speed of 3–wire fans measured using the TACH output from the fan. AIN1 = 1, Pin 11 is reconfigured to measure the speed of 2–wire fans using an external sensing resistor and coupling capacitor. AIN voltage threshold is set via Configuration Register 4 (Reg. 0x7D).
1	AIN2	R/W	AIN2 = 0, Speed of 3-wire fans measured using the TACH output from the fan. AIN2 = 1, Pin 12 is reconfigured to measure the speed of 2-wire fans using an external sensing resistor and coupling capacitor. AIN voltage threshold is set via Configuration Register 4 (Reg. 0x7D).
2	AIN3	R/W	AIN3 = 0, Speed of 3–wire fans measured using the TACH output from the fan. AIN3 = 1, Pin 9 is reconfigured to measure the speed of 2–wire fans using an external sensing resistor and coupling capacitor. AIN voltage threshold is set via Configuration Register 4 (Reg. 0x7D).
3	AIN4	R/W	AIN4 = 0, Speed of 3-wire fans measured using the TACH output from the fan. AIN4 = 1, Pin 14 is reconfigured to measure the speed of 2-wire fans using an external sensing resistor and coupling capacitor. AIN voltage threshold is set via Configuration Register 4 (Reg. $0x7D$).
4	AVG	R/W	AVG = 1, Averaging on the temperature and voltage measurements is turned off. This allows measurements on each channel to be made much faster.
5	ATTN	R/W	ATTN = 1, the ADT7463 removes the attenuators from the 2.5 V, V _{CCP} , 5 V, and 12 V inputs. The inputs can be used for other functions such as connecting up external sensors.
6	CONV	R/W	CONV = 1, the ADT7463 is put into a single-channel ADC conversion mode. In this mode, the ADT7463 can be made to read continuously from one input only, for example, Remote 1 temperature. It is also possible to start ADC conversions using an external clock on Pin 11 by setting Bit 2 of Test Register 2 (Reg. 0x7F). This mode could be useful if, for example, users wanted to characterize/profile CPU temperature quickly. The appropriate ADC channel is selected by writing to Bits <7:5> of TACH1 min high byte register (Reg. 0x55).Bits <7:5> Reg. 0x55Channel Selected0002.5V001 V_{CCP} 010 V_{CC} (3.3V)011 $5V$ 100 $12V$ 101Remote 1 Temp110Local Temp
			111 Remote 2 Temp
7	SHDN	R/W	SHDN = 1, ADT7463 goes into shutdown mode. All PWM outputs assert low (or high depending, on state of INV bit) to switch off all fans. The PWM current duty cycle registers read 0x00 to indicate that the fans are not being driven.

36. This register becomes read-only when the Configuration Register 1 Lock bit is set to 1. Further attempts to write to this register have no effect.

Table 76. REGISTER 0X74 – INTERRUPT MASK REGISTER 1 (POWER–ON DEFAULT <7:0> = 0X00)

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Bit	Name	R/W	Description
0	2.5V	R/W	A 1 masks SMBALERT for out-of-limit conditions on the 2.5 V channel.
1	V _{CCP}	R/W	A 1 masks SMBALERT for out-of-limit conditions on the V _{CCP} channel.
2	V _{CC}	R/W	A 1 masks SMBALERT for out-of-limit conditions on the V _{CC} channel.
3	5V	R/W	A 1 masks SMBALERT for out-of-limit conditions on the 5 V channel.

TADIE 11. REGISTER VATS - INTERROFT WASK REGISTER 2 (FOWER-ON DEFAULT = VAU)	Table 77. REGISTER 0X75	5 – INTERRUPT MASK REGISTER 2	(POWER-ON DEFAULT = 0X00)
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Bit	Name	R/W	Description
0			

Table 81. REGISTER 0X79 - THERM STATUS REGISTER (POWER-

Table 84. REGISTER 0X7D - CONFIGURATION REGISTER 4 (POWER-ON DEFAULT = 0X00) (Note 40)

Bit	Name	R/W	Description	
<0>	AL2.5V	R/W	AL2.5V = 1, Pin 14 (2.5 V/SMBALERT) is configured as an SMBALERT interrupt output to indicate out–of–limit error conditions. AL2.5V = 0, Pin 14 (2.5 V/SMBALERT) is configured as a 2.5 V measurement input.	
<1>	TH5V	R/W	TH5V = 1, Pin 20 (5V/THERM) is configured as THERM pin. For THERM Monitoring, Bit 1 (THERM Timer) of Configuration Register 3 must also be set. TH5V = 0, Pin 20 (5V/THERM) is configured as 5 V measurement input.	
<3:2>	AINL	R/W	These two bits define the input threshold for 2-wire fan speed measurements: 00 = 20 mV 01 = 40 mV 10 = 80 mV 11 = 130 mV	
<7:4>	RES		Unused.	

40. This register becomes read-only when the Configuration Register 1 Lock bit is set to 1. Further attempts to write to this register have no effect.

Table 85. REGISTER 0X7E - MANUFACTURER'S TEST REGISTER 1 (POWER-ON DEFAULT = 0X00)

Bit	Name	R/W	Description	
<7:0>	RES	Read-only	Manufacturer's Test Register. These bits are reserved for manufacturer's test purposes and should NOT be written to under normal operation.	

Table 86. REGISTER 0X7F – MANUFACTURER'S TEST REGISTER 2 (POWER–ON DEFAULT = 0X00)

Bit	Name	R/W	Description	
<7:0>	RES	Read-only	Manufacturer's Test Register. These bits are reserved for manufacturer's test purposes and should NOT be written to under normal operation.	

Table 87. ORDERING INFORMATION

Device Number Temperature Range		Package Type	Package Option	Shipping [†]
ADT7463ARQZ-REEL	–40 C to +120 C	24-lead QSOP	RQ-24	2,500 / Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*The "Z" suffix indicates Pb-Free part.

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QSOP24 NB CASE 492B-01 ISSUE A

DATE 06 MAY 2008



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