D2+

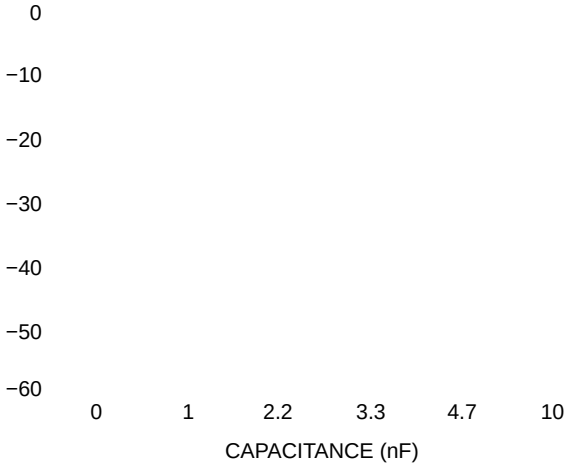
1	SCL	Digital Input (Open Drain). SMBus serial clock input. Requires SMBus pull-up.
2	GND	Ground Pin for the ADT7467.
3	V_{CC}	Power Supply. Can be powered by 3.3 V standby if monitoring in low power states is required. V_{CC} is also monitored through this pin. The ADT7467 can also be powered from a 5 V supply. Setting Bit 7 of Configuration Register 1 (0x40) rescales the V_{CC} input attenuators to correctly measure a 5 V supply.
4	TACH3	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 3. Can be reconfigured as an analog input (AIN3) to measure the speed of 2-wire fans (low frequency mode only).
5	PWM2 $\overline{\text{SMBALERT}}$	Digital Output (Open Drain). Requires 10 kΩ typical pull-up. Pulse width modulated output to control the speed of Fan 2. Can be configured as a high or low frequency drive. Digital Output (Open Drain). This pin can be reconfigured as an $\overline{\text{SMBALERT}}$ interrupt output to signal out-of-limit conditions.
6	TACH1	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 1. Can be reconfigured as an analog input (AIN1) to measure the speed of 2-wire fans (low frequency mode only).
7	TACH2	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 2. Can be reconfigured as an analog input (AIN2) to measure the speed of 2-wire fans (low frequency mode only).
8	PWM3	Digital I/O (Open Drain). Pulse width modulated output to control the speed of Fan 3 and Fan 4. Requires 10 kΩ typical pull-up. Can be configured as a high or low frequency drive.
9	TACH4 GPIO $\overline{\text{THERM}}$ $\overline{\text{SMBALERT}}$	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 4. Can be reconfigured as an analog input (AIN4) to measure the speed of 2-wire fans (low frequency mode only). General-Purpose Open-Drain Digital I/O. Alternatively, the pin can be reconfigured as a bidirectional $\overline{\text{THERM}}$ pin, which can be used to time and monitor assertions on the $\overline{\text{THERM}}$ input. For example, the pin can be connected to the $\overline{\text{PROCHOT}}$ output of an Intel® Pentium® 4 processor or to the output of a trip point temperature sensor. This pin can be used as an output to signal overtemperature conditions. Digital Output (Open Drain). This pin can be reconfigured as an $\overline{\text{SMBALERT}}$ interrupt output to signal out-of-limit conditions.
10	D2−	Cathode Connection to Second Thermal Diode.
11	D2+	Anode Connection to Second Thermal Diode.
12	D1−	Cathode Connection to First Thermal Diode.
13	D1+	Anode Connection to First Thermal Diode.
14	V_{CCP}	Analog Input. Monitors processor core voltage (0 V to 3 V).
15	PWM1 XTO	Digital Output (Open Drain). Pulse width modulated output to control the speed of Fan 1. Requires 10 kΩ typical pull-up. Also functions as the output from the XNOR tree in XNOR test mode.
16	SDA	Digital I/O (Open Drain). SMBus bidirectional serial data. Requires 10 kΩ typical pull-up.

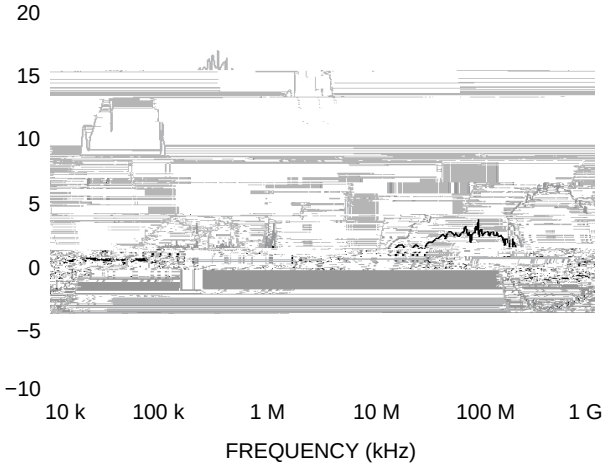
(T_A = T_{MIN} to T_{MAX}, V_{CC} = V_{MIN} to V_{MAX}, unless otherwise noted.) (Note 1)

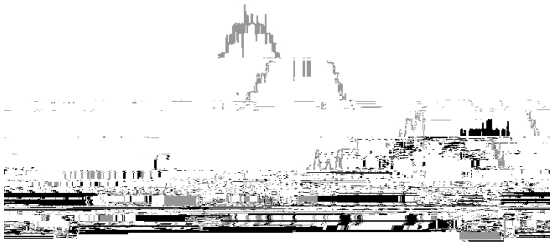
Supply Voltage		3.0	3.3	5.5	V
Supply Current, I_{CC}	Interface Inactive, ADC Active Standby Mode	– –	– –	3 20	mA μA
Local Sensor Accuracy	0°C ≤ T_A ≤ 70°C −40°C ≤ T_A ≤ +100°C −40°C ≤ T_A ≤ +120°C	– −3.5 −4	– – –	±1.5 +2 +2	°C
Resolution		–	0.25	–	°C
Remote Diode Sensor Accuracy	0°C ≤ T_A ≤ 70°C; 0°C ≤ T_D ≤ 120°C 0°C ≤ T_A ≤ 105°C; 0°C ≤ T_D ≤ 120°C −40°C ≤ T_A ≤ +120°C; 0°C ≤ T_D ≤ +120°C	– −3.5 −4.5	±0.5 – –	±1.5 +2 +2	°C
Resolution		–	0.25	–	°C

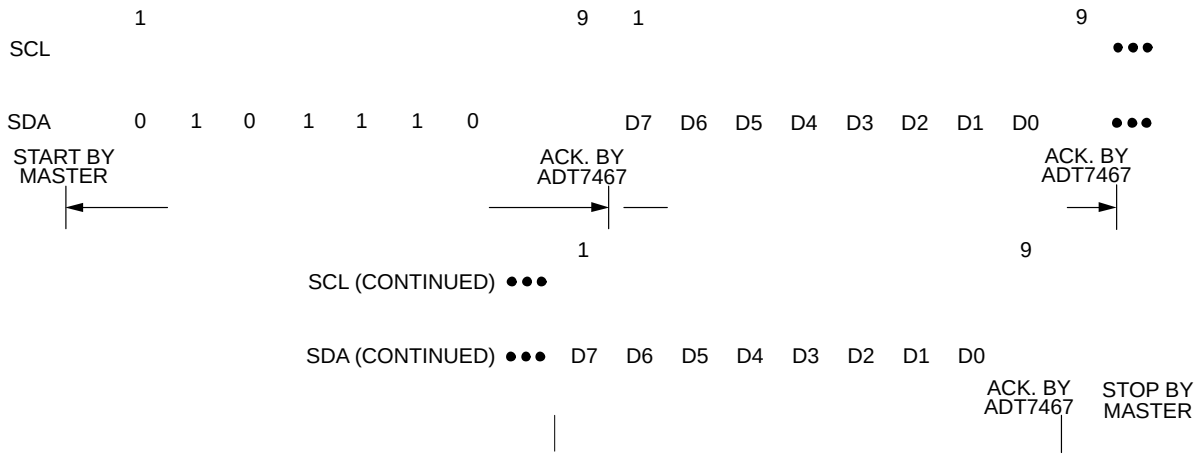
(T_A = T_{MIN} to T_{MAX}, V_{CC} = V_{MIN} to V_{MAX}, unless otherwise noted.) (Note 1)

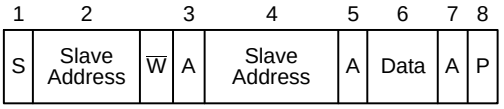
h Voltage, V_{IH}		2.0	−	−	V
Voltage, V_{IL}		−	−	0.4	V
s		−	500	−	mV
h Voltage, V_{IH}	Maximum Input Voltage	2.0 −	− −	− 5.5	V
Voltage, V_{IL}	Minimum Input Voltage	− −0.3	− −	0.8 −	

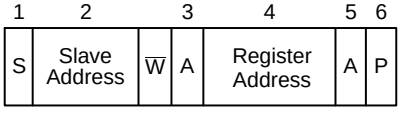

0
−10
−20
−30
−40
−50
−60
0
1
2.2
3.3
4.7
10
CAPACITANCE (nF)

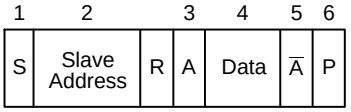

20
15
10
5
0
−5
−10
10 k
100 k
1 M
10 M
100 M
1 G
FREQUENCY (kHz)




1
9
1
9
SCL
SDA
0 1 0 1 1 1 0
D7 D6 D5 D4 D3 D2 D1 D0
START BY MASTER
ACK. BY ADT7467
ACK. BY ADT7467
1
9
SCL (CONTINUED)
SDA (CONTINUED)
D7 D6 D5 D4 D3 D2 D1 D0
ACK. BY ADT7467
STOP BY MASTER


1
2
3
4
5
6
7
8
S
Slave Address
W
A
Slave Address
A
Data
A
P


1
2
3
4
5
6
S
Slave Address
W
A
Register Address
A
P


1
2
3
4
5
6
S
Slave Address
R
A
Data
A
P

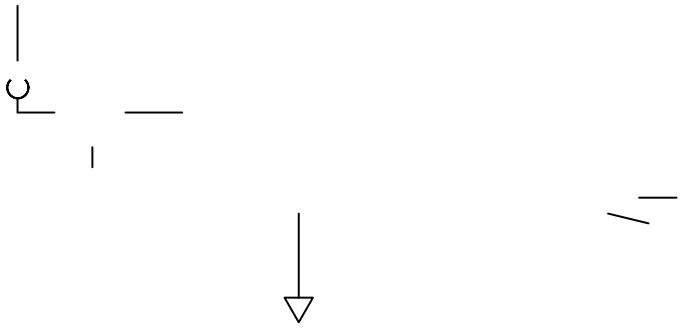
001	V_{CCP}
010	V_{CC}
101	Remote 1 Temperature
110	Local Temperature
111	Remote 2 Temperature

<0.0065	<0.0042	<0.00293	0	00000000 00
0.0065 to 0.0130	0.0042 to 0.0085	0.0293 to 0.0058	1	00000000 01
0.0130 to 0.0195	0.0085 to 0.0128	0.0058 to 0.0087	2	00000000 10
0.0195 to 0.0260	0.0128 to 0.0171	0.0087 to 0.0117	3	00000000 11
0.0260 to 0.0325	0.0171 to 0.0214	0.0117 to 0.0146	4	00000001 00
0.0325 to 0.0390	0.0214 to 0.0257	0.0146 to 0.0175	5	00000001 01
0.0390 to 0.0455	0.0257 to 0.0300	0.0175 to 0.0205	6	00000001 10
0.0455 to 0.0521	0.0300 to 0.0343	0.0205 to 0.0234	7	00000001 11
0.0521 to 0.0586	0.0343 to 0.0386	0.0234 to 0.0263	8	00000010 00
			…	
1.6675 to 1.6740	1.100 to 1.1042	0.7500 to 0.7529	256 (1/4 scale)	01000000 00
			…	
			512 (1/2 scale)	

[redacted]

356 (1/4 scale)

$$\Delta V_{BE} = kT/q \times \ln(N) \qquad \text{(eq. 1)}$$

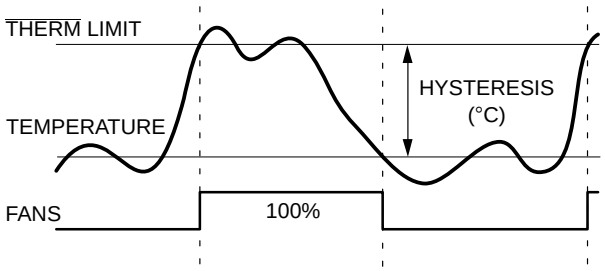


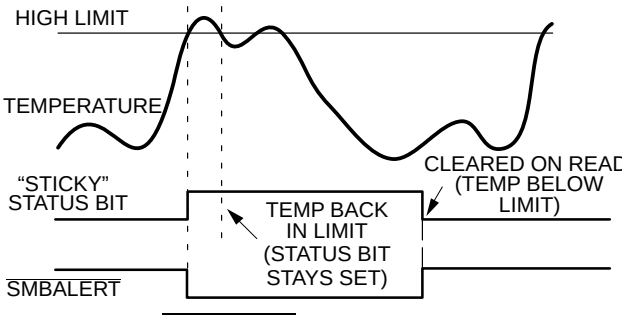
- μ
- μ
- Ω
-

0x25	Remote 1 Temperature	0x01
0x26	Local Temperature	0x01
0x27	Remote 2 Temperature	0x01
0x77	Extended Resolution 2	0x00

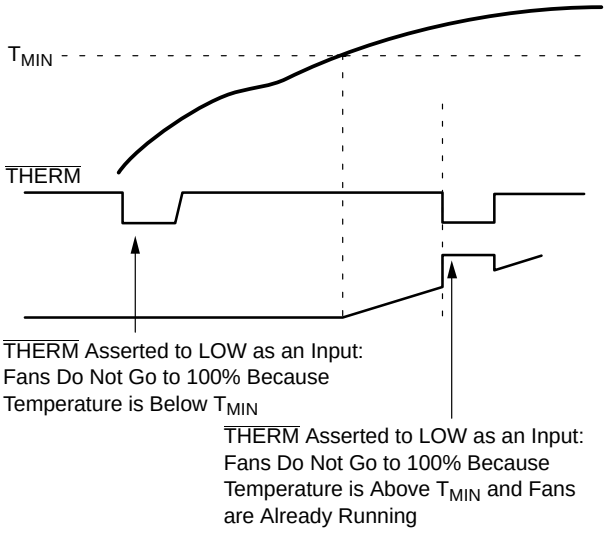
<7:6>	TDM2	Remote 2 Temperature LSBs
<5:4>	LTMP	Local Temperature LSBs
<3:2>	TDM1	Remote 1 Temperature LSBs

0x4E	Remote 1 Temperature Low Limit	0x01
0x4F	Remote 1 Temperature High Limit	0x7F
0x50	Local Temperature Low Limit	0x01
0x51	Local Temperature High Limit	0x7F
0x52	Remote 2 Temperature Low Limit	0x01
0x53	Remote 2 Temperature High Limit	0x7F

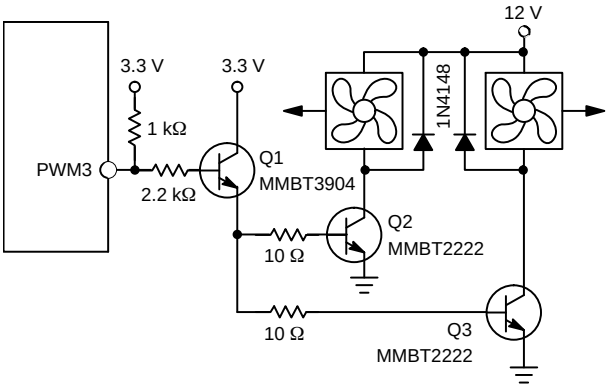

THERM LIMIT
TEMPERATURE
HYSTERESIS
(°C)
FANS
100%

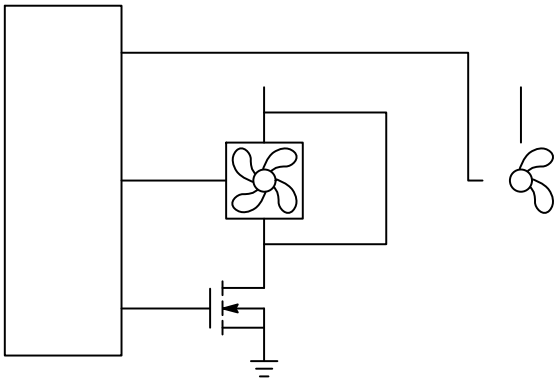

HIGH LIMIT
TEMPERATURE
CLEARED ON READ
(TEMP BELOW
LIMIT)
“STICKY”
STATUS BIT
TEMP BACK
IN LIMIT
(STATUS BIT
STAYS SET)
SMBALERT

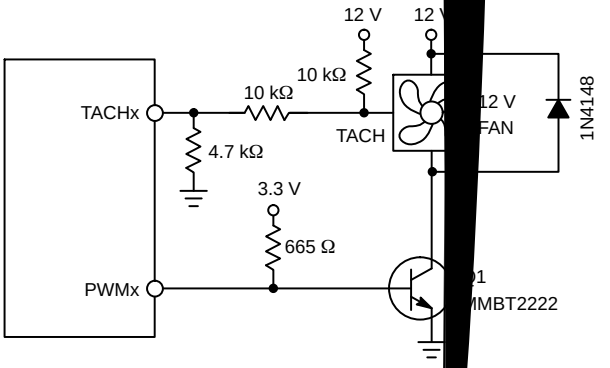
0	0	TACH4
0	1	$\overline{\text{THERM}}$
1	0	$\overline{\text{SMBALERT}}$
1	1	GPIO

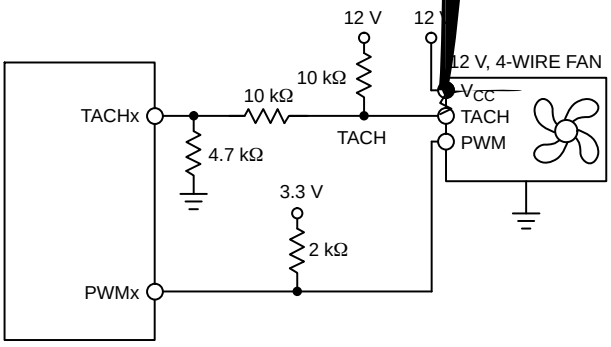


Ω

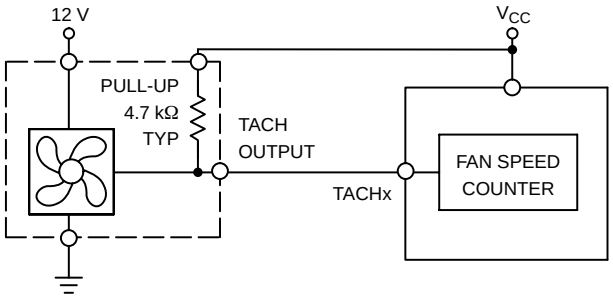

12 V
3.3 V
3.3 V
1N4148
1 kΩ
PWM3
Q1
MMBT3904
2.2 kΩ
Q2
MMBT2222
10 Ω
10 Ω
Q3
MMBT2222

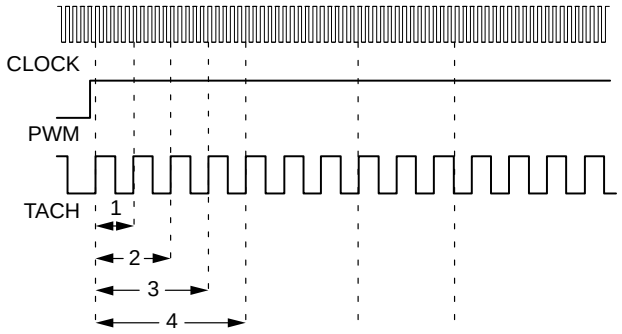



12 V
12 V
10 kΩ
10 kΩ
TACHx
12 V
FAN
TACH
1N4148
4.7 kΩ
3.3 V
665 Ω
PWMx
Q1
MMBT2222


12 V
12 V
12 V, 4-WIRE FAN
10 kΩ
10 kΩ
TACHx
VCC
TACH
PWM
TACH
4.7 kΩ
3.3 V
2 kΩ
PWMx

<4>	SYNC	1 Synchronizes TACH2, TACH3, and TACH4 to PWM3.


12 V
V_{CC}
PULL-UP
4.7 kΩ
TYP
TACH
OUTPUT
TACHx
FAN SPEED
COUNTER



0x54	TACH1 Minimum Low Byte	0xFF
0x55	TACH1 Minimum High Byte	0xFF
0x56	TACH2 Minimum Low Byte	0xFF
0x57	TACH2 Minimum High Byte	0xFF
0x58	TACH3 Minimum Low Byte	0xFF
0x59	TACH3 Minimum High Byte	0xFF
0x5A	TACH4 Minimum Low Byte	0xFF
0x5B	TACH4 Minimum High Byte	0xFF

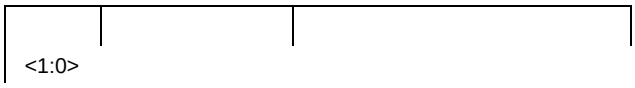
0x28	TACH1 Low Byte	0x00
0x29	TACH1 High Byte	0x00
0x2A	TACH2 Low Byte	0x00
0x2B	TACH2 High Byte	0x00
0x2C	TACH3 Low Byte	0x00
0x2D	TACH3 High Byte	0x00
0x2E	TACH4 Low Byte	0x00
0x2F	TACH4 High Byte	0x00

×

µ

×

×


<1:0>

<4>	INV	0 = logic high for 100% PWM duty cycle 1 = logic low for 100% PWM duty cycle

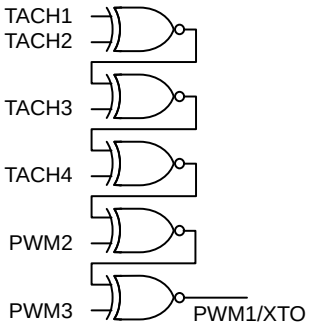
<7:5>	BHVR	111 = Manual Mode

<2:0>	FREQ	000 = 11.0 Hz 001 = 14.7 Hz 010 = 22.1 Hz 011 = 29.4 Hz 100 = 35.3 Hz (Default) 101 = 44.1 Hz 110 = 58.8 Hz 111 = 88.2 Hz

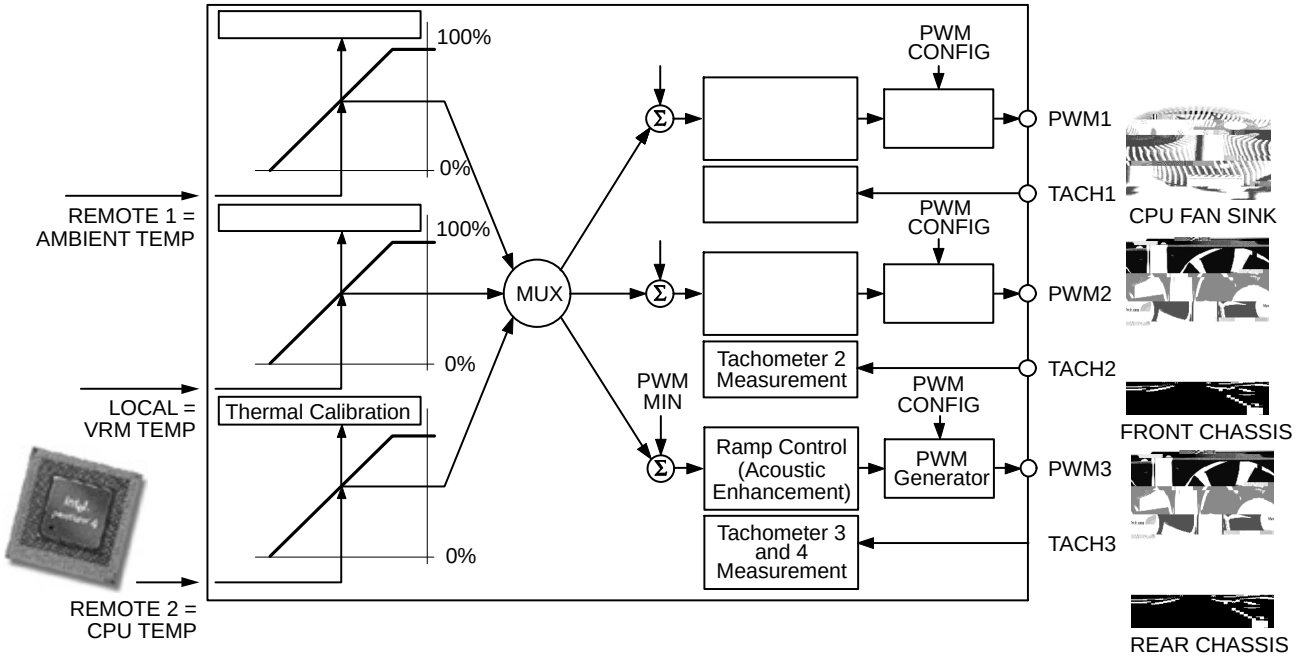
0x30	PWM1 Current Duty Cycle	0x00 (0%)
0x31	PWM2 Current Duty Cycle	0x00 (0%)
0x32	PWM3 Current Duty Cycle	0x00 (0%)

ADT7467 is Powered Up

Start Fail−



® ®


100%
0%
100%
0%
Thermal Calibration
0%
REMOTE 1 =
AMBIENT TEMP
LOCAL =
VRM TEMP
REMOTE 2 =
CPU TEMP
MUX
PWM
MIN
PWM
CONFIG
PWM
CONFIG
PWM
CONFIG
Tachometer 2
Measurement
Ramp Control
(Acoustic
Enhancement)
PWM
Generator
Tachometer 3
and 4
Measurement
PWM1
TACH1
PWM2
TACH2
PWM3
TACH3
CPU FAN SINK
FRONT CHASSIS
REAR CHASSIS

-
-
-
-
-
-
- ® ®
-

REMOTE 2 =
CPU TEMP

LOCAL =
VRM TEMP

REMOTE 1 =
AMBIENT TEMP

PWM1

TACH1

CPU FAN SINK

PWM2

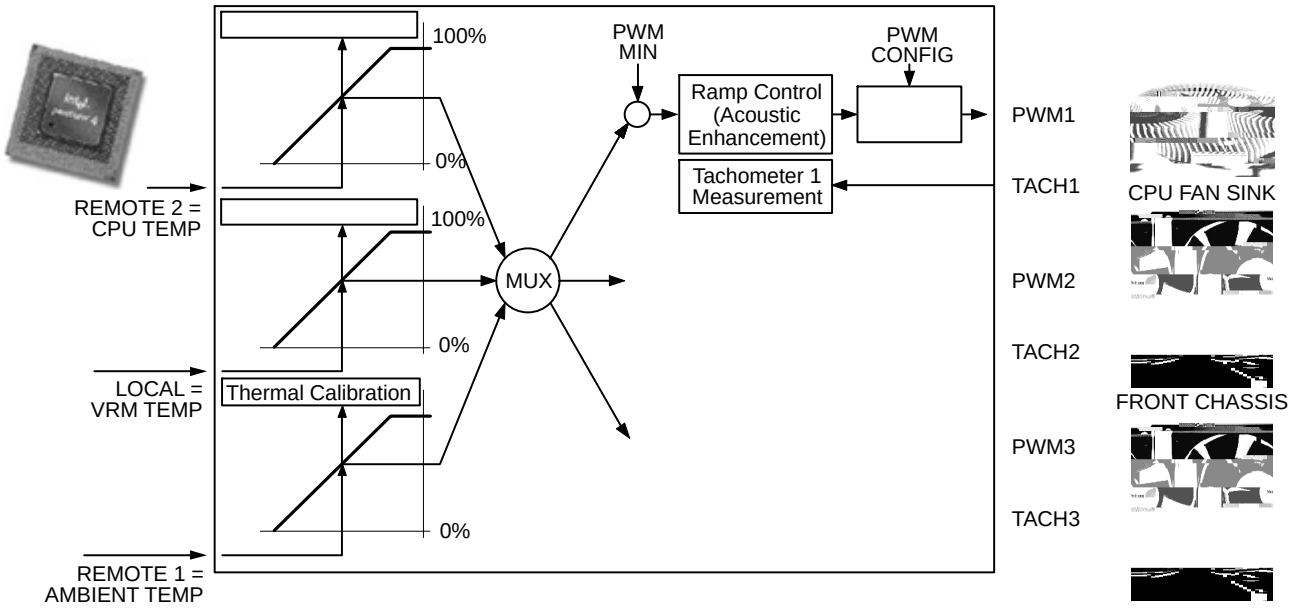
TACH2

FRONT CHASSIS

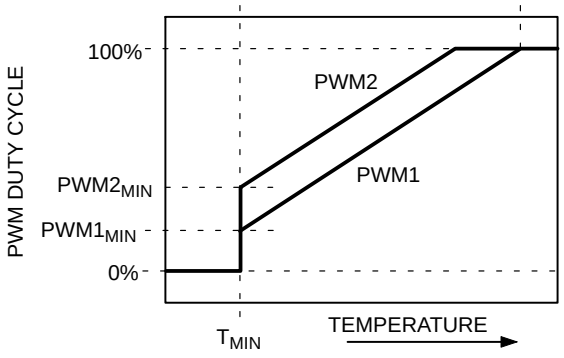
PWM3

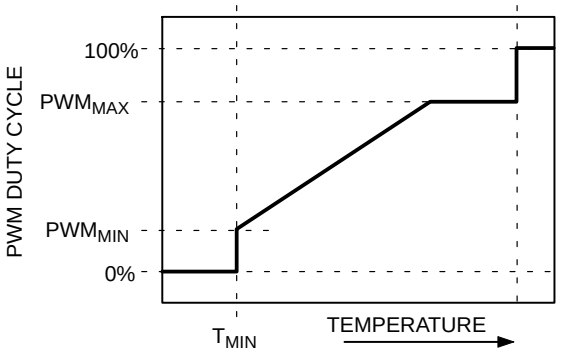
TACH3

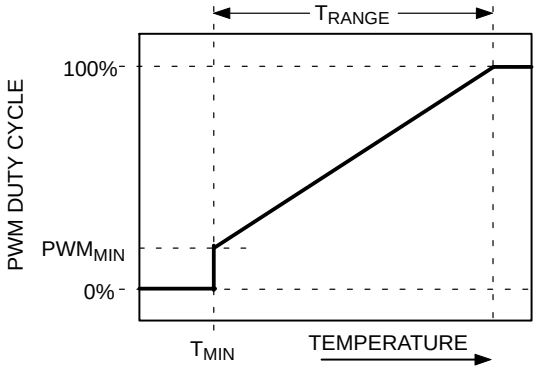
REAR CHASSIS

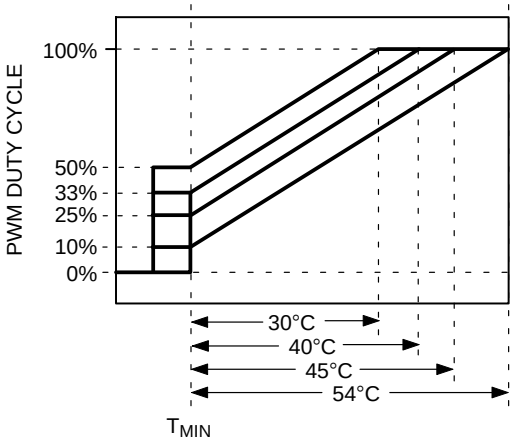

100%
0%
100%
0%
0%
PWM
MIN
PWM
CONFIG
Ramp Control
(Acoustic
Enhancement)
Tachometer 1
Measurement
MUX
Thermal Calibration
REMOTE 2 =
CPU TEMP
LOCAL =
VRM TEMP
REMOTE 1 =
AMBIENT TEMP
PWM1
TACH1
PWM2
TACH2
PWM3
TACH3
CPU FAN SINK
FRONT CHASSIS

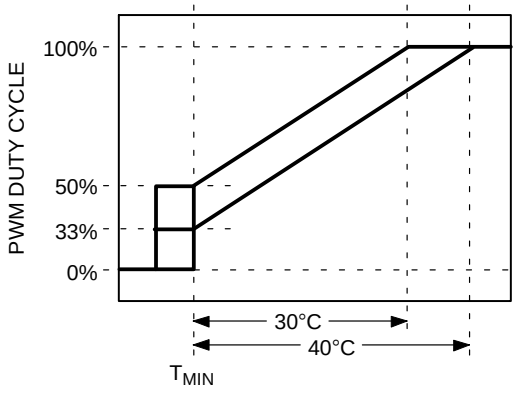
$$\% \text{ fan speed} = \sqrt{\text{PWM duty cycle} \times 10}$$

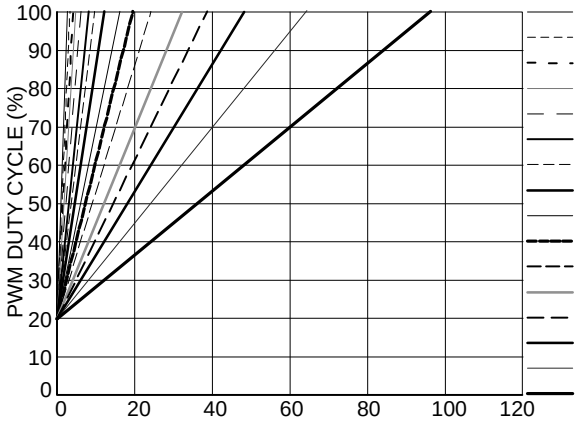


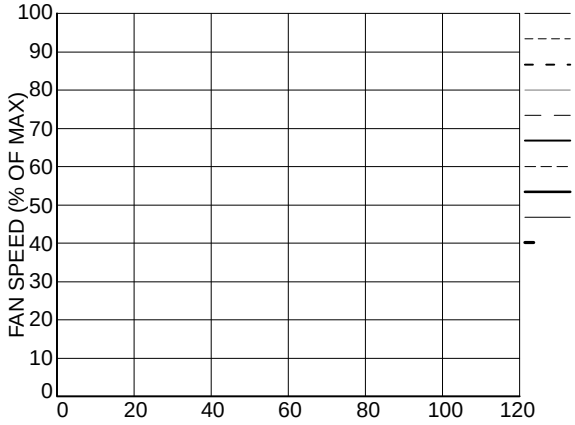


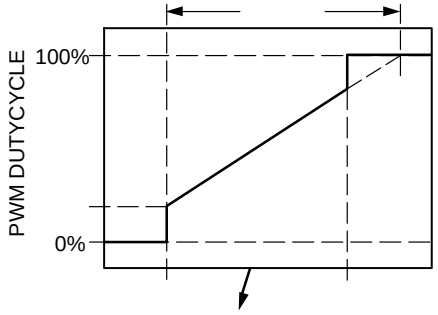

T_RANGE
100%
PWM DUTY CYCLE
PWM_MIN
0%
T_MIN
TEMPERATURE


100%
50%
33%
25%
10%
0%
PWM DUTY CYCLE
30°C
40°C
45°C
54°C
T_MIN


100%
50%
33%
0%
PWM DUTY CYCLE
30°C
40°C
T_MIN


PWM DUTY CYCLE (%)
100
90
80
70
60
50
40
30
20
10
0
0
20
40
60
80
100
120


FAN SPEED (% OF MAX)
100
90
80
70
60
50
40
30
20
10
0
0
20
40
60
80
100
120



REMOTE 2 =
CPU TEMP

LOCAL =
VRM TEMP

REMOTE 1 =
AMBIENT TEMP

PWM1

TE0B8

CPU FAN SINK

PWM2

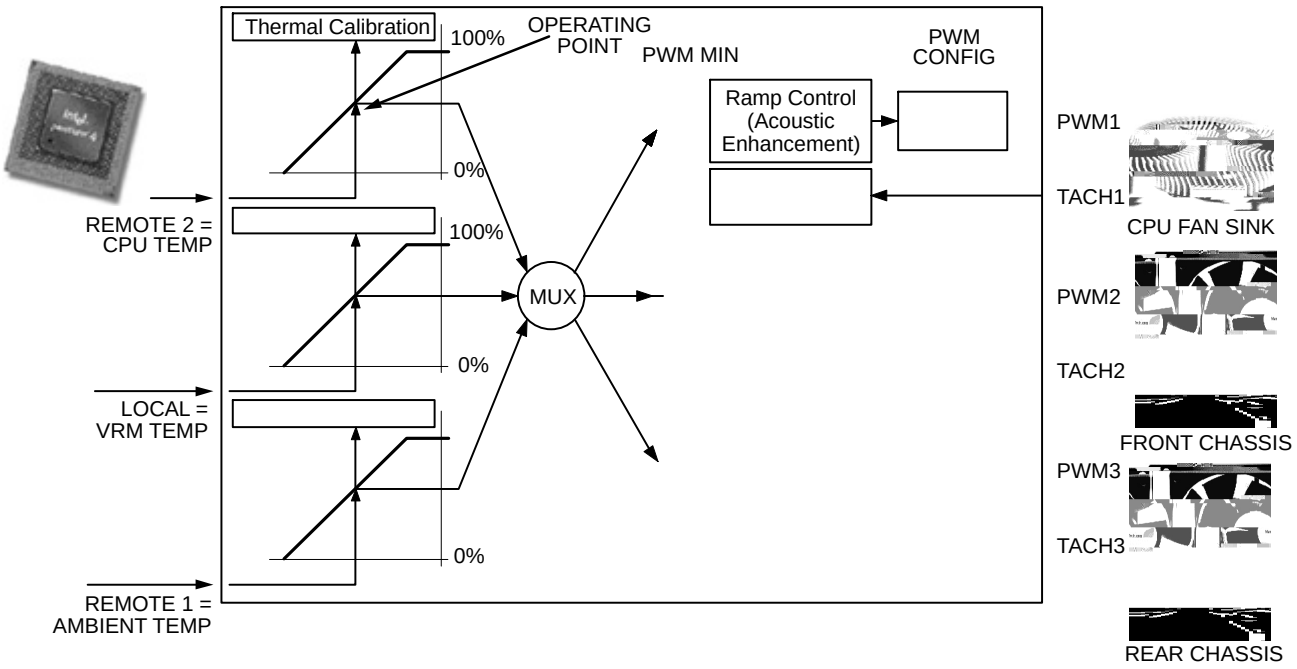
TE0B2

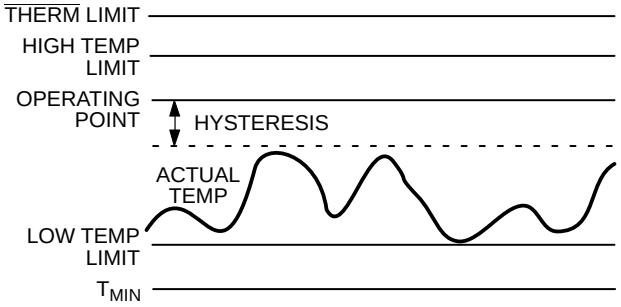
FRONT CHASSIS

PWM3

TE0B3

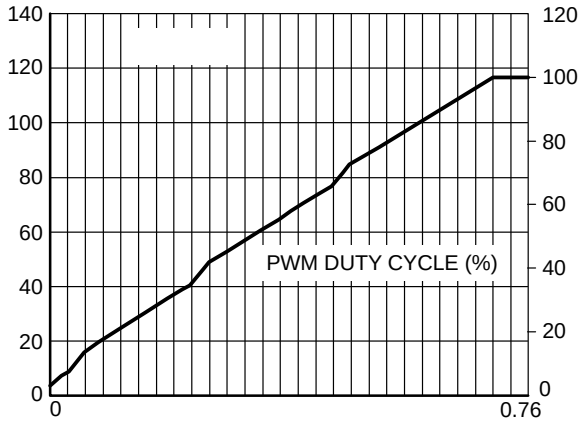
REAR CHASSIS

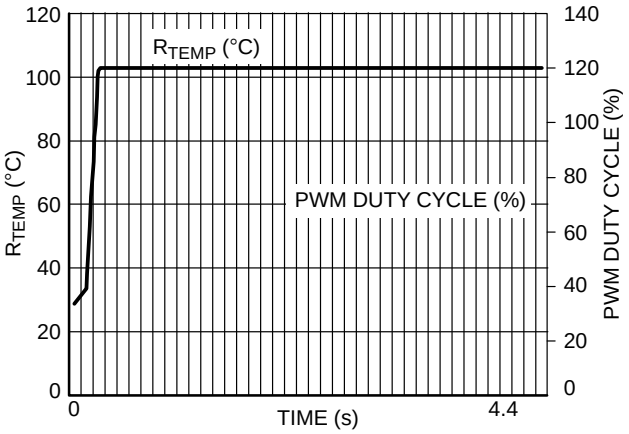

Thermal Calibration
100%
OPERATING POINT
PWM MIN
PWM CONFIG
Ramp Control (Acoustic Enhancement)
0%
100%
0%
0%
MUX
REMOTE 2 = CPU TEMP
LOCAL = VRM TEMP
REMOTE 1 = AMBIENT TEMP
PWM1
TACH1
CPU FAN SINK
PWM2
TACH2
FRONT CHASSIS
PWM3
TACH3
REAR CHASSIS

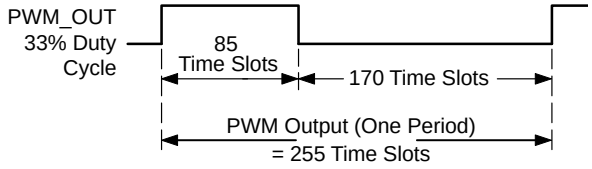

THERM LIMIT
HIGH TEMP LIMIT
OPERATING POINT
HYSTERESIS
ACTUAL TEMP
LOW TEMP LIMIT
T_{MIN}

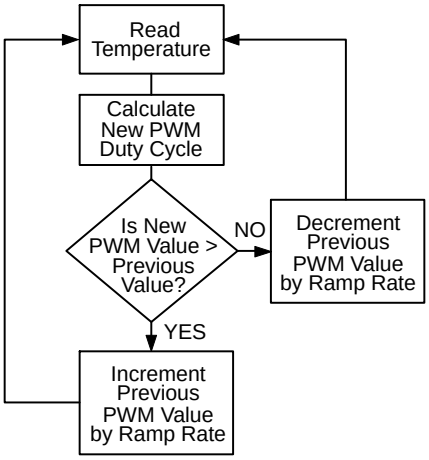
-
-
-

<5>	R1T	1 enables dynamic T_{MIN} control on the Remote 1 temperature channel. The chosen T_{MIN} value is dynamically adjusted based on the current temperature, operating point, and high and low limits for this zone. 0 disables dynamic T_{MIN} control. The T_{MIN} value chosen is not adjusted, and the channel behaves as described in the Automatic Fan Control Overview section.
<6>	LT	1 enables dynamic T_{MIN} control on the local temperature channel. The chosen T_{MIN} value is dynamically adjusted based on the current temperature, operating point, and high and low limits for this zone. 0 disables dynamic T_{MIN} control. The T_{MIN} value chosen is not adjusted, and the channel behaves as described in the Enhancing System Acoustics section.
<7>	R2T	1 enables the dynamic T_{MIN} control on the Remote 2 temperature channel. The chosen T_{MIN} value is dynamically adjusted based on the current temperature, operating point, and high and low limits for this zone.




120
100
80
60
40
20
0
140
120
100
80
60
40
20
0
R_{TEMP} (°C)
PWM DUTY CYCLE (%)
R_{TEMP} (°C)
PWM DUTY CYCLE (%)
0
4.4
TIME (s)


PWM_OUT
33% Duty
Cycle
85
Time Slots
170 Time Slots
PWM Output (One Period)
= 255 Time Slots


Read
Temperature
Calculate
New PWM
Duty Cycle
Is New
PWM Value >
Previous
Value?
NO
Decrement
Previous
PWM Value
by Ramp Rate
YES
Increment
Previous
PWM Value
by Ramp Rate

(continued)

(Note 1)

0x21	Read Only	Reflects the Voltage Measurement (Note 2) at the V_{CCP} Input on Pin 14 (8 MSBs of Reading)
0x22	Read Only	Reflects the Voltage Measurement (Note 3) at the V_{CC} Input on Pin 3 (8 MSBs of Reading)

1. If the extended resolution bits of these readings are also being read, the extended resolution registers (0x76, 0x77) must be read first. Once the extended resolution registers have been read, the associated MSB reading registers are frozen until read. Both the extended resolution registers and the MSB registers are frozen.
2. If V_{CCP}LO (Bit 1 of the Dynamic T_{MIN} Control Register 1, 0x36) is set, V_{CCP} can control the sleep state of the ADT7467.
3. V_{CC} (Pin 3) is the supply voltage for the ADT7467.

(Notes 1, 2)

0x25	Read Only	Remote 1 Temperature Reading (Notes 3, 4) (8 MSBs of Reading)
0x26	Read Only	Local Temperature Reading (8 MSBs of Reading)
0x27	Read Only	Remote 2 Temperature Reading (8 MSBs of Reading)

1. These temperature readings can be in twos complement or Offset 64 format; this interpretation is determined by Bit 0 of Configuration Register 5 (0x7C).
2. If the extended resolution bits of these readings are also being read, the extended resolution registers (0x76, 0x77) must be read first. Once the extended resolution registers have been read, all associated MSB reading registers are frozen until read. Both the extended resolution registers and the MSB registers are frozen.
3. In twos complement mode, a temperature reading of −128°C (0x80) indicates a diode fault (open or short) on that channel.
4. In Offset 64 mode, a temperature reading of −64°C (0x00) indicates a diode fault (open or short) on that channel.

(Note 1)

0x28	Read Only	TACH1 Low Byte
0x29	Read Only	TACH1 High Byte
0x2A	Read Only	TACH2 Low Byte
0x2B	Read Only	TACH2 High Byte
0x2C	Read Only	TACH3 Low Byte
0x2D	Read Only	TACH3 High Byte
0x2E	Read Only	TACH4 Low Byte
0x2F	Read Only	TACH4 High Byte

1. These registers count the number of 11.11 μs periods (based on an internal 90 kHz clock) that occur between a number of consecutive fan TACH pulses (default = 2). The number of TACH pulses used to count can be changed using the TACH pulses per revolution register (0x7B). This allows the fan speed to be accurately measured. Because a valid fan tachometer reading requires that two bytes are read, the low byte must be read first. Both the low and high bytes are then frozen until read. At power-on, these registers contain 0x0000 until the first valid fan TACH measurement is read into these registers. This prevents false interrupts from occurring while the fans are spinning up.
   A count of 0xFFFF indicates that a fan is one of the following:
   - Stalled or blocked (object jamming the fan).
   - Failed (internal circuitry destroyed).
   - Not populated. (The ADT7467 expects to see a fan connected to each TACH. If a fan is not connected to a TACH, the minimum high and low bytes of that TACH should be set to 0xFFFF.)
   - Alternate function (for example, TACH4 reconfigured as $\overline{\text{THERM}}$ pin).
   - 2-wire instead of 3-wire fan.

(Note 1)

0x30	Read/Write	PWM1 Current Duty Cycle (0% to 100% Duty Cycle = 0x00 to 0xFF)
0x31	Read/Write	PWM2 Current Duty Cycle (0% to 100% Duty Cycle = 0x00 to 0xFF)
0x32	Read/Write	PWM3 Current Duty Cycle (0% to 100% Duty Cycle = 0x00 to 0xFF)

1. These registers reflect the PWM duty cycle driving each fan at any given time. When in automatic fan speed control mode, the ADT7467 reports the PWM duty cycles through these registers. The PWM duty cycle values vary according to the temperature in automatic fan speed control mode. During fan startup, these registers report 0x00. In software mode, the PWM duty cycle outputs can be set to any duty cycle value by writing to these registers.

(Notes 1, 2, 3)

0x33	Read/Write	Remote 1 Operating Point Register (Default = 100°C)
0x34	Read/Write	Local Temperature Operating Point Register (Default = 100°C)
0x35	Read/Write	Remote 2 Operating Point Register (Default = 100°C)

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(Note 1)

<2:0>	CYR1	Read/Write	3-bit Remote 1 cycle value. These three bits define the delay time, in terms of the number of monitoring cycles, for making subsequent T_{MIN} adjustments in the control loop for the Remote 1 channel. The system is associated with thermal time constants that must be found to optimize the response of the fans and the control loop. 000 8 cycles (1 sec) 16 cycles (2 sec) 001 16 cycles (2 sec) 32 cycles (4 sec) 010 32 cycles (4 sec) 64 cycles (8 sec)

– (Note 1)

<0>	STRT	Read/Write	Logic 1 enables monitoring and PWM control outputs based on the limit settings programmed. Logic 0 disables monitoring and PWM control based on the default power-up limit settings. Note that the limit values programmed are preserved even if a Logic 0 is written to this bit and the default settings are enabled. This bit becomes a read-only bit and cannot be changed once Bit 1 (LOCK bit) has been written. All limit registers should be programmed by BIOS before setting this bit to 1. (Lockable)
<1>	LOCK	Write Once	Logic 1 locks all limit values to their current settings. Once this bit is set, all lockable registers become read-only registers and cannot be modified until the ADT7467 is powered down and powered up again. This prevents rogue programs such as viruses from modifying critical system limit settings. (Lockable)
<2>	RDY	Read Only	This bit is only set to 1 by the ADT7467 to indicate that the device is fully powered up and ready to begin system monitoring.
<3>	FSPD	Read/Write	When set to 1, this bit runs all fans at full speed. Power-on default = 0. This bit cannot be locked at any time.
<4>	VxI	Read/Write	BIOS should set this bit to a 1 when the ADT7467 is configured to measure current from an ADI ADOPT VRM controller and to measure the CPU's core voltage. This bit allows monitoring software to display the watts used by the CPU. (Lockable)
<5>	FSPDIS	Read/Write	

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<1>	OVT	Read Only	OVT = 1 indicates that one of the $\overline{\text{THERM}}$ overtemperature limits has been exceeded. This bit is cleared upon a read of the status register when the temperature drops below $\overline{\text{THERM}} - T_{HYST}$.
<2>	FAN1	Read Only	FAN1 = 1 indicates that Fan 1 has dropped below minimum speed or has stalled. This bit is not set when the PWM1 output is off.
<3>			

(Note 1)

0x54	Read/Write	TACH1 Minimum Low Byte	0xFF
0x55	Read/Write	TACH1 Minimum High Byte/Single-channel ADC Channel Select	0xFF
0x56	Read/Write	TACH2 Minimum Low Byte	0xFF
0x57	Read/Write	TACH2 Minimum High Byte	0xFF
0x58	Read/Write	TACH3 Minimum Low Byte	0xFF
0x59	Read/Write	TACH3 Minimum High Byte	0xFF
0x5A	Read/Write	TACH4 Minimum Low Byte	0xFF
0x5B	Read/Write	TACH4 Minimum High Byte	0xFF

1. Exceeding any TACH limit register by 1 indicates that the fan is running too slowly or has stalled. The appropriate status bit is set in Interrupt Status Register 2 to indicate the fan failure. Setting the Configuration Register 1 LOCK bit has no effect on these registers.

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<4:0>	Reserved	Read Only	These bits are reserved when Bit 6 of Configuration 2 Register (0x73) is set (single-channel ADC mode). Otherwise, these bits represent Bits <4:0> of the TACH1 minimum high byte.
<7:5>	SCADC	Read/Write	When Bit 6 of Configuration 2 Register (0x73) is set (single-channel ADC mode), these bits are used to select the only channel from which the ADC makes measurements. Otherwise, these bits represent Bits <7:5> of the TACH1 minimum high byte.

	(Note 1)		
0x5C	Read/Write	PWM1 Configuration	0x82
0x5D	Read/Write	PWM2 Configuration	0x82
0x5E	Read/Write	PWM3 Configuration	0x82

1. These registers become read−only registers when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to these registers fail.

		(Note 1)	
<2:0>	SPIN	Read/Write	These bits control the start-up timeout for PWMx. The PWM output stays high until two valid TACH rising edges are seen from the fan. If there is not a valid TACH signal during the fan TACH measurement immediately after the fan start-up timeout period, the TACH measurement

		(Note 1)

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		(Note 1)	
<2:0>	ACOU	Read/Write	These bits select the ramp rate applied to the PWM1 output. Instead of PWM1 jumping instant-aneously to its newly calculated speed, PWM1 ramps gracefully at the rate determined by these bits. This feature enhances the acoustics of the fan being driven by the PWM1 output. 000 = 1 35 sec 001 = 2 17.6 sec 010 = 3 11.8 sec 011 = 5 7 sec 100 = 8 4.4 sec 101 = 12 3 sec 110 = 24 1.6 sec 111 = 48 0.8 sec
<3>	EN1	Read/Write	When this bit is 1, acoustic enhancement is enabled on PWM1 output.

<4>

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		(Note 1)	
<2:0>	ACOU3	Read/Write	These bits select the ramp rate applied to the PWM3 output. Instead of PWM3 jumping instant-

(Note 1)

	(Note 2)		
0x6A	Read/Write	Remote 1 $\overline{\text{THERM}}$ Temperature Limit	0xA4 (100°C)
0x6B	Read/Write	Local $\overline{\text{THERM}}$ Temperature Limit	0xA4 (100°C)
0x6C	Read/Write	Remote 2 $\overline{\text{THERM}}$ Temperature Limit	0xA4 (100°C)

1. If any temperature measured exceeds its $\overline{\text{THERM}}$ limit, all PWM outputs drive their fans at 100% duty cycle. This is a fail-safe mechanism incorporated to cool the system in the event of a critical overtemperature. It also ensures some level of cooling in the event that software or hardware locks up. If set to 0x80, this feature is disabled. The PWM output remains at 100% until the temperature drops below $\overline{\text{THERM}}$ limit – hysteresis. If the $\overline{\text{THERM}}$ pin is programmed as an output, exceeding these limits by 0.25°C can cause the $\overline{\text{THERM}}$ pin to assert low as an output.
2. These registers become read-only registers when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to these registers fail.

(Note 1)

	(Note 2)		
0x6D	Read/Write	Remote 1 and Local Temperature Hysteresis	0x44
0x6E	Read/Write	Remote 2 Temperature Hysteresis	0x40

1. Each 4-bit value controls the amount of temperature hysteresis applied to a particular temperature channel. Once the temperature for that channel falls below its T_{MIN} value, the fan remains running at PWM_{MIN} duty cycle until the temperature = T_{MIN} – hysteresis. Up to 15°C of hysteresis can be assigned to any temperature channel. The hysteresis value chosen also applies to that temperature channel if its $\overline{\text{THERM}}$ limit is exceeded. If the $\overline{\text{THERM}}$ limit is exceeded, the PWM output being controlled goes to 100% and remains at 100% until the temperature drops below $\overline{\text{THERM}}$ – hysteresis. For acoustic reasons, it is recommended that the hysteresis value not be programmed to less than 4°C. Setting the hysteresis value lower than 4°C causes the fan to switch on and off regularly when the temperature is close to T_{MIN}.
2. These registers become read-only registers when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to these registers fail.

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		(Note 1)	
<3:0>	HYSL	Read/Write	Local temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the local temperature AFC and dynamic T_{MIN} control loops.
<7:4>	HYSR1	Read/Write	Remote 1 temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the Remote 1 temperature AFC and dynamic T_{MIN} control loops.

1. This register becomes a read-only register when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

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		(Note 1)	
<7:4>	HYSR2	Read/Write	Local temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the local temperature AFC and dynamic T_{MIN} control loops.

1. This register becomes a read-only register when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

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		(Note 1)	
<0>	XEN	Read/Write	If the XEN bit is set to 1, the device enters the XNOR tree test mode. Clearing the bit removes the device from the XNOR tree test mode.
<7:1>	Reserved	Read Only	Unused. Do not write to these bits.

1. This register becomes a read-only register when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

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<1>	V_{CCP}	Read/Write	V_{CCP} = 1 masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the V_{CCP} channel
<2>	V_{CC}	Read/Write	V_{CC} = 1 masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the V_{CC} channel

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<1:0>	FAN1	Read/Write	Sets the number of pulses to be counted when measuring Fan 1 speed. Can be used to determine fan pulses per revolution for an unknown fan type. 00 = 1 01 = 2 (Default) 10 = 3 11 = 4
<3:2>	FAN2	Read/Write	Sets the number of pulses to be counted when measuring Fan 2 speed. Can be used to determine fan pulses per revolution for an unknown fan type. 00 = 1 01 = 2 (Default) 10 = 3 11 = 4
<5:4>	FAN3	Read/Write	Sets the number of pulses to be counted when measuring Fan 3 speed. Can be used to determine fan pulses per revolution for an unknown fan type. 00 = 1 01 = 2 (Default) 10 = 3 11 = 4
<7:6>	FAN4	Read/Write	Sets the number of pulses to be counted when measuring Fan 4 speed. Can be used to determine fan pulses per revolution for an unknown fan type. 00 = 1 01 = 2 (Default) 10 = 3 11 = 4

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		(Note 1)	
<0>	Twos		

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		(Note 1)	
<1:0>	Pin 9 Func	Read/Write	These bits set the functionality of Pin 9. 00 = TACH4 (default) 01 = bidirectional $\overline{\text{THERM}}$ 10 = $\overline{\text{SMBALERT}}$ 11 = GPIO
<3:2>	AINL	Read/Write	These two bits define the input threshold for 2−wire fan speed measurements (low frequency mode only). 00 = ±20 Mv 01 = ±40 mV 10 = ±80 mV 11 = ±130 mV
<4>	RES		Unused
<5>	BpAtt V_{CCP}		Bypass V_{CCP} attenuator. When set, the measurement scale for this channel changes from 0 V (0x00) to 2.2965 V (0xFF).
<6:7>	RES		Unused

1. This register becomes a read-only register when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

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<7:0>	Reserved	Read Only	Manufacturer’s test register. These bits are reserved for the manufacturer’s testing purposes and should not be written to under normal operation.

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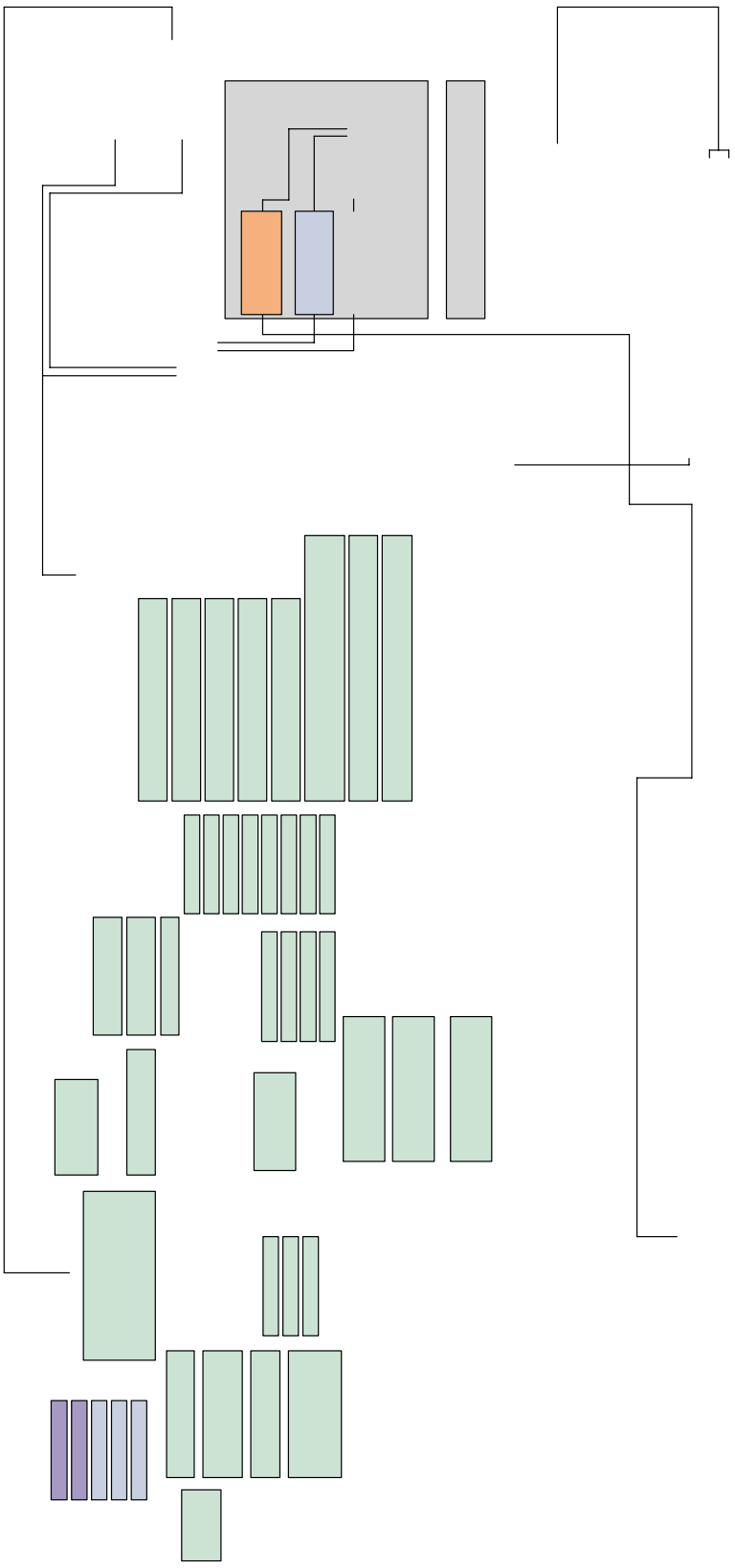
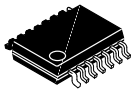
<7:0>	Reserved	Read Only	Manufacturer’s test register. These bits are reserved for the manufacturer’s testing purposes and should not be written to under normal operation.

				†
ADT7467ARQZ−REEL	–40°C to +120°C	16-lead QSOP	RQ−16	2,500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*The “Z” suffix indicates RoHS Compliant part.

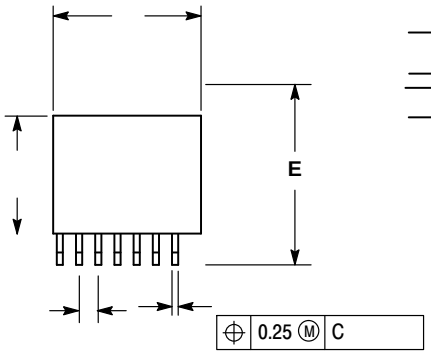


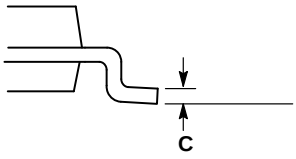


SCALE 2:1

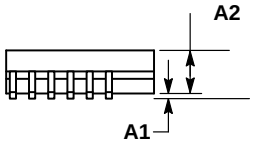
QSOP16
CASE 492−01
ISSUE A

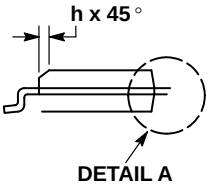
DATE 23 MAR 2011





DETAIL A





DETAIL A

NOTES:

DIM	INCHES MIN	MA
A	0.053	0.069
A1	0.004	0.010
	0.008	0.012
\	0.007	0.010
	0.025 BSC	
	0.009	0.020
L	0.016	0.050
M	0	8