D2+

Table 2. PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	SCL	Digital Input (Open Drain). SMBus serial clock input. Requires SMBus pull-up.
2	GND	Ground Pin for the ADT7467.
3	V _{CC}	Power Supply. Can be powered by 3.3 V standby if monitoring in low power states is required. V _{CC} is also monitored through this pin. The ADT7467 can also be powered from a 5 V supply. Setting Bit 7 of Configuration Register 1 (0x40) rescales the V _{CC} input attenuators to correctly measure a 5 V supply.
4	TACH3	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 3. Can be reconfigured as an analog input (AIN3) to measure the speed of 2-wire fans (low frequency mode only).
5	PWM2	Digital Output (Open Drain). Requires 10 kΩ typical pull-up. Pulse width modulated output to control the speed of Fan 2. Can be configured as a high or low frequency drive.
	SMBALERT	Digital Output (Open Drain). This pin can be reconfigured as an SMBALERT interrupt output to signal out-of-limit conditions.
6	TACH1	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 1. Can be reconfigured as an analog input (AIN1) to measure the speed of 2-wire fans (low frequency mode only).
7	TACH2	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 2. Can be reconfigured as an analog input (AIN2) to measure the speed of 2-wire fans (low frequency mode only).
8	PWM3	Digital I/O (Open Drain). Pulse width modulated output to control the speed of Fan 3 and Fan 4. Requires 10 k Ω typical pull-up. Can be configured as a high or low frequency drive.
9	TACH4	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 4. Can be reconfigured as an analog input (AIN4) to measure the speed of 2-wire fans (low frequency mode only).
	GPIO	General-Purpose Open-Drain Digital I/O.
	THERM	Alternatively, the pin can be reconfigured as a bidirectional THERM pin, which can be used to time and monitor assertions on the THERM input. For example, the pin can be connected to the PROCHOT output of an Intel [®] Pentium [®] 4 processor or to the output of a trip point temperature sensor. This pin can be used as an output to signal overtemperature conditions.
	SMBALERT	Digital Output (Open Drain). This pin can be reconfigured as an SMBALERT interrupt output to signal out-of-limit conditions.
10	D2–	Cathode Connection to Second Thermal Diode.
11	D2+	Anode Connection to Second Thermal Diode.
12	D1–	Cathode Connection to First Thermal Diode.
13	D1+	Anode Connection to First Thermal Diode.
14	V _{CCP}	Analog Input. Monitors processor core voltage (0 V to 3 V).
15	PWM1	Digital Output (Open Drain). Pulse width modulated output to control the speed of Fan 1. Requires 10 k Ω typical pull-up.
	XTO	Also functions as the output from the XNOR tree in XNOR test mode.
16	SDA	Digital I/O (Open Drain). SMBus bidirectional serial data. Requires 10 k Ω typical pull-up.

Table 3. ELECTRICAL	SPECIFICATIONS $(T_A = T_I)$	AIN TO TMAX. $V_{CC} = V_{II}$	IN to VMAX. unless o	therwise noted.) (Note 1)

			, ,	,	
Parameter	Test Conditions/Comments	Min	Тур	Max	Unit
POWER SUPPLY		-			
Supply Voltage		3.0	3.3	5.5	V
Supply Current, I _{CC}	Interface Inactive, ADC Active Standby Mode			3 20	mA μA
TEMPERATURE-TO-DIGITAL CONVER	TER	-			
Local Sensor Accuracy	$\begin{array}{l} 0^{\circ}C \leq T_{A} \leq 70^{\circ}C \\ -40^{\circ}C \leq T_{A} \leq +100^{\circ}C \\ -40^{\circ}C \leq T_{A} \leq +120^{\circ}C \end{array}$	-3.5 -4	_ _ _	±1.5 +2 +2	°C
Resolution		-	0.25	-	°C
Remote Diode Sensor Accuracy	$\begin{array}{l} 0^{\circ}C \leq T_{A} \leq 70^{\circ}C; \ 0^{\circ}C \leq T_{D} \leq 120^{\circ}C \\ 0^{\circ}C \leq T_{A} \leq 105^{\circ}C; \ 0^{\circ}C \leq T_{D} \leq 120^{\circ}C \\ -40^{\circ}C \leq T_{A} \leq +120^{\circ}C; \ 0^{\circ}C \leq T_{D} \leq +120^{\circ}C \end{array}$		±0.5 _ _	±1.5 +2 +2	°C
Resolution		-	0.25	-	°C

ELECTRICAL SPECIFICATION	ONS ($T_A = T_{MIN}$ to T_{MAX} , $V_{CC} = V_{MIN}$ to V_{MAX}	, unless oth	erwise noted.) (N	lote 1)	
Parameter	Test Conditions/Comments	Min	Тур	Max	Unit
IGITAL INPUTS (SCL, SDA)					
n Voltage, V _{IH}		2.0	-	-	V
Voltage, V _{IL}		-	-	0.4	V
8		-	500	-	mV
NPUT LOGIC LEVELS (TACH I	NPUTS)				
n Voltage, V _{IH}	Maximum Input Voltage	2.0		_ 5.5	V
Voltage, V _{IL}	Minimum Input Voltage	-0.3	- -	0.8 -	-

TYPICAL PERFORMANCE CHARACTERISTICS







Figure 5. External Temperature Error vs. Capacitance Between D+ and D-

Product Description

The ADT7467 is a complete thermal monitor and multiple fan controller for systems requiring thermal monitoring and cooling. The device communicates with the system via a serial system management bus. The serial bus controller has a serial data line for reading and writing addresses and data (Pin 16) and an input line for the serial clock (Pin 1). All control and programming functions for the ADT7467 are performed over the serial bus. In addition, one of two pins can be reconfigured as an SMBALERT output to signal out-of-limit conditions.

Comparison between ADT7460 and ADT7467

The ADT7467 is an upgrade from the ADT7460. The ADT7467 and ADT7460 are almost pin and register map compatible. The ADT7467 and ADT7460 have the following differences:

- 1. On the ADT7467, the PWM drive signals can be configured as either high frequency or low frequency drives. The low frequency option is programmable between 10 Hz and 100 Hz. The high frequency option is 22.5 kHz. On the ADT7460, only the low frequency option is available.
- 2. Once V_{CC} and V_{CCP} are powered up, monitoring of temperature and fan speeds is enabled on the ADT7467. If V_{CCP} is never powered up, monitoring is enabled when the first SMBus transaction with the ADT7467 is complete. On the ADT7460, the STRT bit in Configuration Register 1 must be set to enable monitoring.
- 3. The fans are switched off by default upon power-up of the ADT7467. On the ADT7460, the fans run at full speed upon power-up. Fail-safe cooling is provided on the ADT7467. If the measured temperature exceeds the THERM limit (100°C), the fans run at full speed. Fail-safe cooling is also provided 4.6 sec after V_{CCP} is powered up. The fans operate at full speed if the ADT7467 has not been addressed via the SMBus within 4.6 sec of when the V_{CCP} is powered up. This protects the system in the event that the SMBus fails. The ADT7467 can be programmed at any time, and it behaves as programmed. If V_{CCP} is never powered up, fail-safe cooling is effectively disabled. If V_{CCP} is disabled, writing to the ADT7467 at any time causes the ADT7467 to operate normally.
- 4. Series resistance cancellation (SRC) is provided on the remote temperature channels on the ADT7467, but not on the ADT7460. SRC automatically cancels linear offset introduced by a series resistance between the thermal diode and the sensor.
- 5. The ADT7467 has an extended temperature measurement range. The measurement range goes

from -64°C to +191°C. On the ADT7460, the measurement range is from -127°C to +127°C. This means that the ADT7467 can measure higher temperatures. The ADT7467 also includes the ADT7460 temperature range; the temperature measurement range can be switched by setting Bit 0 of Configuration Register 5.

- 6. The ADT7467 maximum fan speed (% duty cycle) in the automatic fan speed control loop can be programmed. The maximum fan speed is 100% duty cycle on the ADT7460 and is not programmable.
- 7. The offset register in the ADT7467 is programmable up to ±64°C with 0.50°C resolution. The offset register of the ADT7460 is programmable up to ±32°C with 0.25°C resolution.
- 8. V_{CCP} is monitored on Pin 14 of the ADT7467 and can be used to set the threshold for THERM (PROCHOT) (2/3 of V_{CCP}). 2.5 V is monitored on Pin 14 of the ADT7460. The threshold for THERM (PROCHOT) is set at V_{IH} = 1.7 V and V_{IL} = 0.8 V on the ADT7460.
- 9. On the ADT7460, Pin 14 could be reconfigured as SMBALERT. This is not available on the ADT7467. SMBALERT can be enabled instead on Pin 9.
- 10. A GPIO can also be made available on Pin 9 on the ADT7467. This is not available on the ADT7460. Set the GPIO polarity and direction in Configuration Register 5. The GPIO status bit is Bit 5 of Status Register 2 (it is shared with TACH4 and THERM because only one can be enabled at a time).
- 11. The ADT7460 has three possible SMBus addresses, which are selectable using the address select and address enable pins. The ADT7467 has one SMBus address available at Address 0x2E.

Due to the inclusion of extra functionality, the register map has changed, including an additional configuration register, Configuration Register 5 at Address 0x7C.

Configuration Register 5

Bit 0: If Bit 0 is set to 1, the ADT7467, in terms of temperature, is backward compatible with the ADT7460. Measurements, including T_{MIN} calibration circuit and fan control, work in the range –127°C to +127°C. In addition, care should be taken in reprogramming the temperature limits (T_{MIN} , operating point, THERM) to their desired twos complement value, because the power-on default for them is at Offset 64. The extended temperature range is –64°C to 191°C. The default is 1, which is in the –64°C to +191°C temperature range.

Bit 1 = 0 is the high frequency (22.5 kHz) fan drive signal.

Bit 1 = 1 switches the fan drive to low frequency PWM, programmable between 10 Hz and 100 Hz, the same as the ADT7460. The default is 0, or HF PWM.

Bit 2 sets the direction for the GPIO: 0 = input, 1 = output. Bit 3 sets the GPIO polarity: 0 = active low, 1 = active high.

Setting the Functionality of Pin 9

Pin 9 on the ADT7467 has four possible functions: SMBALERT, THERM, GPIO, and TACH4. The user chooses the required functionality by setting Bit 0 and Bit 1 of Configuration Register 4 at Address 0x7D.

In the ADT7467, write operations contain either one or two bytes, and read operations contain one byte. To write data to a device data register or read data from it, the address pointer register must first be set. The first byte of a write operation always contains an address, which is stored in the address pointer register, and the second byte, if there is a second byte, is written to the register selected by the address pointer register.

This write operation is illustrated in Figure 15. The device address is sent over the bus, and then R/W is set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register, and the second data byte is the data written to that internal data register.

When reading data from a register, there are two possibilities:

1. If the address pointer register value of the ADT7467 is unknown or not the desired value, it must be set to the correct value before data can be read from the desired data register. This is achieved by writing a data byte containing the register address to the ADT7467. This is shown in Figure 16. A read operation is then performed consisting of the serial bus address and the R/W bit set to 1, followed by the data byte read from the data register. This is shown in Figure 17.

2. If the address pointer register is known to be at the desired address, data can be read from the corresponding data register without first writing to the address pointer register, as shown in Figure 17.

If the address pointer register is already at the correct value, it is possible to read a data byte from the data register without first writing to the address pointer register. However, it is not possible to write data to a register without writing to the address pointer register, because the first data byte of a write is always written to the address pointer register.

In addition to supporting the send byte and receive byte protocols, the ADT7467 also supports the read byte protocol. (See the Intel System Management Bus Specifications Rev. 2 for more information.)

If several read or write operations must be performed in succession, the master can send a repeat start condition instead of a stop condition to begin a new operation.



Figure 15. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

Write Operations

The SMBus specification defines several protocols for different types of read and write operations. The ones used in the ADT7467 are discussed here. The following abbreviations are used in Figure 18 through Figure 20:

- S = start
- P = stop
- R = read
- W = write
- A = acknowledge
- $\overline{A} = no acknowledge$

The ADT7467 uses the following SMBus write protocols.

Send Byte

In this operation, the master device sends a single command byte to a slave device as follows:

- 1. The master device asserts a start condition on SDA.
- 2. The master sends the 7-bit slave address followed by the write bit (low).
- 3. The addressed slave device asserts an acknowledge on SDA.
- 4. The master sends a command code.
- 5. The slave asserts an acknowledge on SDA.
- 6. The master asserts a stop condition on SDA, and the transaction ends.

For the ADT7467, the send byte protocol is used to write a register address to RAM for a subsequent single byte read from the same address. This operation is illustrated in Figure 18.



Figure 18. Setting a Register Address for Subsequent Read

If the master is required to read data from the register directly after setting up the address, it can assert a repeat start condition immediately after the final acknowledge and carry out a single byte read without asserting an intermediate stop condition.

Write Byte

In this operation, the master device sends a command byte and one data byte to the slave device as follows:

- 1. The master device asserts a start condition on SDA.
- 2. The master sends the 7-bit slave address followed by the write bit (low).
- 3. The addressed slave device asserts an acknowledge on SDA.
- 4. The master sends a command code.
- 5. The slave asserts an acknowledge on SDA.
- 6. The master sends a data byte.
- 7. The slave asserts an acknowledge on SDA.

8. The master asserts a stop condition on SDA to end the transaction.

This operation is illustrated in Figure 19.

1	2		3	4	5	6	7	8
s	Slave Address	W	A	Slave Address	A	Data	A	Ρ

Figure 19. Single Byte Write to a Register

Read Operations

The ADT7467 uses the following SMBus read protocols.

Receive Byte

This operation is useful when repeatedly reading a single register. The register address must have been set up previously. In this operation, the master device receives a single byte from a slave device as follows:

- 1. The master device asserts a start condition on SDA.
- 2. The master sends the 7-bit slave address followed by the read bit (high).
- 3. The addressed slave device asserts an acknowledge on SDA.
- 4. The master receives a data byte.
- 5. The master asserts a no acknowledge on SDA.
- 6. The master asserts a stop condition on SDA, and the transaction ends.

In the ADT7467, the receive byte protocol is used to read a single byte of data from a register whose address has previously been set by a send byte or write byte operation. This operation is illustrated in Figure 20.

1	2		3	4	5	6
s	Slave Address	R	A	Data	Ā	Ρ

Figure 20. Single Byte Read from a Register

Alert Response Address

Alert response address (ARA) is a feature of SMBus devices that allows an interrupting device to identify itself to the host when multiple devices exist on the same bus.

The <u>SMBALERT</u> output can be used as either an interrupt output or an <u>SMBALERT</u>. One or more outputs can be connected to a common <u>SMBALERT</u> line connected to the master. If a device's <u>SMBALERT</u> line goes low, the following procedure occurs:

- 1. SMBALERT is pulled low.
- 2. The master initiates a read operation and sends the alert response address (ARA = 0001 100). This is a general call address that must not be used as a specific device address.
- 3. The device whose SMBALERT

device is now known and can be interrogated in the usual way.

- 4. If more than one device's SMBALERT output is low, the one with the lowest device address has priority in accordance with normal SMBus arbitration.
- 5. Once the ADT7467 has responded to the alert response address, the master must read the status registers. The SMBALERT is cleared only if the error condition is absent.

SMBus Timeout

The ADT7467 includes an SMBus timeout feature. If there is no SMBus activity for 35 ms, the ADT7467 assumes that the bus is locked and releases the bus. This prevents the device

Table 5. PROGRAMMING SINGLE-CHANNEL ADC MODE

Bits <7:5>, Register 0x55	Channel Selected
001	V _{CCP}
010	V _{CC}
101	Remote 1 Temperature
110	Local Temperature
111	Remote 2 Temperature

Configuration Register 2 (0x73)

<4> = 1, Averaging Off

<5> = 1, Bypass Input Attenuators

<6> = 1, Single-channel Conversion Mode

TACH1 Minimum High Byte (0x55)

<7:5> Selects ADC Channel for Single-channel Convert Mode

Table 6. 10-BIT ANALOG-TO-DIGITA	L OUTPUT CODE VS. VIN
----------------------------------	-----------------------

	Input Voltage	A/D	Output	
V _{CC} (5 V _{IN})	V _{CC} (3.3 V _{IN})	V _{CCP}	Decimal	Binary (10 Bits)
<0.0065	<0.0042	<0.00293	0	00000000 00
0.0065 to 0.0130	0.0042 to 0.0085	0.0293 to 0.0058	1	0000000 01
0.0130 to 0.0195	0.0085 to 0.0128	0.0058 to 0.0087	2	0000000 10
0.0195 to 0.0260	0.0128 to 0.0171	0.0087 to 0.0117	3	0000000 11
0.0260 to 0.0325	0.0171 to 0.0214	0.0117 to 0.0146	4	00000001 00
0.0325 to 0.0390	0.0214 to 0.0257	0.0146 to 0.0175	5	0000001 01
0.0390 to 0.0455	0.0257 to 0.0300	0.0175 to 0.0205	6	00000001 10
0.0455 to 0.0521	0.0300 to 0.0343	0.0205 to 0.0234	7	00000001 11
0.0521 to 0.0586	0.0343 to 0.0386	0.0234 to 0.0263	8	00000010 00
1.6675 to 1.6740	1.100 to 1.1042	0.7500 to 0.7529	256 (1/4 scale)	0100000 00

512 (1/2 scale)

356 (1/4 scale)

Temperature Measurement

A simple method of measuring temperature is to exploit the negative temperature coefficient of a diode, measuring the base-emitter voltage (V_{BE}) of a transistor operated at constant current. Unfortunately, this technique requires calibration to null the effect of the absolute value of V_{BE} , which varies from each device.

The technique used in the ADT7467 is to measure the change in V_{BE} when the device is operated at three currents. Previous devices have used only two operating currents, but the use of a third current allows automatic cancellation of resistances in series with the external temperature sensor.

Figure 23 shows the input signal conditioning used to measure the output of an external temperature sensor. This figure shows the external sensor as a substrate transistor, but it could equally be a discrete transistor. If a discrete transistor is used, the collector is not grounded and should be linked to the base. To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground but is biased above ground by an internal diode at the D– input. C1 can optionally be added as a noise filter (the recommended maximum value is 1,000 pF). However, a better option in noisy environments is to add a filter as described in the Noise Filtering section.

Local Temperature Measurement

The ADT7467 contains an on-chip band gap temperature sensor whose output is digitized by the on-chip 10-bit ADC. The 8-bit MSB temperature data is stored in the local temperature register (Address 0x26). Because both positive and negative temperatures can be measured, the temperature data is stored in Offset 64 format or twos complement format, as shown in Table 7 and Table 8. Theoretically, the temperature sensor and ADC can measure temperatures from -128° C to $+127^{\circ}$ C (or -64° C to $+191^{\circ}$ C in the extended temperature range) with a resolution of 0.25^{\circ}C. However, this exceeds the operating temperature range of the device, preventing local temperature measurements outside the ADT7467 operating temperature range.

Remote Temperature Measurement

The ADT7467 can measure the temperature of two remote diode sensors or diode-connected transistors connected to Pin 10 and Pin 11 or to Pin 12 and Pin 13.

The forward voltage of a diode or diode-connected transistor operated at a constant current exhibits a negative temperature coefficient of about $-2 \text{ mV/}^{\circ}\text{C}$. Unfortunately, the absolute value of V_{BE} varies from each device and thus requires individual calibration; therefore, the technique is unsuitable for mass production. The technique used in the ADT7467 is to measure the change in V_{BE} when the device is operated at three currents. This is given by:

$$\Delta V_{BE} = kT/q \times \ln(N)$$
 (eq. 1)

where:

k is Boltzmann's constant. q is the charge on the carrier. T is the absolute temperature in Kelvins. N is the ratio of the two currents.

Figure 22 shows the input signal conditioning used to measure the output of a remote temperature sensor. This figure shows the external sensor as a substrate transistor provided for temperature monitoring on some microprocessors. It could also be a discrete transistor such as a 2N3904/2N3906.



Figure 22. Signal Conditioning for Remote Diode Temperature Sensors

If a discrete transistor is used with the ADT7467, the best accuracy is obtained by choosing devices according to the following criteria:

- Base-emitter voltage is greater than 0.25 V at $6 \,\mu A$ with the highest operating temperature.
- Base-emitter voltage is less than 0.95 V at 100 μ A with the lowest operating temperature.
- Base resistance is less than 100 Ω .
- There is a small variation in h_{FE}

temperature below -63° C is entered, the temperature is clamped to -63° C. In this mode, the diode fault condition remains -128° C = 1000 0000, whereas the fault condition is represented by -64° C = 0000 0000 in the extended temperature range (-64° C to $+191^{\circ}$ C).

Table 9. TEMPERATURE MEASUREMENT REGISTERS

Register	Description	Default
0x25	Remote 1 Temperature	0x01
0x26	Local Temperature	0x01
0x27	Remote 2 Temperature	0x01
0x77	Extended Resolution 2	0x00

Table 10. EXTENDED RESOLUTION TEMPERATURE MEASUREMENT REGISTER BITS

Bit	Mnemonic	Description
<7:6>	TDM2	Remote 2 Temperature LSBs
<5:4>	LTMP	Local Temperature LSBs
<3:2>	TDM1	Remote 1 Temperature LSBs

Temperature Measurement Limit Registers

High and low limit registers are associated with each temperature measurement channel. Exceeding the programmed high or low limit sets the appropriate status bit and can also generate SMBALERT interrupts.

Table 11. TEMPERATURE MEASUREMENT LIMIT REGISTERS

Register	Description	Default
0x4E	Remote 1 Temperature Low Limit	0x01
0x4F	Remote 1 Temperature High Limit	0x7F
0x50	Local Temperature Low Limit	0x01
0x51	Local Temperature High Limit	0x7F
0x52	Remote 2 Temperature Low Limit	0x01
0x53	Remote 2 Temperature High Limit	0x7F

Reading Temperature from the ADT7467

It is important to note that temperature can be read from the ADT7467 as an 8-bit value (with 1°C resolution) or as a 10-bit value (with 0.25°C resolution). If only 1°C resolution is required, the temperature readings can be read at **Overtemperature Events**

Overtemperature events on a temperature channel can be automatically detected and dealt with in automatic fan speed control mode. Register 0x6A to Register 0x6C contain the THERM temperature limits. When a temperature exceeds its THERM temperature limit, all PWM outputs run at the maximum PWM duty cycle (0x38, 0x39, 0x3A); therefore, fans run at the fastest speed allowed and continue running at this speed until the temperature drops below THERM minus hysteresis. (This can be disabled by setting the BOOST bit in Configuration Register 3, Bit 2, Register 0x78.) The hysteresis value for that THERM temperature limit is the value programmed into Register 0x6D and Register 0x6E (hysteresis registers). The default hysteresis value is 4°C.



Figure 26. THERM Temperature Limit Operation

Limits, Status Registers, and 787drs, rup

Analog Monitoring Cycle Time

The analog monitoring cycle begins when a 1 is written to the start bit (Bit 0) of Configuration Register 1 (0x40). By default, the ADT7463 powers up with this bit set. The ADC measures each analog input in turn and, as each measurement is completed, the result is automatically stored in the appropriate value register. This round-robin monitoring cycle continues unless disabled by writing a 0 to Bit 0 of Configuration Register 1.

As the ADC is normally left to free-run in this manner, the time to monitor all analog inputs is normally not of interest because the most recently measured value of an input can be



Figure 27. SMBALERT and Status Bit Behavior

Figure 27 shows how the SMBALERT output and sticky status bits behave. Once a limit is exceeded, the corresponding status bit is set to 1. The status bit remains set until the error condition subsides and the status register is read. The status bits are referred to as sticky because they remain set until read by software. This ensures that an out-of-limit event cannot be missed if software is polling the device periodically. Note that the SMBALERT output remains low both for the duration that a reading is out of limit and until the status register has been read. This has implications on how software handles the interrupt.

Handling SMBALERT Interrupts

To prevent the system from being tied up with servicing interrupts, it is recommend to handle the SMBALERT interrupt as follows:

- 1. Detect the SMBALERT assertion.
- 2. Enter the interrupt handler.
- 3. Read the status registers to identify the interrupt source.
- 4. Mask the interrupt source by setting the appropriate mask bit in the interrupt mask registers (Register 0x74 and Register 0x75).
- 5. Take the appropriate action for a given interrupt source.
- 6. Exit the interrupt handler.
- 7. Periodically poll the status registers. If the interrupt status bit has cleared, reset the corresponding interrupt mask bit to 0. This causes the SMBALERT output and status bits to behave as shown in Figure 28.

Figure 28. Effect of Masking the Interrupt Source on SMBALERT Output

Table 24. CONFIGURING PIN 9

Bit 1	Bit 0	Function
0	0	TACH4
0	1	THERM
1	0	SMBALERT
1	1	GPIO

Once Pin 9 is configured as THERM, it must be enabled (Bit 1, Configuration Register 3 at Address 0x78).

THERM as an Input

When THERM is configured as an input, the user can time assertions on the THERM pin. This can be useful for connecting to the PROCHOT output of a CPU to gauge system performance.

The user can also set up the ADT7467 so that when the THERM pin is driven low externally, the fans run at 100%. The fans run at 100% for the duration of the time that the THERM pin is pulled low. This is done by setting the BOOST bit (Bit 2) in Configuration Register 3 (0x78) to 1. This only works if the fan is already running, for example, in manual mode when the current duty cycle is above 0x00, or in automatic mode when the temperature is above T_{MIN}. If the temperature is below T_{MIN} or if the duty cycle in manual mode is set to 0x00, externally pulling THERM low has no effect. See Figure 29 for more information.



THERM Asserted to LOW as an Input: Fans Do Not Go to 100% Because Temperature is Above T_{MIN} and Fans are Already Running

Figure 29. Asserting THERM Low as an Input in Automatic Fan Speed Control Mode

THERM Timer

The ADT7467 has an internal timer to measure THERM assertion time. For example, the THERM input can be connected to the PROCHOT output of a Pentium[®] 4 CPU to measure system performance. The THERM

Generating SMBALERT Interrupts from THERM Timer Events

The ADT7467 can generate SMBALERTs when a programmable THERM timer limit has been exceeded. This allows the system designer to ignore brief, infrequent THERM

BIOS could read the THERM timer once an hour to determine the cumulative THERM assertion time. If, for example, the total THERM assertion time is <22.76 ms in Hour 1, >182.08 ms in Hour 2, and >2.914 sec in Hour 3, this can indicate that system performance is degrading significantly, because THERM is asserting more frequently on an hourly basis.

Alternatively, OS or BIOS level software can timestamp when the system is powered on. If an SMBALERT is generated because the THERM timer limit has been exceeded, another timestamp can be taken. The difference in time can be calculated for a fixed THERM timer limit. For example, if it takes one week for a THERM timer limit of 2.914 sec to be exceeded and the next time it takes only 1 hour, this is an indication of a serious degradation in system performance.

Configuring the THERM Pin as an Output

In addition to monitoring THERM as an input, the ADT7467 can optionally drive THERM low as an output. In cases where PROCHOT is bidirectional, THERM can be used to throttle the processor by asserting PROCHOT. The user can preprogram system-critical thermal limits. If the temperature exceeds a thermal limit by 0.25°C, THERM asserts low. If the temperature is still above the thermal limit on the next monitoring cycle, THERM stays low. THERM remains asserted low until the temperature is equal to or below the thermal limit. Because the temperature for that channel is measured only once for every monitoring cycle, it is guaranteed to remain low for at least one monitoring cycle after THERM is asserted.

The THERM pin can be configured to assert low if the Remote 1, local, or Remote 2 THERM temperature limits are exceeded by 0.25°C. The THERM temperature limit registers are at Register 0x6A, Register 0x6B, and Register 0x6C, respectively. Setting Bit 3 of Register 0x5F, Register 0x60, and Register 0x61 enables the THERM output feature for the Remote 1, local, and Remote 2 temperature channels, respectively. Figure 32 shows how the THERM pin asserts

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Figure 33 uses a 10 k Ω pull-up resisto signal. This assumes that the TACH open-collector from the fan. In all cases, t from the fan must be kept below 5 V maxi damaging the ADT7467. If in doubt as to used has an open-collector or totem pole T one of the input signal conditioning circuits Speed Measurement section.

Figure 34 shows a fan drive circuit transistor such as a general-purpose MMBT these devices are inexpensive, they tend to I current handling capabilities and higher or MOSFETs. When choosing a transistor, can to ensure that it meets the fan's current req

Ensure that the base resistor is chose transistor is saturated when the fan is power

Because 4-wire fans are powered conti speed is not switched on or off as with driven/powered fans. This enables it to per 3-wire fans, especially for high frequen Figure 35 shows a typical drive circuit for

12 V 12 10 kΩ N4148 10 kΩ 12 V TACHx AN TAC ADT7467 3.3 V ≩665 Ω **PWMx** MBT2222 Figure 34. Driving a 3-wire Fan bina an NPN Transistor 12 V 12 2 V, 4-WIRE FAN $10 k\Omega$ $10 \ k\Omega$ Vrr TACHx Э ТАСН TACH Орwм Ş 4.7 kΩ ADT7467 3.3 V ę **≥**2 kΩ **PWMx**

Figure 35. Driving a 4-wire Fan

Driving Two Fans from PWM3

The ADT7467 has four TACH inputs available for fan speed measurement, but only three PWM drive outputs. If a fourth fan is used in the system, it should be driven from the PWM3 output in parallel with the third fan. Figure 36 shows how to drive two fans in parallel using low cost NPN transistors. Figure 37 shows the equivalent circuit using a MOSFET.



Figure 36. Interfacing Two Fans in Parallel to the PWM3 Output Using Low Cost NPN Transistors





Table 25. SYNC: ENHANCE ACOUSTICS REGISTER 1 (REG. 0X62)

Bit	Mnemonic	Description
<4>	SYNC	1 Synchronizes TACH2, TACH3, and TACH4 to PWM3.

Driving 2-wire Fans

TACH Inputs

When configured as TACH inputs, Pin 4, Pin 6, Pin 7, and Pin 9 are open-drain TACH inputs intended for fan speed measurement.

Signal conditioning in the ADT7467 accommodates the slow rise and fall times typical of fan tachometer outputs. The maximum input signal range is 0 V to 5 V, even when V_{CC} is less than 5 V. In the event that these inputs are supplied from fan outputs that exceed 0 V to 5 V, either resistive attenuation of the fan signal or diode clamping must be included to keep inputs within an acceptable range.

Figure 41 to Figure 44 show circuits for most common fan TACH outputs. If the fan TACH output has a resistive pull-up to V_{CC} , it can be connected directly to the fan input, as shown in Figure 41.



Figure 41. Fan with TACH Pull-up to $V_{\mbox{CC}}$

If the fan output has a resistive pull-up to 12 V (or another

register). This register contains two bits for each fan, allowing counting of one, two (default), three, or four TACH pulses.



Fan Speed Measurement Registers

The fan tachometer readings are 16-bit values consisting of a 2-byte read from the ADT7467.

Table 26	ΕΛΝ	SDEED		SUDEN	PECIS	TEDS
Table 20.	FAIN	SPEED	IVIEA	SUKEN	REGIO	IERO

Register	Description	Default
0x28	TACH1 Low Byte	0x00
0x29	TACH1 High Byte	0x00
0x2A	TACH2 Low Byte	0x00
0x2B	TACH2 High Byte	0x00
0x2C	TACH3 Low Byte	0x00
0x2D	TACH3 High Byte	0x00
0x2E	TACH4 Low Byte	0x00
0x2F	TACH4 High Byte	0x00

Reading Fan Speed from the ADT7467

The measurement of fan speeds involves a 2-register read for each measurement. The low byte should be read first. This freezes the high byte until both high and low byte registers are read, preventing erroneous TACH readings. The fan tachometer reading registers report the number of 11.11 µs period clocks (90 kHz oscillator) gated to the fan speed counter from the rising edge of the first fan TACH pulse to the rising edge of the third fan TACH pulse, assuming two pulses per revolution are being counted. Because the device is essentially measuring the fan TACH period, the higher the count value, the slower the fan runs. A 16-bit fan tachometer reading of 0xFFFF indicates either that the fan has stalled or is running very slowly (<100 RPM).

High limit > comparison performed

Because the actual fan TACH period is being measured, falling below a fan TACH limit by 1 sets the appropriate status bit and can be used to generate an SMBALERT.

Fan TACH Limit Registers

The fan TACH limit registers are 16-bit values consisting of two bytes.

Register	Description	Default
0x54	TACH1 Minimum Low Byte	0xFF
0x55	TACH1 Minimum High Byte	0xFF
0x56	TACH2 Minimum Low Byte	0xFF
0x57	TACH2 Minimum High Byte	0xFF
0x58	TACH3 Minimum Low Byte	0xFF
0x59	TACH3 Minimum High Byte	0xFF
0x5A	TACH4 Minimum Low Byte	0xFF
0x5B	TACH4 Minimum High Byte	0xFF

Table 27. FAN TACH LIMIT REGISTERS

Fan Speed Measurement Rate

The fan TACH readings are normally updated once every second.

When set, the FAST bit (Bit 3) of Configuration Register 3 (0x78) updates the fan TACH readings every 250 ms.

If a fan is powered directly from 5 V or 12 V and is not driven by a PWM channel, its associated dc bit in Configuration Register 3 should be set. This allows TACH readings to be taken on a continuous basis for fans connected directly to a dc source. For optimal results, the associated dc bit should always be set when using 4-wire fans.

Calculating Fan Speed

Assuming a fan with two pulses per revolution (and two pulses per revolution being measured), fan speed is calculated by

Fan Speed (RPM) = $(90,000 \times 60)$ /Fan TACH Reading

where Fan TACH Reading is the 16-bit fan tachometer reading.

Example

TACH1 high byte (Register 0x29) = 0x17TACH1 low byte (Register 0x28) = 0xFF

What is Fan 1 speed in RPM?

Fan 1 TACH Reading = 0x17FF = 6143 (decimal) RPM = (f × 60)/Fan 1 TACH Reading RPM = (90,000 × 60)/6143 Fan Speed = 879 RPM

Fan Pulses per Revolution

Different fan models can output either one, two, three, or four TACH pulses per revolution. Once the number of fan TACH pulses has been determined, it can be programmed into the fan pulses per revolution register (0x7B) for each fan. Alternatively, this register can be used to determine the

number of pulses per revolution output for a given fan. By plotting fan speed measurements at 100% speed with different pulses per revolution setting, the smoothest graph with the lowest ripple determines the correct pulses per revolution value.

Table 28. FAN PULSES/REVOLUTION REGISTER (REG. 0X7B)

Bit	Mnemonic	Description
<1:0>		

PWM Logic State

The PWM outputs can be programmed high for 100% duty cycle (non-inverted) or programmed low for 100% duty cycle (inverted).

Table 33. PWM1 TO PWM3 CONFIGURATION (REG. 0X5C TO 0X5E) BITS

Bit	Mnemonic	Description
<4>	INV	0 = logic high for 100% PWM duty cycle

Low Frequency Mode PWM Drive Frequency

The PWM drive frequency can be adjusted for the application. Register 0x5F to Register 0x61 configure the PWM frequency for PWM1 to PWM3, respectively. In high frequency mode, the PWM drive frequency is 22.5 kHz and cannot be changed.

Table 34. PWM1 FREQUENCY REGISTERS (REG. 0X5F TO 0X61)

Bit	Mnemonic	Description
<2:0>	FREQ	$\begin{array}{l} 000 = 11.0 \ \text{Hz} \\ 001 = 14.7 \ \text{Hz} \\ 010 = 22.1 \ \text{Hz} \\ 011 = 29.4 \ \text{Hz} \\ 100 = 35.3 \ \text{Hz} \ (\text{Default}) \\ 101 = 44.1 \ \text{Hz} \\ 110 = 58.8 \ \text{Hz} \\ 111 = 88.2 \ \text{Hz} \end{array}$

Fan Speed Control

The ADT7467 controls fan speed using two modes: automatic and manual.

In automatic fan speed control mode, fan speed is varied with temperature without CPU intervention once initial parameters are set up. The advantage of this is that if the system hangs, it is guaranteed that the system is protected from overheating. The automatic fan speed control incorporates a feature called dynamic T_{MIN} calibration. This feature reduces the design effort required to program the automatic fan speed control loop. For information on programming the automatic fan speed control loop and the dynamic T_{MIN} calibration, see the Automatic Fan Control Overview section.

In manual fan speed control mode, the ADT7467 allows the duty cycle of any PWM output to be manually adjusted. This can be useful if the user wants to change fan speed in software or adjust PWM duty cycle output for test purposes. Bits <7:5> of Register 0x5C to Register 0x5E (PWM Configuration) control the behavior of each PWM output.

Table 35. PWM1 TO PWM3 CONFIGURATION
(REG. 0X5C TO 0X5E) BITS

Bit	Mnemonic	Description
<7:5>	BHVR	111 = Manual Mode

In manual fan speed control mode, each PWM output can be manually updated by writing to Register 0x30 through Register 0x32 (PWMx current duty cycle registers).

Programming the PWM Current Duty Cycle Registers

The PWM current duty cycle registers are 8-bit registers that allow the PWM duty cycle for each output to be set anywhere from 0% to 100% in steps of 0.39%.

The value to be programmed into the $\ensuremath{\mathsf{PWM}_{\mathsf{MIN}}}$ register is given by

Value (decimal) = PWM_{MIN}/0.39

Example 1: For a PWM duty cycle of 50%, Value (decimal) = 50/0.39 = 128 (decimal) Value = 128 (decimal) or 0x80 (hexadecimal)

Example 2: For a PWM duty cycle of 33%, Value (decimal) = 33/0.39 = 85 (decimal) Value = 85 (decimal) or 0x54 (hexadecimal)

PWM Current Duty Cycle Registers

By reading the PWMx current duty cycle registers, the user can keep track of the current duty cycle on each PWM output even when the fans are running in automatic fan speed control mode or acoustic enhancement mode. See the Automatic Fan Control Overview section for details.

Table 36. PWM CURRENT DUTY CYCLE REGISTERS

Register	Description	Default
0x30	PWM1 Current Duty Cycle	0x00 (0%)
0x31	PWM2 Current Duty Cycle	0x00 (0%)
0x32	PWM3 Current Duty Cycle	0x00 (0%)

Miscellaneous Functions

Operating from 3.3 V Standby

The ADT7467 has been specifically designed to operate from a 3.3 V STANDBY supply. In computers that support S3 and S5 states, the core voltage of the processor is lowered in these states. If using the dynamic T_{MIN} mode, lowering the core voltage of the processor changes the CPU temperature and changes the dynamics of the system under dynamic T_{MIN} control. Likewise, when monitoring THERM, the THERM timer should be disabled during these states.

Dynamic T_{MIN} Control Register 1 (0x36) <1> V_{CCP}LO = 1

When the power is supplied from 3.3 V STANDBY and the V_{CCP} voltage drops below the V_{CCP} low limit, the following occurs:

- 1. Status Bit 1 (V_{CCP}) in Interrupt Status Register 1 is set.
- 2. SMBALERT is generated if enabled.
- 3. THERM monitoring is disabled. The THERM timer should hold its value prior to the S3 or S5 state.
- 4. Dynamic T_{MIN} control is disabled. This prevents T_{MIN} from being adjusted due to an S3 or S5 state.
- 5. The ADT7467 is prevented from shutting down.

Once the core voltage, V_{CCP} goes above the V_{CCP} low limit, everything is re-enabled and the system resumes normal operation.

XNOR Tree Test Mode

The ADT7467 includes an XNOR tree test mode. This mode is useful for in-circuit test equipment at board-level testing. By applying stimulus to the pins included in the XNOR tree, it is possible to detect opens or shorts on the system board.

Figure 46 shows the signals that are exercised in the XNOR tree test mode. The XNOR tree test is invoked by setting Bit 0 (XEN) of the XNOR tree test enable register (0x6F).



Figure 46. XNOR Tree Test

Power-On Default

When the ADT7467 is powered up, it polls the $\mathsf{V}_{\mathsf{CCP}}$ input.

If V_{CCP} stays below 0.75 V (the system CPU power rail is not powered up), the ADT7467 assumes the functionality of the default registers after the ADT7467 is addressed via any valid SMBus transaction.

If V_{CC} goes high (the system processor power rail is powered up), a fail-safe timer begins to count down. If the ADT7467 is not addressed by a valid SMBus transaction before the fail-safe timeout (4.6 sec) lapses, the ADT7467 drives the fans to full speed. If the ADT7467 is addressed by a valid SMBus transaction after this point, the fans stop and the ADT7467 assumes its default settings and begins normal operation.

If V_{CCP} goes high (the system processor power rail is powered up), a fail-safe timer begins to count down. If the ADT7467 is addressed by a valid SMBus transaction before the fail-safe timeout (4.6 sec) lapses, the ADT7467 operates normally, assuming the functionality of all default registers. See the flow chart in Figure 47.



Start Fail-

Figure 47. Power-On Flowchart

Automatic Fan Control Overview

The ADT7467 can automatically control the speed of fans based on the measured temperature. This is done independently of CPU intervention once initial parameters are set up.

The ADT7467 has a local temperature sensor and two remote temperature channels that can be connected to a CPU on-chip thermal diode (available on Intel[®] Pentium[®] class and other CPUs). These three temperature channels can be used as the basis for automatic fan speed control to drive fans using pulse-width modulation (PWM).

Automatic fan speed control reduces acoustic noise by optimizing fan speed according to accurately measured temperature. Reducing fan speed can also decrease system current consumption. The automatic fan speed control mode is very flexible due to the number of programmable parameters, including T_{MIN} and T_{RANGE} . The T_{MIN} and T_{RANGE} values for a temperature channel and, therefore, for a given fan are critical because they define the thermal characteristics of the system. Thermal validation of the system is one of the most important steps in the design process; therefore, these values should be selected carefully.

Figure 48 shows a top-level overview of the automatic fan control circuitry on the ADT7467. From a systems-level perspective, up to three system temperatures can be monitored and used to control three PWM outputs. The three PWM outputs can be used to control up to four fans. The ADT7467 allows the speed of four fans to be monitored. Each temperature channel has a thermal calibration block, allowing the designer to individually configure the thermal characteristics of each temperature channel. For example, one can decide to run the CPU fan when CPU temperature increases above 60°C and to run a chassis fan when the local temperature increases above 45°C. At this stage, the designer has not assigned these thermal calibration settings to a particular fan drive (PWM) channel. The right side of Figure 48 shows controls that are fan specific. The designer can individually control parameters such as minimum PWM duty cycle, fan speed failure thresh7Te of





Recommended Implementation

Configuring the ADT7467 as shown in Figure 53 provides the system designer with the following features:

- Two PWM outputs for control of up to three fans. (The front and rear chassis fans are connected in parallel.)
- Three TACH fan speed measurement inputs.
- V_{CC} measured internally through Pin 3.
- CPU core voltage measurement (V_{CORE}).
- CPU temperature measured using the Remote 1 temperature channel.
- Ambient temperature measured through the Remote 2 temperature channel.
- The bidirectional THERM pin allows monitoring PROCHOT output from, for example, an Intel[®] Pentium[®] 4 processor, or it can be used as an overtemperature THERM output.
- SMBALERT system interrupt output.

STEP 2: Configuring the MUX

After the system hardware configuration is determined, the fans can be assigned to particular temperature channels. Not only can fans be assigned to individual channels, but the behavior of

Mux Configuration Example

This is an example of how to configure the mux in a system using the ADT7467 to control three fans. The CPU fan sink is controlled by PWM1, the front chassis fan is controlled by PWM2, and the rear chassis fan is controlled by PWM3. The mux is configured for the following fan control behavior:

- PWM1 (CPU fan sink) is controlled by the fastest speed calculated by the local (VRM temperature) and Remote 2 (processor) temperature. In this case, the CPU fan sink is also used to cool the VRM.
- PWM2 (front chassis fan) is controlled by the Remote 1 temperature (ambient).

• PWM3 (rear chassis fan) is controlled by the Remote 1 temperature (ambient).

Example Mux Settings

- <7:5> (BHVR), PWM1 Configuration Register 0x5C 101 = fastest speed calculated by local and Remote 2 temperature controls PWM1
- <7:5> (BHVR), PWM2 Configuration Register 0x5D 000 = Remote 1 temperature controls PWM2
- <7:5> (BHVR), PWM3 Configuration Register 0x5E 000 = Remote 1 temperature controls PWM3

These settings configure the mux as shown in Figure 55.


Bit 6 (MIN2) = 1, PWM2 runs at PWM2 minimum duty cycle when the temperature is below $T_{MIN} - T_{HYST}$. Bit 5 (MIN1) = 0, PWM1 is off (0% PWM duty cycle) when the temperature is below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 1, PWM1 runs at PWM1 minimum duty cycle when the temperature is below $T_{MIN} - T_{HYST}$.



Figure 56. Understanding the $T_{\mbox{MIN}}$ Parameter

More than one PWM output can be controlled from a single temperature measurement channel. For example, Remote 1 temperature can control PWM1 and PWM2 outputs. If two fans are used on PWM1 and PWM2, each fan's characteristics can be set up differently. As a result, Fan 1 driven by PWM1 can have a different PWM_{MIN} value than that of Fan 2 connected to PWM2. In Figure 58, PWM1_{MIN} (front fan) is turned on at a minimum duty cycle of 20%, and PWM2_{MIN} (rear fan) turns on at a minimum of 40% duty cycle; however, both fans turn on at the same temperature, defined by T_{MIN}.



Figure 58. Operating Two Fans from a Single Temperature Channel

Programming the PWM_{MIN} Registers

The PWM_{MIN} registers are 8-bit registers that allow the minimum PWM duty cycle for each output to be configured from 0% to 100%. This allows the minimum PWM duty cycle to be set in steps of 0.39%.

The value to be programmed into the PWM_{MIN} register is given by:

Value (decimal) = PWM_{MIN}/0.39%

Example 1: For a minimum PWM duty cycle of 50%,

Value (decimal) = 50%/0.39% = 128 (decimal) Value = 128 (decimal) or 0x80 (hexadecimal)

Example 2: For a minimum PWM duty cycle of 33%,

Value (decimal) = 33%/0.39% = 85 (decimal) Value = 85 (decimal)I or 0x54 (hexadecimal)

PWM_{MIN} Registers

Register 0x64, PWM1 minimum duty cycle = 0x80 (50% default)

Register 0x65 PWM2 minimum duty cycle = 0x80 (50% default)

Register 0x66, PWM3 minimum duty cycle = 0x80 (50% default)

Fan Speed and PWM Duty Cycle

The PWM duty cycle does not directly correlate to fan speed in RPM. Running a fan at 33% PWM duty cycle does not equate to running the fan at 33% speed. Driving a fan at 33% PWM duty cycle runs the fan at closer to 50% of its full speed, because fan speed as a percentage of RPM generally relates to the square root of the PWM duty cycle. Given a PWM square wave as the drive signal, fan speed in RPM approximates to

% fan speed =
$$\sqrt{PWM}$$
 duty cycle \times 10

STEP 5: PWM_{MAX} for PWM (Fan) Outputs

 PWM_{MAX} is the maximum duty cycle that each fan in the system runs at during the automatic fan speed control loop. For maximum system acoustic benefit, PWM_{MAX} should be as low as possible but capable of keeping the processor below its maximum temperature limit, even in a worst-case scenario. If the THERM temperature limit is exceeded, the fans are still boosted to 100% for fail-safe cooling.

There is a PWM_{MAX} limit for each fan channel. The default value of this register is 0xFF and, therefore, has no effect unless it is programmed.



Figure 59. PWM_{MAX} Determines Maximum PWM Duty Cycle Below the THERM Temperature Limit

Programming the PWM_{MAX} Registers

The PWM_{MAX} registers are 8-bit registers that allow the maximum PWM duty cycle for each output to be configured from 0% to 100%. This allows the maximum PWM duty cycle to be set in steps of 0.39%.

The value to be programmed into the $\ensuremath{\mathsf{PWM}_{\mathsf{MAX}}}$ register is given by

Value (decimal) = PWM_{MAX}/0.39%

Example 1: For a maximum PWM duty cycle of 50%, Value (decimal) = 50%/0.39% = 128 (decimal) Value = 128 (decimal) or 0x80 (hexadecimal)

Example 2: For a minimum PWM duty cycle of 75%, Value (decimal) = 75%/0.39% = 192 (decimal) Value = 192 (decimal) or 0xC0 (hexadecimal)

PWM_{MAX} Registers

Register 0x38, PWM1 maximum duty cycle = 0xFF (100% default)

Register 0x39, PWM2 maximum duty cycle = 0xFF (100% default)

Register 0x3A, PWM3 maximum duty cycle = 0xFF (100% default)

See the Fan Speed and PWM Duty Cycle section.

STEP 6: T_{RANGE} for Temperature Channels

 T_{RANGE} is the range of temperature over which automatic fan control occurs once the programmed T_{MIN} temperature has been exceeded. T_{RANGE} is a temperature slope, not an arbitrary value, that is, a T_{RANGE} of 40°C holds true only for PWM_{MIN} = 33%. If PWM_{MIN} is increased or decreased, the effective T_{RANGE} changes.



Figure 60. T_{RANGE} Parameter Affects Cooling Slope

The T_{RANGE} or fan control slope is determined by the following procedure:

- 1. Determine the maximum operating temperature for that channel (for example, 70°C).
- Through experimentation, determine the fan speed (PWM duty cycle value) that does not exceed the temperature at the worst-case operating points. (For example, 70°C is reached when the fans are running at 50% PWM duty cycle.)
- 3. Determine the slope of the required control loop to meet these requirements.
- The ADT7467 evaluation software can graphically program and visualize this functionality. Ask your local Analog Devices sales representative for details.



Figure 61. Adjusting PWM_{MIN} Affects T_{RANGE}

 T_{RANGE} is implemented as a slope, which means that as $\mathsf{PWM}_{\mathsf{MIN}}$ is changed, T_{RANGE} changes, but the actual slope remains the same. The higher the $\mathsf{PWM}_{\mathsf{MIN}}$ value, the smaller the effective T_{RANGE} , that is, the fan reaches full speed (100%) at a lower temperature.





For a given T_{RANGE} value, the temperature at which the fan runs at full speed, which varies with the PWM_{MIN} value, can be easily calculated.

 $T_{MAX} = T_{MIN} + (Max DC - Min DC) \times T_{RANGE} / 170$ where:

 T_{MAX} is the temperature at which the fan runs full speed. T_{MIN} is the temperature at which the fan turns on. Max DC is the maximum duty cycle (100%) = 255 decimal

Max DC is the maximum duty cycle (100%) = 255 decimal. Min DC is equal to PWM_{MIN} .

T_{RANGE} is the duty PWM duty cycle vs. temperature slope. Example 1:

Calculate T, given that $T_{MIN} = 30^{\circ}$ C, $T_{RANGE} = 40^{\circ}$ C, and PWM_{MIN} = 10% duty cycle = 26 (decimal).

 $T_{MAX} = T_{MIN} + (Max DC - Min DC) \times T_{RANGE} / 170$ $T_{MAX} = 30^{\circ}C + (100\% - 10\%) \times 40^{\circ}C / 170$

 $T_{MAX} = 30^{\circ}C + (255 - 26) \times 40^{\circ}C/170$

$$T_{MAX} = 84^{\circ}C$$
 (Effective $T_{RANGE} = 54^{\circ}C$)

Example 2:

Calculate T_{MAX} , given that $T_{MIN} = 30^{\circ}$ C, $T_{RANGE} = 40^{\circ}$ C, and PWM_{MIN} = 25% duty cycle = 64 (decimal).

$$\begin{split} T_{MAX} &= T_{MIN} + (Max DC - Min DC) \times T_{RANGE} / 170 \\ T_{MAX} &= 30^{\circ}C + (100\% - 25\%) \times 40^{\circ}C / 170 \\ T_{MAX} &= 30^{\circ}C + (255 - 64) \times 40^{\circ}C / 170 \\ T_{MAX} &= 75^{\circ}C \text{ (Effective } T_{RANGE} = 45^{\circ}C \text{)} \end{split}$$

Example 3:

Calculate T_{MAX} , given that $T_{MIN} = 30^{\circ}$ C, $T_{RANGE} = 40^{\circ}$ C, and PWM_{MIN} = 33% duty cycle = 85 (decimal).

 $T_{MAX} = T_{MIN} + (Max DC - Min DC) \times T_{RANGE} / 170$ $T_{MAX} = 30^{\circ}C + (100\% - 33\%) \times 40^{\circ}C / 170$

 $T_{MAX} = 30^{\circ}C + (255 - 85) \times 40^{\circ}C/170$

$$T_{MAX} = 70^{\circ}C$$
 (Effective $T_{RANGE} = 40^{\circ}C$)

Example 4:

Calculate T_{MAX} , given that $T_{MIN} = 30^{\circ}$ C, $T_{RANGE} = 40^{\circ}$ C, and PWM_{MIN} = 50% duty cycle = 128 (decimal).

$$\begin{split} T_{MAX} = T_{MIN} + (Max \ DC \ - \ Min \ DC) \times T_{RANGE} \ / 170 \\ T_{MAX} = 30^{\circ}C + (100\% \ - \ 50\%) \times 40^{\circ}C \ / 170 \end{split}$$



and a hard limit (such as 70°C) can be programmed as T_{MAX} (the temperature at which the fan reaches full speed) by setting T_{THERM} to that limit (for example, 70°C).

THERM Limit Registers

Register 0x6A, Remote 1 THERM limit = 0xA4 (100°C default)

Register 0x6B, local THERM limit = 0xA4 (100°C default) Register 0x6C, Remote 2 THERM limit = 0xA4 (100°C default)

Hysteresis Registers

Register 0x6D, Remote 1 and Local hysteresis register



<7:4>, Remote 1 temperature hysteresis (4°C default) <3:0>, local temperature hysteresis (4°C default)

Register 0x6E, Remote 2 temperature hysteresis register <7:4>, Remote 2 temperature hysteresis (4°C default)

Because each hysteresis setting is four bits, hysteresis values are programmable from 1°C to 15°C. It is recommended that hysteresis values are not programmed to 0°C because this disables hysteresis. In effect, this would cause the fans to cycle between normal speed and 100% speed, creating unsettling acoustic noise.



Hysteresis Registers Register 0x6D, Remote 1 and local hysteresis register <7:4>, Remote 1 temperature hysteresis (4°C default) <3:0>, local temperature hysteresis (4°C default)

Register 0x6E, Remote 2 temperature hysteresis register <7:4>, Remote 2 temperature hysteresis (4°C default)

point. Likewise, too high a T_{MIN} value causes the operating point to be exceeded, and, in turn, the ADT7467 reduces T_{MIN} to turn the fans on sooner to cool the system.

Programming Operating Point Registers

There are three operating point registers, one for each temperature channel. These 8-bit registers allow the operating point temperatures to be programmed with 1°C resolution.

Operating Point Registers

Register 0x33, Remote 1 operating point = 0xA4($100^{\circ}C$ default)

Register 0x34, local temperature operating point = 0xA4 (100°C default)

Register 0x35, Remote 2 operating point = 0xA4 (100°C default)





Figure 71. Temperature Between Operating Point and Low Temperature Limit

Because neither the operating point minus the hysteresis temperature nor the low temperature limit has been exceeded, the T_{MIN} value is not adjusted and the fan runs at a speed determined by the fixed T_{MIN} and T_{RANGE} values, defined in the automatic fan speed control mode in the Enhancing System Acoustics section.

Operating Point Exceeded-T_{MIN} Reduced

When the measured temperature is below the operating point temperature minus the hysteresis, ${\sf T}_{\sf MIN}$ remains the same.

Once the temperature exceeds the operating temperature minus the hysteresis (OP1 – Hyst), T_{MIN} decreases during the short cycle (see Figure 69) at a rate determined by the

programmed value of n. This rate also depends on the amount that the temperature has increased between this monitoring cycle and the last monitoring cycle. For example, if the temperature has increased by 1°C, then T_{MIN} is reduced by 2°C. Decreasing T_{MIN} has the effect of increasing the fan speed, thus providing more cooling to the system.

Ö

- T_{MIN} is below the high temperature limit. T_{MIN} is never allowed to exceed the high temperature limit. As a result, the high limit should be chosen carefully because it deter-mines the high limit of T_{MIN}.
- T_{MIN} is below the operating point temperature. T_{MIN} should never be allowed to increase above the operating point temperature, because the fans would not switch on until the temperature rose above the operating point.
- The temperature is above T_{MIN} . The dynamic T_{MIN} control is turned off below T_{MIN} .

Figure 73 shows how T_{MIN} increases when the current temperature is above T_{MIN} but below the low temperature limit, and how T_{MIN} is below the high temperature limit and below the operating point. Once the temperature rises above the low temperature limit, T_{MIN} remains fixed.

Figure 73. Increasing T

Enabling Dynamic T_{MIN} Control Mode

Bits <7:5> of the dynamic T_{MIN} control Register 1 (0x36) enable/disable dynamic T_{MIN} control on the temperature channels.

Table 41. DYNAMIC T_{MIN} CONTROL REGISTER 1 (REG. 0X36)

Bit	Mnemonic	Description
<5>	R1T	1 enables dynamic T_{MIN} control on the Remote 1 temperature channel. The chosen T_{MIN} value is dynamically adjusted based on the current temperature, operating point, and high and low limits for this zone.
		0 disables dynamic $T_{\rm MIN}$ control. The $T_{\rm MIN}$ value chosen is not adjusted, and the channel behaves as described in the Automatic Fan Control Overview section.
<6>	LT	1 enables dynamic T_{MIN} control on the local temperature channel. The chosen T_{MIN} value is dynamically adjusted based on the current temperature, operating point, and high and low limits for this zone.
		0 disables dynamic T_{MIN} control. The T_{MIN} value chosen is not adjusted, and the channel behaves as described in the Enhancing System Acoustics section.
<7>	R2T	1 enables the dynamic T_{MIN} control on the Remote 2 temperature channel. The chosen T_{MIN} value is dynamically adjusted based on the current temperature, operating point, and high and low limits for this zone.

R2T = 0 disables dynamic T_{MIN} control. The T_{MIN} value chosen is not adjusted, and the channel behaves as described in the Enhancing System Acoustics section.

Step 12: Ramp Rate for Acoustic Enhancement

The optimal ramp rate for acoustic enhancement can be determined through system characterization after completing the thermal optimization. If possible, the effect of each ramp rate should be logged to determine the best setting for a given solution.

Enhanced Acoustics Register 1 (0x62)

<2:0> ACOU selects the ramp rate for PWM1.

000 = 1 time slot = 35 sec 001 = 2 time slots = 17.6 sec 010 = 3 time slots = 11.8 sec 011 = 5 time slots = 7 sec 100 = 8 time slots = 4.4 sec 101 = 12 time slots = 3 sec 110 = 24 time slots = 1.6 sec

111 = 48 time slots = 0.8 sec

Enhanced Acoustics Register 2 (0x63)

<2:0> ACOU3 selects the ramp rate for PWM3.

000 = 1 time slot = 35 sec
001 = 2 time slots = 17.6 sec
010 = 3 time slots = 11.8 sec
011 = 5 time slots = 7 sec
100 = 8 time slots = 4.4 sec
101 = 12 time slots = 3 sec
110 = 24 time slots = 1.6 sec
111 = 48 time slots = 0.8 sec
<6:4> ACOU2 selects the ramp rate for PWM2.
000 = 1 time slot = 35 sec
001 = 2 time slots = 17.6 sec
010 = 3 time slots = 11.8 sec
011 = 5 time slots = 7 sec
100 = 8 time slots = 4.4 sec

101 = 12 time slots = 3 sec

110 = 24 time slots = 1.6 sec

111 = 48 time slots = 0.8 sec

Another way to view the ramp rates is as the time it takes for the PWM output to ramp up from 0% to 100% duty cycle for an instantaneous change in temperature. This can be tested by putting the ADT7467 into manual mode and changing the PWM output from 0% to 100% PWM duty cycle. The PWM output takes 35 sec to reach 100% when a ramp rate of 1 time slot is selected.

Figure 75 shows remote temperature plotted against PWM duty cycle for enhanced acoustics mode. The ramp rate is set to 48, which corresponds to the fastest ramp rate. Assume that a new temperature reading is available every 115 ms. With these settings, it takes approximately 0.76 sec to go from 33% duty cycle to 100% duty cycle (full speed). Even though the temperature increases very rapidly, the fan ramps up to full speed gradually.



Figure 75. Enhanced Acoustics Mode with Ramp Rate = 48



Enhanced Acoustics Register 2 (0x63)

immediately

<2:0> ACOU3 selects the ramp rate for PWM3. 000 = 140 sec001 = 70.4 sec010 = 47.2 sec $011 = 28 \sec 2000$ $100 = 17.6 \, \text{sec}$ $101 = 12 \, \text{sec}$ 110 = 6.4 sec111 = 3.2 sec<6:4> ACOU2 selects the ramp rate for PWM2. 000 = 140 sec001 = 70.4 sec010 = 47.2 sec011 = 28 sec $100 = 17.6 \, \text{sec}$ $101 = 12 \, \text{sec}$ 110 = 6.4 sec111 = 3.2 sec

Enhancing System Acoustics

Automatic fan speed control mode reacts instantaneously to changes in temperature, that is, the PWM duty cycle a chassis fan (on PWM2) use Remote 1 temperature. Because the Remote 1 temperature is smoothed, both fans are updated at exactly the same rate. If the chassis fan is much louder than the CPU fan, there is no way to improve its acoustics without changing the thermal solution of the CPU cooling fan.

The fan-centric approach to system acoustic enhancement controls the PWM duty cycle, driving the fan at a fixed rate (for example, 6%). Each time the PWM duty cycle is updated, it is incremented by a fixed 6%. As a result, the fan ramps smoothly to its newly calculated speed. If the temperature starts to drop, the PWM duty cycle immediately decreases by 6% at every update. Therefore, the fan ramps up or down smoothly without inherent system delay. Consider, for example, controlling the same CPU cooler fan (on PWM1) and chassis fan (on PWM2) using Remote 1 temperature. The T_{MIN} and T_{RANGE} settings have been defined in automatic fan speed control mode; that is, thermal characterization of the control loop has been optimized. Now the chassis fan is noisier than the CPU cooling fan. Using the fan-centric approach, PWM2 can be placed into acoustic enhancement mode independently of PWM1. The acoustics of the chassis fan can, therefore, be adjusted without affecting the acoustic behavior of the CPU cooling fan, even though both fans are controlled by Remote 1 temperature.

Enabling Acoustic Enhancement for Each PWM Output

Enhanced Acoustics Register 1 (0x62)

<3> = 1 enables acoustic enhancement on PWM1 output.

Enhanced Acoustics Register 2 (0x63)

<7> = 1 enables acoustic enhancement on PWM2 output.

<3> = 1 enables acoustic enhancement on PWM3 output.

Effect of Ramp Rate on Enhanced Acoustics Mode

The PWM signal driving the fan has a period, T, given by the PWM drive frequency, f, because T = 1/f. For a given PWM period, T, the PWM period is subdivided into 255 equal time slots. One time slot corresponds to the smallest possible increment in the PWM duty cycle. A PWM signal of 33% duty cycle is, therefore, high for $1/3 \times 255$ time slots and low for $2/3 \times 255$ time slots. Therefore, a 33% PWM duty cycle corresponds to a signal that is high for 85 time slots and low for 170 time slots.



Figure 81. 33% PWM Duty Cycle, Represented in Time Slots

The ramp rates in the enhanced acoustics mode are selectable from the values 1, 2, 3, 5, 8, 12, 24, and 48. The ramp rates are discrete time slots. For example, if the ramp rate is 8, eight time slots are added or subtracted to increase or decrease, respectively, the PWM high duty cycle. Figure 82 shows how the enhanced acoustics mode algorithm operates.



Figure 82. Enhanced Acoustics Algorithm

The enhanced acoustics mode algorithm calculates a new PWM duty cycle based on the temperature measured. If the new PWM duty cycle value is greater than the previous PWM value, the previous PWM duty cycle value is incremented by 1, 2, 3, 5, 8, 12, 24, or 48 time slots, depending on the settings of the enhanced acoustics registers. If the new PWM duty cycle value is less than the previous PWM value, the previous PWM duty cycle is decremented by 1, 2, 3, 5, 8, 12, 24, or 48 time slots. Each time the PWM duty cycle is incremented or decremented, its value is stored as the previous PWM duty cycle for the next comparison. A ramp rate of 1 corresponds to one time slot, which is 1/255 of the PWM period. In enhanced acoustics mode, incrementing or decrementing by 1 changes the PWM output by $1/255 \times 100\%$.

Table 42. ADT7467 REGISTERS (continued)										
									De-	Lock-
Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	fault	able

Table 43. VOLTAGE READING REGISTERS (POWER-ON DEFAULT = 0X00) (Note 1)

Register Address	R/W	Description
0x21	Read Only	Reflects the Voltage Measurement (Note 2) at the V _{CCP} Input on Pin 14 (8 MSBs of Reading)
0x22	Read Only	Reflects the Voltage Measurement (Note 3) at the V_{CC} Input on Pin 3 (8 MSBs of Reading)

1. If the extended resolution bits of these readings are also being read, the extended resolution registers (0x76, 0x77) must be read first. Once the extended resolution registers have been read, the associated MSB reading registers are frozen until read. Both the extended resolution registers and the MSB registers are frozen.

2. If V_{CCP}LO (Bit 1 of the Dynamic T_{MIN} Control Register 1, 0x36) is set, V_{CCP} can control the sleep state of the ADT7467.

3. V_{CC} (Pin 3) is the supply voltage for the ADT7467.

Table 44. TEMPERATURE READING REGISTERS (POWER-ON DEFAULT = 0X01) (Notes 1, 2)

Register Address	R/W	Description
0x25	Read Only	Remote 1 Temperature Reading (Notes 3, 4) (8 MSBs of Reading)
0x26	Read Only	Local Temperature Reading (8 MSBs of Reading)
0x27	Read Only	Remote 2 Temperature Reading (8 MSBs of Reading)

1. These temperature readings can be in twos complement or Offset 64 format; this interpretation is determined by Bit 0 of Configuration Register 5 (0x7C).

 If the extended resolution bits of these readings are also being read, the extended resolution registers (0x76, 0x77) must be read first. Once the extended resolution registers have been read, all associated MSB reading registers are frozen until read. Both the extended resolution registers and the MSB registers are frozen.

3. In twos complement mode, a temperature reading of -128°C (0x80) indicates a diode fault (open or short) on that channel.

4. In Offset 64 mode, a temperature reading of -64°C (0x00) indicates a diode fault (open or short) on that channel.

Table 45. FAN TACHOMETER READING REGISTERS (POWER-ON DEFAULT = 0X00) (Note 1)

Register Address	R/W	Description
0x28	Read Only	TACH1 Low Byte
0x29	Read Only	TACH1 High Byte
0x2A	Read Only	TACH2 Low Byte
0x2B	Read Only	TACH2 High Byte
0x2C	Read Only	TACH3 Low Byte
0x2D	Read Only	TACH3 High Byte
0x2E	Read Only	TACH4 Low Byte
0x2F	Read Only	TACH4 High Byte

I. These registers count the number of 11.11 µs periods (based on an internal 90 kHz clock) that occur between a number of consecutive fan TACH pulses (default = 2). The number of TACH pulses used to count can be changed using the TACH pulses per revolution register (0x7B). This allows the fan speed to be accurately measured. Because a valid fan tachometer reading requires that two bytes are read, the low byte must be read first. Both the low and high bytes are then frozen until read. At power-on, these registers contain 0x0000 until the first valid fan TACH measurement is read into these registers. This prevents false interrupts from occurring while the fans are spinning up. A count of 0xFFFF indicates that a fan is one of the following:

• Stalled or blocked (object jamming the fan).

• Failed (internal circuitry destroyed).

• Not populated. (The ADT7467 expects to see a fan connected to each TACH. If a fan is not connected to a TACH, the minimum high and low bytes of that TACH should be set to 0xFFFF.)

- Alternate function (for example, TACH4 reconfigured as THERM pin).
- 2-wire instead of 3-wire fan.

Table 46. CURRENT PWM DUTY CYCLE REGISTERS (POWER-ON DEFAULT = 0X00) (Note 1)

Register Address	R/W	Description
0x30	Read/Write	PWM1 Current Duty Cycle (0% to 100% Duty Cycle = 0x00 to 0xFF)
0x31	Read/Write	PWM2 Current Duty Cycle (0% to 100% Duty Cycle = 0x00 to 0xFF)
0x32	Read/Write	PWM3 Current Duty Cycle (0% to 100% Duty Cycle = 0x00 to 0xFF)

1. These registers reflect the PWM duty cycle driving each fan at any given time. When in automatic fan speed control mode, the ADT7467 reports the PWM duty cycles through these registers. The PWM duty cycle values vary according to the temperature in automatic fan speed control mode. During fan startup, these registers report 0x00. In software mode, the PWM duty cycle outputs can be set to any duty cycle value by writing to these registers.

Table 47. OPERATING POINT REGISTERS (POWER-ON DEFAULT = $0XA4$) (Notes 1, 2, 3)	Table 47.	OPERATING POINT	REGISTERS	POWER-ON DEFAULT	= 0XA4) (Notes 1, 2, 3)
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Register Address	R/W	Description
0x33	Read/Write	Remote 1 Operating Point Register (Default = 100°C)
0x34	Read/Write	Local Temperature Operating Point Register (Default = 100°C)
0x35	Read/Write	Remote 2 Operating Point Register (Default = 100°C)

Table 49. REGISTER 0X37 – DYNAMIC T_{MIN} CONTROL REGISTER 2 (POWER-ON DEFAULT = 0X00) (Note 1)

Bit	Name	R/W		Description				
<2:0>	CYR1	Read/Write	3-bit Rei monitori channel respons	bit Remote 1 cycle value. These three bits define the delay time, in terms of the number of ionitoring cycles, for making subsequent T_{MIN} adjustments in the control loop for the Remote 1 nannel. The system is associated with thermal time constants that must be found to optimize the asponse of the fans and the control loop.				
			Bits	Decrease (Short) Cycle	Increase (Long) Cycle			
			000 001 010	8 cycles (1 sec) 16 cycles (2 sec) 32 cycles (4 sec)	16 cycles (2 sec) 32 cycles (4 sec) 64 cycles (8 sec)			

Table 51. REGISTER 0X40 - CONFIGURATION REGISTER 1 (POWER-ON DEFAULT = 0X01) (Note 1)

Bit	Name	R/W	Description
<0>	STRT	Read/Write	Logic 1 enables monitoring and PWM control outputs based on the limit settings programmed. Logic 0 disables monitoring and PWM control based on the default power-up limit settings. Note that the limit values programmed are preserved even if a Logic 0 is written to this bit and the default settings are enabled. This bit becomes a read-only bit and cannot be changed once Bit 1 (LOCK bit) has been written. All limit registers should be programmed by BIOS before setting this bit to 1. (Lockable)
<1>	LOCK	Write Once	Logic 1 locks all limit values to their current settings. Once this bit is set, all lockable registers become read-only registers and cannot be modified until the ADT7467 is powered down and powered up again. This prevents rogue programs such as viruses from modifying critical system limit settings. (Lockable)
<2>	RDY	Read Only	This bit is only set to 1 by the ADT7467 to indicate that the device is fully powered up and ready to begin system monitoring.
<3>	FSPD	Read/Write	When set to 1, this bit runs all fans at full speed. Power-on default = 0. This bit cannot be locked at any time.
<4>	VxI	Read/Write	BIOS should set this bit to a 1 when the ADT7467 is configured to measure current from an ADI ADOPT VRM controller and to measure the CPU's core voltage. This bit allows monitoring software to display the watts used by the CPU. (Lockable)
<5>	FSPDIS	Read/Write	

Table 53. REGISTER 0X42 - INTERRUPT STATUS REGISTER 2 (POWER-ON DEFAULT = 0X00)

Bit	Name	R/W	Description
<1>	OVT	Read Only	OVT = 1 indicates that one of the THERM overtemperature limits has been exceeded. This bit is cleared upon a read of the status register when the temperature drops below THERM – T_{HYST} .
<2>	FAN1	Read Only	FAN1 = 1 indicates that Fan 1 has dropped below minimum speed or has stalled. This bit is not set when the PWM1 output is off.
<3>			

Table 56. FAN TACHOMETER LIMIT REGISTERS (Note 1)

Register Address	R/W	Description	Power-On Default
0x54	Read/Write	TACH1 Minimum Low Byte	0xFF
0x55	Read/Write	TACH1 Minimum High Byte/Single-channel ADC Channel Select	0xFF
0x56	Read/Write	TACH2 Minimum Low Byte	0xFF
0x57	Read/Write	TACH2 Minimum High Byte	0xFF
0x58	Read/Write	TACH3 Minimum Low Byte	0xFF
0x59	Read/Write	TACH3 Minimum High Byte	0xFF
0x5A	Read/Write	TACH4 Minimum Low Byte	0xFF
0x5B	Read/Write	TACH4 Minimum High Byte	0xFF

1. Exceeding any TACH limit register by 1 indicates that the fan is running too slowly or has stalled. The appropriate status bit is set in Interrupt Status Register 2 to indicate the fan failure. Setting the Configuration Register 1 LOCK bit has no effect on these registers.

Table 57. REGISTER 0X55 - TACH 1 MINIMUM HIGH BYTE (POWER-ON DEFAULT = 0XFF)

Bit	Name	R/W	Description
<4:0>	Reserved	Read Only	These bits are reserved when Bit 6 of Configuration 2 Register (0x73) is set (single-channel ADC mode). Otherwise, these bits represent Bits <4:0> of the TACH1 minimum high byte.
<7:5>	SCADC	Read/Write	When Bit 6 of Configuration 2 Register (0x73) is set (single-channel ADC mode), these bits are used to select the only channel from which the ADC makes measurements. Otherwise, these bits represent Bits <7:5> of the TACH1 minimum high byte.

Table 58. PWM CONFIGURATION REGISTERS

Register Address	R/W (Note 1)	Description	Power-On Default
0x5C	Read/Write	PWM1 Configuration	0x82
0x5D	Read/Write	PWM2 Configuration	0x82
0x5E	Read/Write	PWM3 Configuration	0x82

1. These registers become read-only registers when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 59. REGISTER 0X5C, REGISTER 0X5D, AND REGISTER 0X5E – PWM1, PWM2, AND PWM3 CONFIGURATION REGISTERS (POWER-ON DEFAULT = 0X82)

Bit	Name	R/W (Note 1)	Description
<2:0>	SPIN	Read/Write	These bits control the start-up timeout for PWMx. The PWM output stays high until two valid TACH rising edges are seen from the fan. If there is not a valid TACH signal during the fan TACH measurement immediately after the fan start-up timeout period, the TACH measurement

Table 61. REGISTER 0X5F, REGISTER 0X60, AND REGISTER 0X61 – REMOTE 1, LOCAL, AND REMOTE 2 T_{RANGE} /PWMX FREQUENCY REGISTERS (POWER-ON DEFAULT = 0XC4)

Bit Name R/W (Note 1)

Table 62. REGISTER 0X62 – ENHANCED ACOUSTICS REGISTER 1 (POWER-ON DEFAULT = 0X00)

Bit	Name	R/W (Note 1)		Description	
<2:0>	ACOU	Read/Write	These bits select the ramp rate applied to the PWM1 output. Instead of PWM1 jumping instant- aneously to its newly calculated speed, PWM1 ramps gracefully at the rate determined by these bits. This feature enhances the acoustics of the fan being driven by the PWM1 output.		
			Time Slot Increase	Time for 33% to 100%	
			000 = 1 001 = 2 010 = 3 011 = 5 100 = 8 101 = 12 110 = 24 111 = 48	35 sec 17.6 sec 11.8 sec 7 sec 4.4 sec 3 sec 1.6 sec 0.8 sec	
<3>	EN1	Read/Write	When this bit is 1, acous	tic enhancement is enabled on PWM1 output.	

<4>

Bit	Name	R/W (Note 1)	Description
<2:0>	ACOU3	Read/Write	These bits select the ramp rate applied to the PWM3 output. Instead of PWM3 jumping instant-
	I		

Table 67. THERM TEMPERATURE LIMIT REGISTERS (Note 1)

Register Address	R/W (Note 2)	Description	Power-On Default
0x6A	Read/Write	Remote 1 THERM Temperature Limit	0xA4 (100°C)
0x6B	Read/Write	Local THERM Temperature Limit	0xA4 (100°C)
0x6C	Read/Write	Remote 2 THERM Temperature Limit	0xA4 (100°C)

 If any temperature measured exceeds its THERM limit, all PWM outputs drive their fans at 100% duty cycle. This is a fail-safe mechanism incorporated to cool the system in the event of a critical overtemperature. It also ensures some level of cooling in the event that software or hardware locks up. If set to 0x80, this feature is disabled. The PWM output remains at 100% until the temperature drops below THERM limit – hysteresis. If the THERM pin is programmed as an output, exceeding these limits by 0.25°C can cause the THERM pin to assert low as an output.

2. These registers become read-only registers when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 68. TEMPERATURE/T_{MIN} HYSTERESIS REGISTERS (Note 1)

Register Address	R/W (Note 2)	Description	Power-On Default
0x6D	Read/Write	Remote 1 and Local Temperature Hysteresis	0x44
0x6E	Read/Write	Remote 2 Temperature Hysteresis	0x40

1. Each 4-bit value controls the amount of temperature hysteresis applied to a particular temperature channel. Once the temperature for that channel falls below its T_{MIN} value, the fan remains running at PWM_{MIN} duty cycle until the temperature = T_{MIN} – hysteresis. Up to 15°C of hysteresis can be assigned to any temperature channel. The hysteresis value chosen also applies to that temperature channel if its THERM limit is exceeded. If the THERM limit is exceeded, the PWM output being controlled goes to 100% and remains at 100% until the temperature drops below THERM – hysteresis. For acoustic reasons, it is recommended that the hysteresis value not be programmed to less than 4°C. Setting the hysteresis value lower than 4°C causes the fan to switch on and off regularly when the temperature is close to T_{MIN} .

 These registers become read-only registers when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 69. REGISTER 0X6D - REMOTE 1 AND LOCAL TEMPERATURE HYSTERESIS

Bit	Name	R/W (Note 1)	Description
<3:0>	HYSL	Read/Write	Local temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the local temperature AFC and dynamic T_{MIN} control loops.
<7:4>	HYSR1	Read/Write	Remote 1 temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the Remote 1 temperature AFC and dynamic T_{MIN} control loops.

1. This register becomes a read-only register when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

Table 70. REGISTER 0X6E – REMOTE 2 TEMPERATURE HYSTERESIS

Bit	Name	R/W (Note 1)	Description
<7:4>	HYSR2	Read/Write	Local temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the local temperature AFC and dynamic T_{MIN} control loops.

1. This register becomes a read-only register when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

Table 71. REGISTER 0X6F - XNOR TREE TEST ENABLE (POWER-ON DEFAULT = 0X00)

Bit	Name	R/W (Note 1)	Description
<0>	XEN	Read/Write	If the XEN bit is set to 1, the device enters the XNOR tree test mode. Clearing the bit removes the device from the XNOR tree test mode.
<7:1>	Reserved	Read Only	Unused. Do not write to these bits.

1. This register becomes a read-only register when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

Table 72. REGISTER 0X70 -

Bit	Name	R/W	Description	
<1>	V _{CCP}	Read/Write	V_{CCP} = 1 masks SMBALERT for out-of-limit conditions on the V_{CCP} channel	
<2>	V _{CC}	Read/Write	V_{CC} = 1 masks SMBALERT for out-of-limit conditions on the V_{CC} channel	

Bit	Name	R/W	Description	
<1:0>	FAN1	Read/Write	Sets the number of pulses to be counted when measuring Fan 1 speed. Can be used to determine fan pulses per revolution for an unknown fan type. Pulses Counted 00 = 1 01 = 2 (Default) 10 = 3 11 = 4	
<3:2>	FAN2	Read/Write	Sets the number of pulses to be counted when measuring Fan 2 speed. Can be used to determine fan pulses per revolution for an unknown fan type. Pulses Counted 00 = 1 01 = 2 (Default) 10 = 3 11 = 4	
<5:4>	FAN3	Read/Write	Sets the number of pulses to be counted when measuring Fan 3 speed. Can be used to determine fan pulses per revolution for an unknown fan type. Pulses Counted 00 = 1 01 = 2 (Default) 10 = 3 11 = 4	
<7:6>	FAN4	Read/Write	Sets the number of pulses to be counted when measuring Fan 4 speed. Can be used to determine fan pulses per revolution for an unknown fan type. Pulses Counted 00 = 1 01 = 2 (Default) 10 = 3 11 = 4	

Table 83. REGISTER 0X7B - TACH PULSES PER REVOLUTION REGISTER (POWER-ON DEFAULT = 0X55)

Table 84. REGISTER 0X7C - CONFIGURATION REGISTER 5 (POWER-ON DEFAULT = 0X00)

Bit	Name	R/W (Note 1)	Description
<0>	Twos		

Table 85. REGISTER 0X7D - CONFIGURATION REGISTER 4 (POWER-ON DEFAULT = 0X00)

Bit	Name	R/W (Note 1)	Description	
<1:0>	Pin 9 Func	Read/Write	These bits set the functionality of Pin 9. 00 = TACH4 (default) 01 = bidirectional THERM 10 = SMBALERT 11 = GPIO	
<3:2>	AINL	Read/Write	These two bits define the input threshold for 2-wire fan speed measurements (low frequency mode only). $00 = \pm 20 \text{ Mv}$ $01 = \pm 40 \text{ mV}$ $10 = \pm 80 \text{ mV}$ $11 = \pm 130 \text{ mV}$	
<4>	RES		Unused	
<5>	BpAtt V _{CCP}		Bypass V _{CCP} attenuator. When set, the measurement scale for this channel changes from 0 V (0x00) to 2.2965 V (0xFF).	
<6:7>	RES		Unused	

1. This register becomes a read-only register when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

Table 86. REGISTER 0X7E - MANUFACTURER'S TEST REGISTER 1 (POWER-ON DEFAULT = 0X00)

Bit	Name	R/W	Description	
<7:0>	Reserved	Read Only	Manufacturer's test register. These bits are reserved for the manufacturer's testing purposes and should not be written to under normal operation.	

Table 87. REGISTER 0X7F - MANUFACTURER'S TEST REGISTER 2 (POWER-ON DEFAULT = 0X00)

Bit	Name	R/W	Description	
<7:0>	Reserved	Read Only	Manufacturer's test register. These bits are reserved for the manufacturer's testing purposes and should not be written to under normal operation.	

Table 88. ORDERING INFORMATION

Device Number*	Temperature Range	Package Description	Package Option	Shipping [†]
ADT7467ARQZ-REEL	-40°C to +120°C	16-lead QSOP	RQ-16	2,500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. *The "Z" suffix indicates RoHS Compliant part.



Figure 83. Block Diagram

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DATE 23 MAR 2011



DETÁIL A

SCALE 2:1

 INCHE

 DIM
 MIN
 MA

 A
 0.053
 0.069

 A1
 0.004
 0.010

	0.025	BSC	
	0.009	0.020	
L	0.016	0.050	
м	0	8	
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