



Table 3. PIN ASSIGNMENT

Pin No.	Mnemonic	Description
1	SCL	Digital Input (Open Drain). SMBus serial clock input. Requires SMBus pullup.
2	GND	Ground Pin.
3	V _{CC}	Power Supply. V_{CC} is also monitored through this pin.
4	TACH3	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 3.
5	PWM2 SMBALERT	PWM2: Digital Output (Open Drain). Requires 10 kΩ typical pullup. Pulse-width modulated output to control Fan 2 speed. Can be configured as a high or low frequency drive. SMBALERT: Digital Output (Open Drain). This pin can be reconfigured as an SMBALERT interrupt output to signal out-of-limit conditions.
6	TACH1	Digital Input (Open Drain). Fan tachometer input to measure the speed of Fan 1.
7	TACH2	Digital Input (Open Drain). Fan tachometer input to measure the speed of Fan 2.
8	PWM3	Digital I/O (Open Drain). Pulse-width modulated output to control the speed of Fan 3 and Fan 4. Requires 10 k Ω typical pullup. Can be configured as a high or low frequency drive.
9	TACH4 THERM GPIO SMBALERT	 TACH4: Digital Input (Open Drain). Fan tachometer input to measure the speed of Fan 4. THERM: Digital I/O (Open Drain). Alternatively, this pin can be reconfigured as a bidirectional THERM pin that can be used to time and monitor assertions on the THERM input. For example, the pin can be connected to the PROCHOT output of an Intel Pentium 4 processor or to the output of a trip point temperature sensor. This pin can be used as an output to signal overtemperature conditions. GPIO: General-Purpose Open Drain Digital I/O. SMBALERT: Digital Output (Open Drain). This pin can be reconfigured as an SMBALERT interrupt output to signal out-of-limit conditions.
10	D2-	Cathode Connection to Second Thermal Diode.
11	D2+	Anode Connection to Second Thermal Diode.
12	D1–	Cathode Connection to First Thermal Diode.
13	D1+	Anode Connection to First Thermal Diode.
14	VCCP	Analog Input. Monitors processor core voltage (0 V to 3.0 V).
15	PWM1 XTO	Digital Output (Open Drain). Pulse-width modulated output to control Fan 1 speed. Requires 10 k Ω typical pullup. Also functions as the output from the XNOR tree in XNOR test mode.
	×10	Also functions as the output from the ANOR tree in ANOR test mode.

Table 4. ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX} , $V_{CC} = V_{MIN}$ to V_{MAX} , unless otherwise noted.) (Note 1)

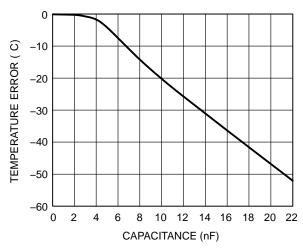
Parameter	Conditions	Min	Тур	Max	Unit
Power Supply					
Supply Voltage		3.0	3.3	3.6	

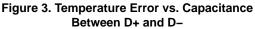
Table 4. ELECTRICAL CHARACTERISTICS (T _A = T _{MIN} to T _{MAX} , V _{CC} = V _{MIN} to V _{MAX} , unless otherwise noted	.) (Note 1)
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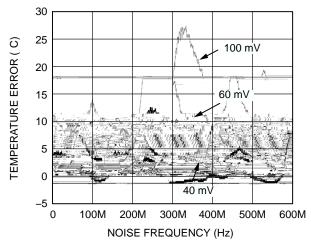
Parameter

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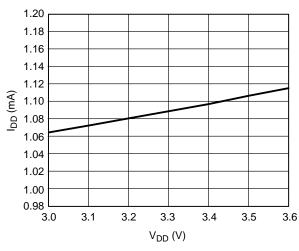
TYPICAL PERFORMANCE CHARACTERISTICS













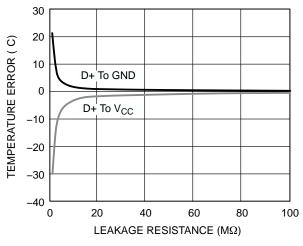


Figure 4. Remote Temperature Error vs. PCB Resistance

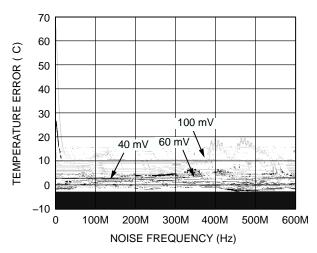
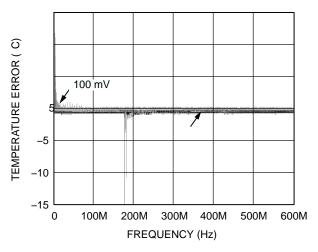
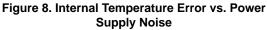


Figure 6. Remote Temperature Error vs. Differential-Mode Noise Frequency





PRODUCT DESCRIPTION

The ADT7475 is a complete thermal monitor and multiple fan controller for any system requiring thermal monitoring and cooling. The device communicates with the system via a serial system management bus. The serial bus controller has a serial data line for reading and writing addresses and data (Pin 16), and an input line for the serial clock (Pin 1). All control and programming functions for the ADT7475 are performed over the serial bus. In addition, a pin can be reconfigured as an SMBALERT output to signal out-of-limit conditions.

Quick Comparison Between ADT7473 and ADT7475

The ADT7473 supports advanced dynamic $T_{\rm MIN}$ features while the ADT7475 does not.

Acoustic smoothing is improved on the ADT7475.

THERM can be selected as an output only on the ADT7475.

The ADT7475 has two additional configuration registers.

The ADT7475 has other minor register changes.

The ADT7475 is similar to the ADT7473 in that it is powered by a supply no greater than 3.6 V. Exceeding this

specification results in irreversible damage to the ADT7475. Signal pins (TACH/PWM) should be pulled up or clamped to 3.6 V maximum. See the Specifications Section for more information.

Recommended Implementation

Configuring the ADT7475 as shown in Figure 12 allows the system designer to use the following features:

Two PWM outputs for fan control of up-to-three fans (the front and rear chassis fans are connected in parallel).

Three TACH fan speed measurement inputs

V_{CC} measured internally through Pin 3.

CPU temperature measured using the Remote 1 temperature channel.

Ambient temperature measured through the Remote 2

the tenth clock pulse, and then high during the tenth clock pulse to assert a stop condition.

It is possible to read a data byte from a data register without first writing to the address pointer register if the address pointer register is already at the correct value. However, it is not possible to write data to a register without writing to the address pointer register because the first data byte of a write is always written to the address pointer register.

In addition to supporting the send byte and receive byte protocols, the ADT7475 also supports the read byte protocol (for more information, see System Management Bus Specifications Rev. 2.0, available from Intel).

If several read or write operations must be performed in succession, the master can send a repeat start condition instead of a stop condition to begin a new operation.

M ion

master. If a device's <u>SMBALERT</u> line goes low, the following events occur:

- 1. **SMBALERT** is pulled low.
- 2. The master initiates a read operation and sends the alert response address (ARA = 0001 100). This general call address must not be used as a specific device address.
- 3. The device whose <u>SMBALERT</u> output is low responds to the alert response address, and the master reads its device address. The address of the device is now known and can be interrogated in the usual way.
- 4. If more than one device's <u>SMBALERT</u> output is low, the one with the lowest device address has priority in accordance with normal SMBus arbitration.
- 5. Once the ADT7475 has responded to the alert response address, the master must read the status registers, and the <u>SMBALERT</u> is cleared only if the error condition has gone away.

SMBus Timeout

The ADT7475 includes an SMBus timeout feature. If there is no SMBus activity for 35 ms, the ADT7475 assumes that the bus is locked and releases the bus. This prevents the device from locking or holding the SMBus expecting data. Some SMBus controllers cannot handle the SMBus timeout feature, so it can be disabled.

Table 5. CONFIGURATION REGISTER 1 (REG. 0X40)

Bit	Description
<6> TODIS	0: SMBus Timeout Enabled (Default) 1: SMBus Timeout Disabled

Virus Protection

To prevent rogue programs or viruses from accessing critical ADT7475 register settings, the lock bit can be set. Setting Bit 1 of Configuration Register 1 (0x40) sets the lock bit and locks critical registers. In this mode, certain registers can no longer be written to until the ADT7475 is powered down and powered up again. For more information on which registers are locked, see the Register Tables section.

Voltage Measurement Input

The ADT7475 has one external voltage measurement channel. It can also measure its own supply voltage, V_{CC} . Pin 14 can measure V_{CCP} . The V_{CC} supply voltage measurement is carried out through the V_{CC} pin (Pin 3). The V_{CCP} input can be used to monitor a chipset supply voltage in computer systems.

Analog-to-Digital Converter

All analog inputs are multiplexed into the on-chip, successive approximation, analog-to-digital converter. This has a resolution of 10 bits. The basic input range is 0 V to

2.25 V, but the input has built-in attenuators to allow measurement of V_{CCP} without any external components. To allow for the tolerance of the supply voltage, the ADC produces an output of 3/4 full scale (decimal 768 or 300 hex) for the nominal input voltage and so has adequate headroom to deal with overvoltages.

Input Circuitry

The internal structure for the V_{CCP} analog input is shown in Figure 19. The input circuit consists of an input protection diode, an attenuator, and a capacitor to form a first-order, low-pass filter that gives the input immunity to high frequency noise.

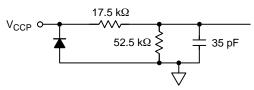


Figure 19. Structure of Analog Inputs

Table 6. VOLTAGE MEASUREMENT REGISTERS

Register	Description	Default
0x21	V _{CCP} Reading	0x00
0x22	V _{CCP} Reading	0x00

V_{CCP} Limit Registers

Associated with the V_{CCP} measurement channel is a high and low limit register. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate SMBALERT interrupts.

Table 7. V_{CCP} LIMIT REGISTERS

Register	Description	Default
0x46	V _{CCP} Low Limit	0x00
0x47		

Additional ADC Functions for Voltage Measurements

A number of other functions are available on the ADT7475 to offer the system designer increased flexibility.

Turn-off Averaging

For each voltage measurement read from a value register, 16 readings have been made internally, and the results averaged, before being placed into the value register. For instances where faster conversions are needed, setting Bit 4 of Configuration Register 2 (0x73) turns averaging off. This effectively gives a reading 16 times faster (711 μ s), but the reading may be noisier.

Bypass Voltage Input Attenuator

Setting Bit 5 of Configuration Register 2 (0x73) removes the attenuation circuitry from the V_{CCP} input. This allows the user to directly connect external sensors or to rescale the analog voltage measurement inputs for other applications. The input range of the ADC without the attenuators is 0 V to 2.25 V.

Single-Channel ADC Conversion

Setting Bit 6 of Configuration Register 2 (0x73) places the ADT7475 into single-channel ADC conversion mode. In

this mode, the ADT7475 can be made to read a single voltage channel only. If the internal ADT7475 clock is used, the selected input is read every 711 μ s. The appropriate ADC channel is selected by writing to Bits <7:5> of the TACH1 minimum high byte register (0x55).

Table 8. SINGLE-CHANNEL ADC CONVERSION

Register 0x55, Bits <7:5>	Channel Selected
001	V _{CCP}
010	V _{CC}
101	Remote 1 Temperature

TACH1 Minimum High Byte (0x55)

Bits <7:5> select the ADC channel for single-channel convert mode.

Table 10. 10-BIT ADC OUTPUT CODE VS. VIN

ADC Output			
V _{CC} (3.3 V _{IN}) (Note 1)	V _{CCP}	Decimal	Binary (10 Bits)
<0.0042	<0.00293	0	00000000 00
0.0042 to 0.0085	0.0293 to 0.0058	1	0000000 01
0.0085 to 0.0128	0.0058 to 0.0087	2	00000000 10
0.0128 to 0.0171	0.0087 to 0.0117	3	00000000 11
0.0171 to 0.0214	0.0117 to 0.0146	4	00000001 00
0.0214 to 0.0257	0.0146 to 0.0175	5	00000001 01
0.0257 to 0.0300	0.0175 to 0.0205	6	00000001 10
0.0300 to 0.0343	0.0205 to 0.0234	7	00000001 11
0.0343 to 0.0386	0.0234 to 0.0263	8	00000010 00
-	-	-	-
1.100 to 1.1042	0.7500 to 0.7529	256 (1/4 scale)	01000000 00
-	-	-	-
2.200 to 2.2042	1.5000 to 1.5029	512 (1/2 scale)	1000000 00
-	-	-	-
3.300 to 3.3042	2.2500 to 2.2529	768 (3/4 scale)	11000000 00
-	-	-	-
4.3527 to 4.3570	2.9677 to 2.9707	1013	11111101 01
4.3570 to 4.3613	2.9707 to 2.9736	1014	11111101 10

TEMPERATURE MEASUREMENT METHOD

Local Temperature Measurement

The ADT7475 contains an on-chip band gap temperature sensor whose output is digitized by the on-chip, 10-bit ADC. The 8-bit MSB temperature data is stored in the temperature registers (0x25, 0x26, and 0x27). Because both positive and negative temperatures can be measured, the temperature data is stored in Offset 64 format or twos complement format, as shown in Tables 11 and 12.

Theoretically, the temperature sensor and ADC can measure temperatures from 128 C to +127 C (or 64 C to +191 C in the extended temperature range) with a resolution of 0.25 C.

However, this exceeds the operating temperature range of the device, so local temperature measurements outside the ADT7475 operating temperature range are not possible.

Remote Temperature Measurement

The ADT7475 can measure the temperature of two remote diode sensors or diode-connected transistors connected to Pin 10 and Pin 11 or to Pin 12 and Pin 13.

The forward voltage of a diode or diode-connected transistor operated at a constant current exhibits a negative temperature coefficient of about -2 mV/ C. Because the absolute value of V_{BE} varies from device to device and individual calibration is required to null this out, the technique is unsuitable for mass production.

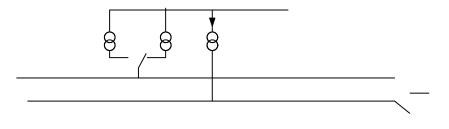


Figure 20. Signal Conditioning for Remote Diode Temperature Sensors

Noise Filtering

For temperature sensors operating in noisy environments, previous practice was to place a capacitor across the D+ pin and D pin to help combat the effects of noise. However, large capacitance's affect the accuracy of the temperature measurement, leading to a recommended maximum capacitor value of 1,000 pF.

This capacitor reduces the noise but does not eliminate it. Sometimes, this sensor noise is a problem in a very noisy environment. In most cases, a capacitor is not required because differential inputs, by their very nature, have a high immunity to noise.

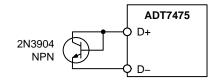


Figure 21. Measuring Temperature by Using an NPN Transistor

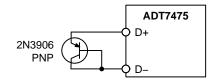


Figure 22. Measuring Temperature by Using a PNP Transistor

FACTORS AFFECTING DIODE ACCURACY

Remote Sensing Diode

The ADT7475 is designed to work with either substrate transistors built into processors or with discrete transistors. Substrate transistors are generally PNP types with the collector connected to the substrate. Discrete types can be either PNP or NPN transistors connected as a diode (base-shorted to the collector). If an NPN transistor is used, the collector and base are connected to D+ and the emitter to D . If a PNP transistor is used, the collector and base are connected to D+.

To reduce the error due to variations in both substrate and discrete transistors, a number of factors should be taken into consideration:

The ideality factor, n_f , of the transistor is a measure of the deviation of the thermal diode from ideal behavior. The ADT7475 is trimmed for an n_f value of 1.008. Use the following equation to calculate the error introduced at a temperature, T (C), when using a transistor whose n_f does not equal 1.008. See the processor data sheet for the n_f values.

$$\Delta T = (n_f - 1.008) \times (273.15 \text{ k} + T)$$
 (eq. 2)

To factor this in, the user can write the ΔT value to the offset register. The ADT7475 automatically adds it to or subtracts it from the temperature measurement. Some CPU manufacturers specify the high and low current levels of the substrate transistors. The high current level of the ADT7475, I_{HIGH}, is 180 µA and the low level current, I_{LOW}, is 11 µA. If the ADT7475 current levels do not match the current levels specified by the CPU manufacturer, it might be necessary to remove an offset. The CPU's data sheet advises whether this offset needs to be removed and how to calculate it. This offset can be programmed to the offset register. If more than one offset must be considered, the algebraic sum of these offsets must be programmed to the offset register.

If a discrete transistor is used with the ADT7475, the best accuracy is obtained by choosing devices according to the following criteria:

Base-emitter voltage greater than 0.25 V at 11 μ A, at the highest operating temperature.

Table 20. VOLTAGE LIMIT REGISTERS

Register	Description	Default
0x46	V _{CCP} Low Limit	0x00
0x47	V _{CCP} High Limit	0xFF
0x48	V _{CC} Low Limit	0x00
0x49	V _{CC} High Limit	0xFF

Table 21. TEMPERATURE LIMIT REGISTERS

Register

Interrupt Status Register 2 when this bit is set. Alternatively, Pin 5 or Pin 9 can be configured as an <u>SMBALERT</u> output. This automatically notifies the system supervisor of an out-of-limit condition. Reading the status registers clears the appropriate status bit as long as the error condition that caused the interrupt has cleared.

Status register bits are sticky. Whenever a status bit is set, indicating an out-of-limit condition, it remains set even if the event that caused it has gone away (until read). The only way to clear the status bit is to read the status register after the event has gone away. Interrupt status mask registers (0x74 and 0x75) allow individual interrupt sources to be masked from causing an <u>SMBALERT</u>. However, if one of these masked interrupt sources goes out-of-limit, its associated status bit is set in the interrupt status registers.

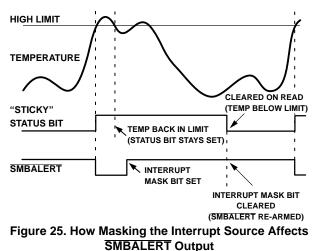
Table 24. INTERRUPT STATUS REGISTER 1 (REG. 0X41)

Bit	Mnemonic	Description
7	OOL	

Handling SMBALERT Interrupts

To prevent the system from being tied up servicing interrupts, it is recommended to handle the $\overline{\text{SMBALERT}}$ interrupt as follows:

- 1. Detect the **SMBALERT** assertion.
- 2. Enter the interrupt handler.
- 3. Read the status registers to identify the interrupt source.
- 4. Mask the interrupt source by setting the appropriate mask bit in the interrupt mask registers (0x74 and 0x75).
- 5. Take the appropriate action for a given interrupt source.
- 6. Exit the interrupt handler.
- 7. Periodically poll the status registers. If the interrupt status bit has cleared, reset the corresponding interrupt mask bit to 0. This causes the SMBALERT output and status bits to behave as shown in Figure 25.



Masking Interrupt Sources

Interrupt Mask Register 1 (0x74) and Interrupt Mask Register 2 (0x75) allow individual interrupt sources to be masked out to prevent <u>SMBALERT</u> interrupts. Note that masking an interrupt source prevents only the <u>SMBALERT</u> output from being asserted; the appropriate status bit is set normally.

Table 26. INTERRUPT MASK REGISTER 1 (REG. 0X74)

Bit	Mnemonic	Description
7	OOL	1 masks SMBALERT for any alert condition flagged in Interrupt Status Register 2.
6	R2T	1 masks SMBALERT for Remote 2 temperature.
5	LT	1 masks SMBALERT for Local temperature.
4	R1T	1 masks SMBALERT for Remote 1 temperature.
2	V _{CC}	1 masks SMBALERT for the V _{CC} channel.
0	V _{CCP}	1 masks SMBALERT for the V _{CCP} channel.

Table 27. INTERRUPT MASK REGISTER 2 (REG. 0X75)

Bit	Mnemonic	Description
7	D2	1 masks SMBALERT for Diode 2 errors.
6	D1	1 masks SMBALERT for Diode 1 errors.
5	FAN4	1 masks SMBALERT for Fan 4 failure. If the TACH4 pin is being used as the THERM input, this bit masks SMBALERT for a THERM event.
4	FAN3	1 masks SMBALERT for Fan 3.
3	FAN2	1 masks SMBALERT for Fan 2.
2	FAN1	1 masks SMBALERT for Fan 1.
1	OVT	1 masks SMBALERT for overtemperature (exceeding THERM limits).

Enabling the SMBALERT Interrupt Output

The <u>SMBALERT</u> interrupt function is disabled by default. Pin 5 or Pin 9 can be reconfigured as an <u>SMBALERT</u> output to signal out-of-limit conditions.

Table 28. CONFIGURING PIN 5 AS SMBALERT OUTPUT

Register

Assigning THERM Functionality to a Pin

Pin 9 on the ADT7475 has four possible functions: <u>SMBALERT</u>, <u>THERM</u>, GPIO, and TACH4. The user chooses the required functionality by setting Bit 0 and Bit 1

When using the $\overline{\text{THERM}}$ timer, be aware of the following. After a $\overline{\text{THERM}}$ timer read (Register 0x79), the following happens:

1. The contents of the timer are cleared on read.

If the $\overline{\text{THERM}}$ timer value exceeds the $\overline{\text{THERM}}$ timer limit value, then the F4P bit (Bit 5) of Interrupt Status

Enabling and Disabling THERM on Individual Channels

THERM can be enabled/disabled for individual or combinations of temperature channels using Bits <7:5> of Configuration Register 5 (0x7C).

THERM Hysteresis

Setting Bit 0 of Configuration Register 7 (0x11) disables THERM hysteresis.

If THERM hysteresis is enabled and THERM is disabled (Bit 2 of Configuration Register 4, 0x7D), the THERM pin does not assert low when a THERM event occurs. If THERM hysteresis is disabled and THERM is disabled (Bit 2 of Configuration Register 4, 0x7D, and assuming the appropriate pin is configured as THERM), the THERM pin asserts low when a THERM event occurs.

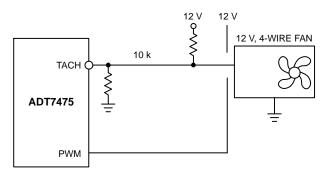


Figure 32. Driving a 4-wire Fan

input but less than 3.6 V, allowing for the voltage tolerance of the Zener. A value between 3.0 V and 3.6 V is suitable.

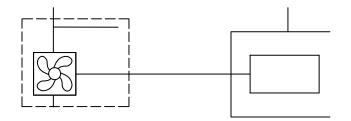


Figure 36. Fan with TACH Pullup to Voltage > 3.6 V (Example, 12 V) Clamped with Zener Diode

Reading Fan Speed from the ADT7475

The measurement of fan speeds involves a 2-register read for each measurement. The low byte should be read first. This causes the high byte to be frozen until both high and low byte registers have been read, preventing erroneous TACH readings. The fan tachometer reading registers report back the number of 11.11 μ s period clocks (90 kHz oscillator) gated to the fan speed counter, from the rising edge of the first fan TACH pulse to the rising edge of the third fan TACH pulse (assuming two pulses per revolution are being counted). Because the device is essentially measuring the fan TACH period, the higher the count value, the slower the fan is actually running. A 16-bit fan tachometer reading of 0xFFFF indicates that the fan either has stalled or is running very slowly (<100 RPM).

High Limit > Comparison Performed

Because the actual fan TACH period is being measured, falling below a fan TACH limit by 1 sets the appropriate status bit and can be used to generate an SMBALERT.

Fan TACH Limit Registers

The fan TACH limit registers are 16-bit values consisting of two bytes.

Table 32. FAN TACH LIMIT REGISTERS

Register	Description	Default
0x54	TACH1 Minimum Low Byte	0xFF
0x55	TACH1 Minimum High Byte	0xFF

Example 2:

For a PWM duty cycle of 33%, Value (decimal) = 33/0.39 = 85 (decimal) Value = 85 (decimal) or 0x54 (hex)

Table 39. PWM CURRENT DUTY CYCLE REGISTERS

Register	Description	Default
0x30	PWM1 Current Duty Cycle	0x00 (0%)
0x31	PWM2 Current Duty Cycle	0x00 (0%)
0x32	PWM3 Current Duty Cycle	0x00 (0%)

By reading the PWMx current duty cycle registers, the user can keep track of the current duty cycle on each PWM output, even when the fans are running in automatic fan speed control mode or acoustic enhancement mode. See the Programming the Automatic Fan Speed Control Loop section for details.

Operating from 3.3 V Standby

The ADT7475 has been specifically designed to operate from a 3.3 V STBY supply. In computers that support S3 and S5 states, the core voltage of the processor is lowered in these states. When monitoring THERM, the THERM timer should be disabled during these states.

Standby Mode

before the fail-safe timeout (4.6 seconds) lapses, then the

Step 1: Hardware Configuration

During system design, the motherboard sensing and

Step 2: Configuring the Mux

After the system hardware configuration is determined, the fans can be assigned to particular temperature channels. Not only can fans be assigned to individual channels but the behavior of the fans is also configurable. For example, fans can be run under automatic fan control, manually under software control, or at the fastest speed calculated by multiple temperature channels. The mux is the bridge between temperature measurement channels and the three PWM outputs.

Bits <7.5> (BHVR) of Register 0x5C, Register 0x5D, and Register 0x5E (PWM configuration registers) control the behavior of the fans connected to the PWM1, PWM2, and PWM3 outputs. The values selected for these bits determine how the mux connects a temperature measurement channel to a PWM output.

Automatic Fan Control Mux Options

Bits <7:5> (BHVR), Register 0x5C, Register 0x5D, and Register 0x5E.

- 000 = Remote 1 temperature controls PWMx
- 001 =Local temperature controls PWMx

- 010 = Remote 2 temperature controls PWMx
- 101 = Fastest speed calculated by local and Remote 2 temperature controls PWMx
- 110 = Fastest speed calculated by all three temperature channel controls PWMx

The fastest speed calculated options pertain to controlling one PWM output based on multiple temperature channels. The thermal characteristics of the three temperature zones can be set to drive a single fan. An example is the fan turning on when Remote 1 temperature exceeds 60 C or when the local temperature exceeds 45 C.

Other Mux Options

Bits <7:5> (BHVR), Register 0x5C, Register 0x5D, and Register 0x5E.

- 011 = PWMx runs full speed
- 100 = PWMx disabled (default)
- 111 = manual mode. PWMx is running under software control. In this mode, PWM current duty cycle registers (0x30 to 0x32) are writable and control the PWM outputs

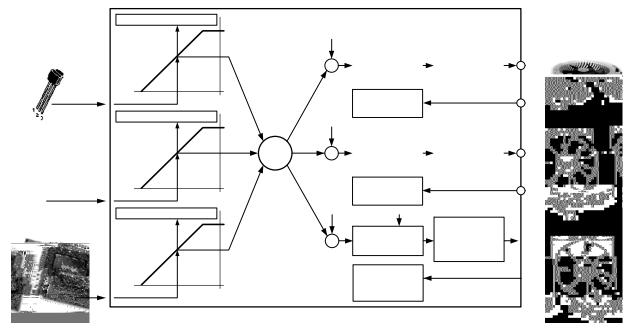


Figure 46. Assigning Temperature Channels to Fan Channels

40% duty cycle. Note that both fans turn on at exactly the same temperature, defined by $T_{\mbox{\scriptsize MIN}}.$

Programming the PWM

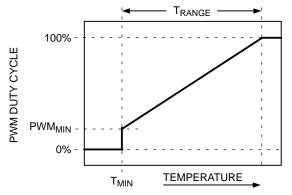


Figure 52. T_{RANGE} Parameter Affects Cooling Slope

The T_{RANGE} is determined by the following procedure:

- 1. Determine the maximum operating temperature for that channel (for example, 70 C).
- Determine, experimentally, the fan speed (PWM duty cycle value) that does not exceed the temperature at the worst-case operating points. (For example, 70 C is reached when the fans are running at 50% PWM duty cycle.)
- 3. Determine the slope of the required control loop to meet these requirements.
- 4. Using the ADT7475 evaluation software, graphically program and visualize this functionality.

As $\ensuremath{\text{PWM}_{\text{MIN}}}\xspace$ is changed, the automatic fan control slope also changes.

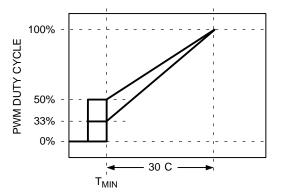


Figure 53. Adjusting PWM_{MIN} Changes the Automatic Fan Control Slope

As T_{RANGE} is changed, the slope also changes. As T_{RANGE} gets smaller, the fans reach 100% speed with a smaller temperature change.

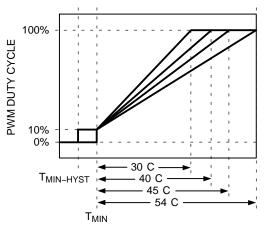


Figure 54. Increasing T_{RANGE} Changes the AFC Slope

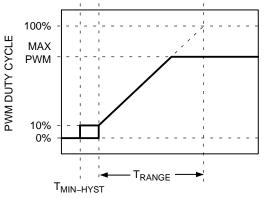


Figure 55. Changing PWM_{MAX} Does Not Change the AFC Slope

Selecting T_{RANGE}

The T_{RANGE} value can be selected for each temperature channel: Remote 1, local, and Remote 2 temperatures. Bits <7:4> (RANGE) of Register 0x5F to Register 0x61 define the T_{RANGE}

TABLE 43: BELLETING A TRANGE VALUE						
Bits <7:4> (Note 1)	T _{RANGE} (°C)					
0000	2					
0001	2.5					
0010	3.33					
0011	4					
0100	5					
0101	6.67					
0110	8					
0111	10					
1000	13.33					
1001	16					
1010	20					
1011	26.67					
1100	32 (Default)					
1101	40					
1110	53.33					
1111	80					

Table 43. SELECTING A T_{RANGE} VALUE

 Register 0x5F configures Remote 1 T_{RANGE}; Register 0x60 configures local T_{RANGE}; Register 0x61 configures Remote 2 T_{RANGE}.

Actual Changes in PWM Output (Advanced Acoustics Settings)

While the automatic fan control algorithm describes the general response of the PWM output, the enhanced acoustics registers (0x62 and 0x63) can be used to set/clamp the maximum rate of change of PWM output for a given temperature zone. This means if T_{RANGE} is programmed

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Figure 57. T_{RANGE} and % Fan Speed Slopes with PWM_{MIN} = 20%

be set up as a fail-safe, and the designer should ensure that it is not exceeded under normal system operating conditions.

Note that T_{THERM} limits are non-maskable and affect the fan speed no matter how automatic fan control settings are configured. This allows some flexibility because a T_{RANGE} value can be selected based on its slope, while a hard limit (such as 70 C) can be programmed as T_{MAX} (the temperature at which the fan reaches full speed) by setting T_{THERM} to that limit (for example, 70 C).

Table 44. THERM REGISTERS

Register	Description	Default
0x6A	Remote 1 THERM Temperature Limit	0x64 (100 C)
0x6B	Local THERM Temperature Limit	0x64 (100 C)
0x6C	Remote 2 THERM Temperature Limit	0x64 (100 C)

THERM Hysteresis

THERM hysteresis on a particular channel is configured via the hysteresis settings in Register 0x6D and Register 0x6E. For example, setting hysteresis on the Remote 1 channel also sets the hysteresis on Remote 1 THERM.

Hysteresis Registers

Step 8: T_HYST for Temperature Channels T_{HYST}

Enhanced Acoustics Register 1 (0x62)

Bit 7 (MIN3) = 0, PWM3 is off (0% PWM duty cycle) when temperature is below T_{MIN} T_{HYST}.

Bit 7 (MIN3) = 1, PWM3 runs at PWM3 minimum duty cycle below T_{MIN} T_{HYST}.

Bit 6 (MIN2) = 0, PWM2 is off (0% PWM duty cycle) when temperature is below T_{MIN} T_{HYST}.

Bit 6 (MIN2) = 1, PWM2 runs at PWM2 minimum duty cycle below T_{MIN} T_{HYST}.

Bit 5 (MIN1) = 0, PWM1 is off (0% PWM duty cycle) when temperature is below T_{MIN} T_{HYST}.

Bit 5 (MIN1) = 1, PWM1 runs at PWM1 minimum duty cycle below T_{MIN} T_{HYST} .

Configuration Register 6 (0x10)

Bit 0 (SLOW Remote 1), 1 slows the ramp rate for PWM changes associated with the Remote 1 temperature channel by 4.

Bit 1 (SLOW Local), 1 slows the ramp rate for PWM changes associated with the Local temperature channel by 4.

Bit 2 (SLOW Remote 2), 1 slows the ramp rate for PWM changes associated with the Remote 2 temperature channel by 4.

Bit 7 (ExtraSlow), 1 slows the ramp rate for all fans by a factor of 39.2%.

The following sec06 T i7 www.

Table 45. ADT7475 REGISTERS (continued)

Addr	R/W	Desc	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Defaul t	Locka ble
0x4E	R/W	Remote 1 Temp Low Limit	7	6	5	4	3	2	1	0	0x81	-
0x4F	R/W	Remote 1 Temp High Limit	7	6	5	4	3	2	1	0	0x7F	-
0x50	R/W	Local Temp Low Limit	7	6	5	4	3	2	1	0	0x81	-
0x51	R/W	Local Temp High Limit	7	6	5	4	3	2	1	0	0x7F	-
0x52	R/W	Remote 2 Temp Low Limit	7	6	5	4	3	2	1	0	0x81	-
0x53	R/W	Remote 2 Temp High Limit	7	6	5	4	3	2	1	0	0x7F	-
0x54	R/W	TACH1 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	-
0x55	R/W	TACH1 Min High Byte	15	14	13	12	11	10	9	8	0xFF	-
0x56	R/W	TACH2 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	-
0x57	R/W	TACH2 Min High Byte	15	14	13	12	11	10	9	8	0xFF	-
0x58	R/W	TACH3 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	-
0x59	R/W	TACH3 Min High Byte	15	14	13	12	11	10	9	8	0xFF	-
0x5A	R/W	TACH4 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	_
0x5B	R/W	TACH4 Min High Byte	15	14	13	12	11	10	9	8	0xFF	-
0x5C	R/W	•		•		•		•	•		•	

Table 46. REGISTER 0X10 – CONFIGURATION REGISTER 6 (POWER-ON DEFAULT = 0X00) (Notes 1 and 2)

Bit No. Mnemonic R/W

Description

Table 50. FAN TACHOMETER READING REGISTERS (POWER-ON DEFAULT = 0X00) (Note 1)

Register Address	R/W	Description
0x28	Read-only	TACH1 Low Byte
0x29	Read-only	TACH1 High Byte
0x2A	Read-only	TACH2 Low Byte
0x2B	Read-only	TACH2 High Byte
0x2C	Read-only	TACH3 Low Byte
0x2D	Read-only	TACH3 High Byte
0x2E	Read-only	TACH4 Low Byte
0x2F	Read-only	TACH4 High Byte

1. These registers count the number of 11.11 µs periods (based on an internal 90 kHz clock) that occur between a number of consecutive fan TACH pulses (default = 2). The number of TACH pulses used to count can be changed using the TACH pulses per revolution register (0x7B). This allows the fan speed to be accurately measured. Because a valid fan tachometer reading requires that two bytes be read, the low byte must be read first. Both the low and high bytes are then frozen until read. At power-on, these registers contain 0x0000 until the first valid fan TACH measurement is read into these registers. This prevents false interrupts from occurring while the fans are spinning up.

A count of 0xFFFF indicates that a fan is one of the following:

Stalled or blocked (object jamming the fan).

Failed (internal circuitry destroyed).

Not populated. (The ADT7475 expects to see a fan connected to each TACH. If a fan is not connected to that TACH, its TACH minimum high and low bytes should be set to 0xFFFF.)

Alternate function, for example, TACH4 reconfigured as a THERM pin.).

Table 51. CURRENT PWM DUTY CYCLE REGISTERS (POWER-ON DEFAULT = 0X00) (Note 1)

Register Address	R/W	Description
0x30	R/W	PWM1 Current Duty Cycle (0% to 100% Duty Cycle = 0x00 to 0xFF)
0x31	R/W	PWM2 Current Duty Cycle (0% to 100% Duty Cycle = 0x00 to 0xFF)
0x32	R/W	PWM3 Current Duty Cycle (0% to 100% Duty Cycle = 0x00 to 0xFF)

These registers reflect the PWM duty cycle driving each fan at any given time. When in automatic fan speed control mode, the ADT7475
reports the PWM duty cycles back through these registers. The PWM duty cycle values vary according to temperature in automatic fan speed
control mode. During fan startup, these registers report back 0x00. In software mode, the PWM duty cycle outputs can be set to any duty
cycle value by writing to these registers.

Table 52. MAXIMUM PWM DUTY CYCLE REGISTERS (POWER-ON DEFAULT = 0XFF)

	R/W	Description
0x38	R/W	Maximum Duty Cycle for PWM1 Output, Default = 100% (0xFF)
0x39	R/W	Maximum Duty Cycle for PWM2 Output, Default = 100% (0xFF)
0x3A	R/W	Maximum Duty Cycle for PWM3 Output, Default = 100% (0xFF)

1. This register becomes read-only when the Configuration Register 1 Lock bit is set to 1. Any subsequent attempts to write to this register fail.

2. These registers set the maximum PWM duty cycle of the PWM output.

Register Address	R/W	Description	Power-On Default
0x54	R/W	TACH1 Minimum Low Byte	0xFF
0x55	R/W	TACH1 Minimum High Byte/Single-channel ADC Channel Select	0xFF
0x56	R/W	TACH2 Minimum Low Byte	0xFF
0x57	R/W	TACH2 Minimum High Byte	0xFF
0x58	R/W	TACH3 Minimum Low Byte	0xFF
0x59	R/W	TACH3 Minimum High Byte	0xFF
0x5A	R/W	TACH4 Minimum Low Byte	0xFF
0x5B	R/W	TACH4 Minimum High Byte	0xFF

Table 58. FAN TACHOMETER LIMIT REGISTERS (Note 1)

1. Exceeding any of the TACH limit registers by 1 indicates that the fan is running too slowly or has stalled. The appropriate status bit is set in Interrupt Status Register 2 to indicate the fan failure. Setting the Configuration Register 1 Lock bit has no effect on these registers.

Table 59. REGISTER 0X55 – TACH1 MINIMUM HIGH BYTE (POWER-ON DEFAULT = 0XFF)

Bit No.	Mnemonic	R/W	Description
<4:0>	Reserved	Read-only	These bits are reserved when Bit 6 of Configuration Register 2 (0x73) is set (single-channel ADC mode). Otherwise, these bits represent Bits <4:0> of the TACH1 minimum high byte register.
<7:5>	SCADC		

Table 61. REGISTER 0X05C, REGISTER 0X5D, AND REGISTER 0X5E – PWM CONFIGURATION REGISTERS (POWER-ON DEFAULT = 0X62)

Bit No.	Mnemonic	R/W	Description
<2:0>	SPIN	R/W	These bits control the startup timeout for PWMx. The PWM output stays high until two valid TACH rising edges are seen from the fan. If there is not a valid TACH signal during the fan TACH measurement directly after the fan startup timeout period, the TACH measurement reads 0xFFFF and Interrupt Status Register 2 reflects the fan fault. If the TACH minimum high and low bytes contain 0xFFFF or 0x0000, the Interrupt Status Register 2 bit is not set, even if the fan has not started. 000 = No Startup Timeout 001 = 100 ms 010 = 250 ms (Default) 011 = 400 ms 100 = 667 ms 101 = 1 sec 111 = 4 sec
<4>	INV	R/W	This bit inverts the PWM output. The default is 0, which corresponds to a logic high output for 100% duty cycle. Setting this bit to 1 inverts the PWM output so that 100% duty cycle corresponds to a logic low output.
<7:5>	BHVR	R/W	These bits assign each fan to a particular temperature sensor for localized cooling. 000 = Remote 1 temperature controls PWMx (automatic fan control mode). 001 = Local temperature controls PWMx (automatic fan control mode). 010 = Remote 2 temperature controls PWMx (automatic fan control mode). 011 = PWMx runs full speed. 100 = PWMx disabled (default). 101 = Fastest speed calculated by local and Remote 2 temperature controls PWMx. 110 = Fastest speed calculated by all three temperature channel controls PWMx. 111 = Manual Mode. PWM duty cycle registers (0x30 to 0x32) become writable.

Table 62. TEMP T_{RANGE}/PWM FREQUENCY REGISTERS (Note 1)

Register Address	R/W	Description	Power-On Default
0x5F	R/W	Remote 1 T _{RANGE} /PWM1 Frequency	0xC4
0x60	R/W	Local T _{RANGE} /PWM2 Frequency	0xC4
0x61	R/W	Remote 2 T _{RANGE} /PWM3 Frequency	0xC4

1. These registers become read-only when the Configuration Register 1 Lock bit is set. Any subsequent attempts to write to these registers fail.

Table 63. REGISTER 0X05F, REGISTER 0X60, AND REGISTER 0X61 – TEMP T_{RANGE}/PWM FREQUENCY REGISTERS (POWER-ON DEFAULT = 0XC4)

Bit No.	Mnemonic	R/W	Description
<2:0>	FREQ	R/W	These bits control the PWMx frequency. 000 = 11.0 Hz 001 = 14.7 Hz 010 = 22.1 Hz 011 = 29.4 Hz 100 = 35.3 Hz (Default) 101 = 44.1 Hz 110 = 58.8 Hz 111 = 88.2 Hz
<3>	HF/LF	R/W	HF/LF = 1, enables high frequency PWM output for 4-wire fans. Once enabled, 3-wire fan specific settings have no effect (this means, pulse stretching).
<7:4>	RANGE	R/W	

Table 64. REGISTER 0X62 - ENHANCED ACOUSTICS REGISTER 1 (POWER-ON DEFAULT = 0X00) (Note 1)

Bit No.	Mnemonic	R/W			Description
<2:0>	ACOU1	ACOU1 R/W	maximum rate Instead of the f	of change of th an speed jump	ciated with the Remote 1 temperature channel, these bits define the ne PWMx output for Remote 1 temperature related changes. and instantaneously to its newly determined speed, it ramps ned by these bits. This feature ultimately enhances the acoustics of
			When Bit 7 of	Configuration	Register 6 (0x10) is 0
			Time Slot Incr	ease	Time for 0% to 100%
			000 = 1 001 = 2 010 = 3 011 = 4 100 = 8 101 = 12 110 = 24 111 = 48 When Bit 7 of	37.5 sec 18.8 sec 12.5 sec 7.5 sec 3.1 sec 1.6 sec 0.8 sec Configuration	Register 6 (0x10) is 1
			Time Slot Incr	-	Time for 0% to 100%
			000 = 1 001 = 2 010 = 3 0114= 4	52.2 sec 26.1 sec 17.4 sec =set0.4 sec	

Bit No.	Mnemonic	R/W	Description
<2:0>			

Table 71. XNOR TREE TEST ENABLE REGISTER (I	Note 1)
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Register Address	R/W	Bit Name	Description	Power-On Default
0x6F	R/W	XEN <0>	XNOR tree test enable register. If the XEN bit is set to 1, the device enters the XNOR tree test mode. Clearing the bit removes the device from the XNOR tree test mode.	0x00
		RES <7:1>	Unused. Do not write to these bits.	

1. These registers become read-only when the Configuration Register 1 Lock bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 72. REMOTE 1 TEMPERATURE OFFSET REGISTER (Note 1)

Register Address	R/W	Bit Name	Description	Power-On Default
0x70	R/W	<7:0>	Remote 1 temperature offset. Allows a twos complement offset value to be automatically added to or subtracted from the Remote 1 temperature reading. This is to compensate for any inherent system offsets such as PCB trace resistance. LSB value = 0.5 C.	0x00

1. These registers become read-only when the Configuration Register 1 Lock bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 73. LOCAL TEMPERATURE OFFSET REGISTER (Note 1)

Register Address	R/W	Bit Name	Description	Power-On Default
0x71	R/W	<7:0>	Local temperature offset. Allows a twos complement offset value to be automatically added to or subtracted from the local temperature reading. LSB value = 0.5 C.	0x00

1. These registers become read-only when the Configuration Register 1 Lock bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 74. REMOTE 2 TEMPERATURE OFFSET REGISTER (Note 1)

Register Address	R/W	Bit Name	Description	Power-On Default
0x72	R/W	<7:0>	Remote 2 temperature offset. Allows a twos complement offset value to be automatically added to or subtracted from the Remote 2 temperature reading. This is to compensate for any inherent system offsets such as PCB trace resistance. LSB value = 0.5 C.	0x00

1. These registers become read-only when the Configuration Register 1 Lock bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 75. REGISTER 0X73 - CONFIGURATION REGISTER 2 (POWER-ON DEFAULT = 0X00) (Note 1)

Bit No.	Mnemonic	R/W	Description	
<0:3>	RES		Reserved.	
<4>	AVG	R/W	AVG = 1, averaging on the temperature and voltage measurements is turned off. This allows measurements on each channel to be made much faster.	
<5>	ATTN	R/W	ATTN = 1, the ADT7475 removes the attenuators from the V_{CCP} input. The V_{CCP} input can be used for other functions such as connecting up external sensors.	
<6>	CONV	R/W	used for other functions such as connecting up external sensors.CONV = 1, the ADT7475 is put into a single-channel ADC conversion mode. In this mode, the ADT7475 can be made to read continuously from one input only, for example, Remote 1 temperature. The appropriate ADC channel is selected by writing to Bits <7:5> of TACH1 minimum high byte register (0x55). Register 0x55, Bits <7:5> 000Reserved 001001V _{CCP} 010010V _{CC} (3.3 V) 011011Reserved 100102Reserved 101103Remote 1 Temperature 110110Local Temperature	
<7>	SHDN	R/W	SHDN = 1, ADT7475 goes into shutdown mode. All PWM outputs assert low (or high depending on state of the INV bit) to switch off all fans. The PWM current duty cycle registers read 0x00 to indicate that the fans are not being driven.	

1. These registers become read-only when the Configuration Register 1 Lock bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 80. REGISTER 0X78 -

Table 83. REGISTER 0X7B – TACH PULSES PER REVOLUTION REGISTER (POWER-ON DEFAULT = 0X55)

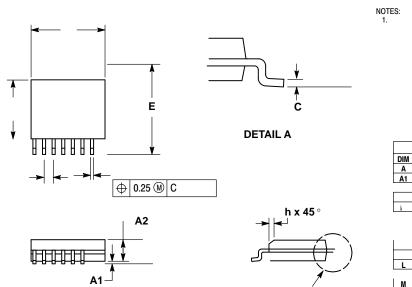
Bit No.	Mnemonic	R/W	Description
<1:0>			00 = 1 01 = 2 (Default) 10 = 3
<3:2>	FAN2	R/W	Sets the number of pulses to be counted when measuring Fan 2 speed. Can be used to determine fan pulses per revolution for an unknown fan type. Pulses Counted 00 = 1 01 = 2 (Default) 10 = 3 11 = 4
<5:4>	FAN3	R/W	Sets the number of pulses to be counted when measuring Fan 3 speed. Can be used to determine fan pulses per revolution for an unknown fan type. Pulses Counted 00 = 1 01 = 2 (Default) 10 = 3 11 = 4

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	<1:0>	PIN9FUNC	R/W	These bits set the functionality of Pin 9: 00 = TACH4 (Default) 01 = Bidirectional THERM 10 = SMBALERT 11 = GPIO
	<2>	THERM Disable	R/W	THERM Disable = 0, THERM overtemperature output is enabled assuming THERM is correctly configured (Register 0x78, Register 0x7C, and Register 0x7D). THERM Disable = 1, THERM overtemperature output is disabled on all channels. THERM can also be disabled on any channel by the following: In Offset 64 mode, writing -64 C to the appropriate THERM temperature limit. In twos complement mode, writing -128 C to the appropriate THERM temperature limit.
ſ	<3>	Max/Full on THERM	R/W	Max/Full on THERM = 0. When THERM limit is exceeded, fans go to full speed. Max/Full on THERM = 1. When THERM limit is exceeded, fans go to maximum speed as defined in Register 0x38, Register 0x39, and Register 0x3A.
	<4:7>	RES		Unused.
	<5>	BpAttV _{CCP}	R/W	Bypass V _{CCP} attenuator. When set, the measurement scale for this channel changes from 0 V (0x00) to 2.2965 V (0xFF).

QSOP16 CASE 492-01 ISSUE A

DATE 23 MAR 2011



DETÁIL A

	INC	HĔ	
DIM	MIN	MA	
Α	0.053	0.069	
A1	0.004	0.010	
	0.008	0.012	
1	0.007	0.010	

	0.025 BSC		
	0.009	0.020	
L	0.016	0.050	
Μ	0	8	

SCALE 2:1

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