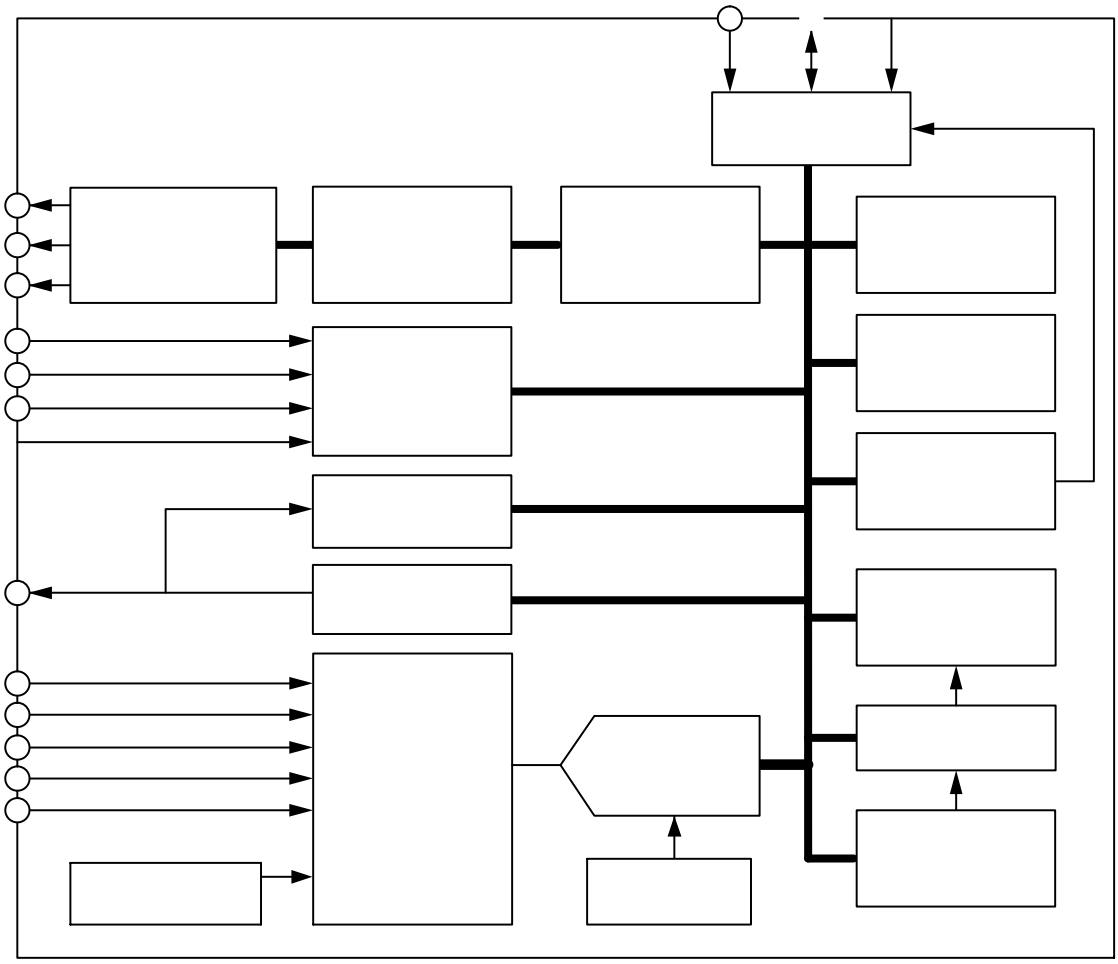


Figure 1. Functional Block Diagram

Table 3. PIN ASSIGNMENT

Pin No.	Mnemonic	Description
		Ω
		Ω
	–	
	–	
		Ω
		Ω

Table 4. ELECTRICAL CHARACTERISTICS

Parameter	Conditions	Min	Typ	Max	Unit
Power Supply					

Table 4. ELECTRICAL CHARACTERISTICS

Parameter	Max	Unit

TYPICAL PERFORMANCE CHARACTERISTICS

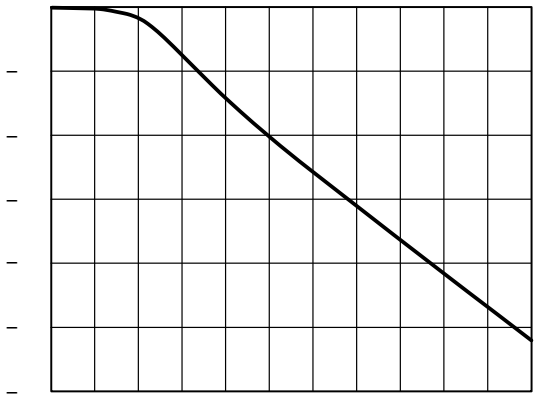


Figure 3. Temperature Error vs. Capacitance Between D+ and D−

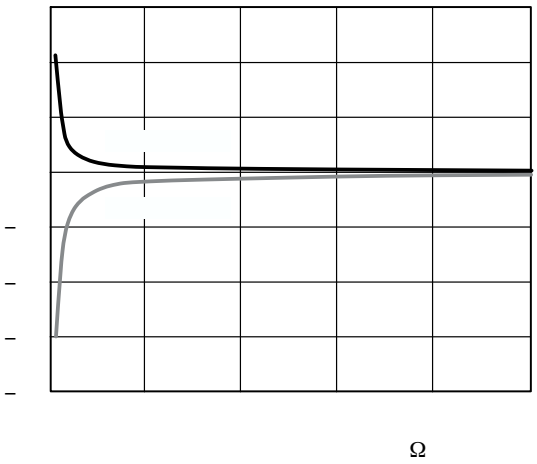


Figure 4. Remote Temperature Error vs. PCB Resistance

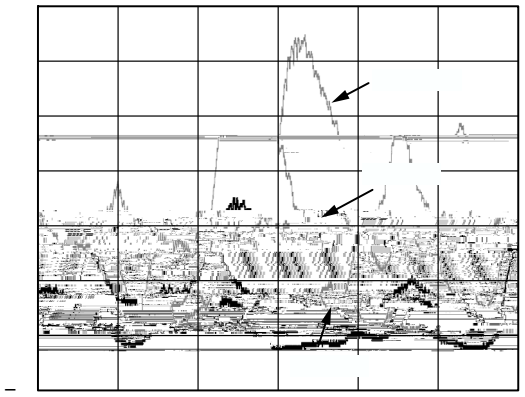


Figure 5. Remote Temperature Error vs. Common-Mode Noise Frequency

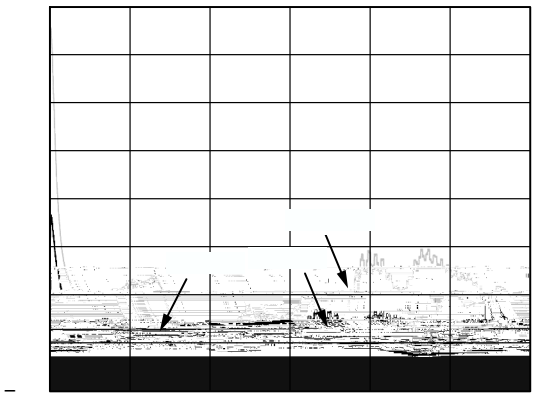


Figure 6. Remote Temperature Error vs. Differential-Mode Noise Frequency

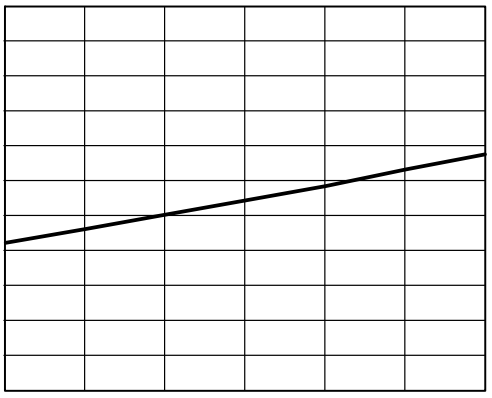


Figure 7. Normal I_{DD} vs. Power Supply

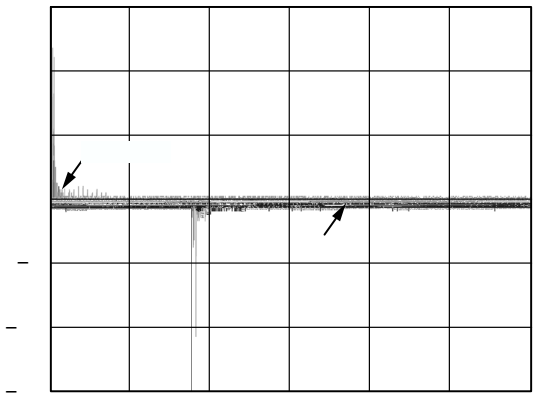


Figure 8. Internal Temperature Error vs. Power Supply Noise

PRODUCT DESCRIPTION

The ADT7475 is a complete thermal monitor and multiple fan controller for any system requiring thermal monitoring and cooling. The device communicates with the system via a serial system management bus. The serial bus controller has a serial data line for reading and writing addresses and data (Pin 16), and an input line for the serial clock (Pin 1). All control and programming functions for the ADT7475 are performed over the serial bus. In addition, a pin can be reconfigured as an $\overline{\text{SMBALERT}}$ output to signal out-of-limit conditions.

Quick Comparison Between ADT7473 and ADT7475

The ADT7473 supports advanced dynamic T_{MIN} features while the ADT7475 does not.

Acoustic smoothing is improved on the ADT7475.

$\overline{\text{THERM}}$ can be selected as an output only on the ADT7475.

The ADT7475 has two additional configuration registers.

The ADT7475 has other minor register changes.

The ADT7475 is similar to the ADT7473 in that it is powered by a supply no greater than 3.6 V. Exceeding this specification results in irreversible damage to the ADT7475. Signal pins (TACH/PWM) should be pulled up or clamped to 3.6 V maximum. See the Specifications Section for more information.

Recommended Implementation

Configuring the ADT7475 as shown in Figure 12 allows the system designer to use the following features:

Two PWM outputs for fan control of up-to-three fans (the front and rear chassis fans are connected in parallel).

Three TACH fan speed measurement inputs

V_{CC} measured internally through Pin 3.

CPU temperature measured using the Remote 1 temperature channel.

Ambient temperature measured through the Remote 2

the tenth clock pulse, and then high during the tenth clock pulse to assert a stop condition.

It is possible to read a data byte from a data register without first writing to the address pointer register if the address pointer register is already at the correct value. However, it is not possible to write data to a register without writing to the address pointer register because the first data byte of a write is always written to the address pointer register.

In addition to supporting the send byte and receive byte protocols, the ADT7475 also supports the read byte protocol (for more information, see System Management Bus Specifications Rev. 2.0, available from Intel).

If several read or write operations must be performed in succession, the master can send a repeat start condition instead of a stop condition to begin a new operation.

M ion

master. If a device's $\overline{\text{SMBALERT}}$ line goes low, the following events occur:

1. $\overline{\text{SMBALERT}}$ is pulled low.
2. The master initiates a read operation and sends the alert response address (ARA = 0001 100). This general call address must not be used as a specific device address.
3. The device whose $\overline{\text{SMBALERT}}$ output is low responds to the alert response address, and the master reads its device address. The address of the device is now known and can be interrogated in the usual way.
4. If more than one device's $\overline{\text{SMBALERT}}$ output is low, the one with the lowest device address has priority in accordance with normal SMBus arbitration.
5. Once the ADT7475 has responded to the alert response address, the master must read the status registers, and the $\overline{\text{SMBALERT}}$ is cleared only if the error condition has gone away.

SMBus Timeout

The ADT7475 includes an SMBus timeout feature. If there is no SMBus activity for 35 ms, the ADT7475 assumes that the bus is locked and releases the bus. This prevents the device from locking or holding the SMBus expecting data. Some SMBus controllers cannot handle the SMBus timeout feature, so it can be disabled.

Table 5. CONFIGURATION REGISTER 1 (REG. 0X40)

Bit	Description

Virus Protection

To prevent rogue programs or viruses from accessing critical ADT7475 register settings, the lock bit can be set. Setting Bit 1 of Configuration Register 1 (0x40) sets the lock bit and locks critical registers. In this mode, certain registers can no longer be written to until the ADT7475 is powered down and powered up again. For more information on which registers are locked, see the Register Tables section.

Voltage Measurement Input

The ADT7475 has one external voltage measurement channel. It can also measure its own supply voltage, V_{CC}. Pin 14 can measure V_{CCP}. The V_{CC} supply voltage measurement is carried out through the V_{CC} pin (Pin 3). The V_{CCP} input can be used to monitor a chipset supply voltage in computer systems.

Analog-to-Digital Converter

All analog inputs are multiplexed into the on-chip, successive approximation, analog-to-digital converter. This has a resolution of 10 bits. The basic input range is 0 V to 2.25 V, but the input has built-in attenuators to allow measurement of V_{CCP} without any external components. To allow for the tolerance of the supply voltage, the ADC produces an output of 3/4 full scale (decimal 768 or 300 hex) for the nominal input voltage and so has adequate headroom to deal with overvoltages.

Input Circuitry

The internal structure for the V_{CCP} analog input is shown in Figure 19. The input circuit consists of an input protection diode, an attenuator, and a capacitor to form a first-order, low-pass filter that gives the input immunity to high frequency noise.

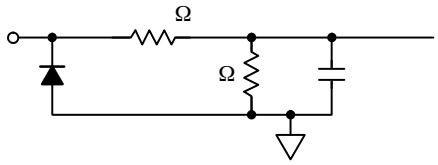


Figure 19. Structure of Analog Inputs

Table 6. VOLTAGE MEASUREMENT REGISTERS

Register	Description	Default

V_{CCP} Limit Registers

Associated with the V_{CCP} measurement channel is a high and low limit register. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate $\overline{\text{SMBALERT}}$ interrupts.

Table 7. V_{CCP} LIMIT REGISTERS

Register	Description	Default

Additional ADC Functions for Voltage Measurements

A number of other functions are available on the ADT7475 to offer the system designer increased flexibility.

Turn-off Averaging

For each voltage measurement read from a value register, 16 readings have been made internally, and the results averaged, before being placed into the value register. For instances where faster conversions are needed, setting Bit 4 of Configuration Register 2 (0x73) turns averaging off. This effectively gives a reading 16 times faster (711 μs), but the reading may be noisier.

Bypass Voltage Input Attenuator

Setting Bit 5 of Configuration Register 2 (0x73) removes the attenuation circuitry from the V_{CCP} input. This allows the user to directly connect external sensors or to rescale the analog voltage measurement inputs for other applications. The input range of the ADC without the attenuators is 0 V to 2.25 V.

Single-Channel ADC Conversion

Setting Bit 6 of Configuration Register 2 (0x73) places the ADT7475 into single-channel ADC conversion mode. In this mode, the ADT7475 can be made to read a single voltage channel only. If the internal ADT7475 clock is used, the selected input is read every 711 μs. The appropriate ADC channel is selected by writing to Bits <7:5> of the TACH1 minimum high byte register (0x55).

Table 8. SINGLE-CHANNEL ADC CONVERSION

Register 0x55, Bits <7:5>	Channel Selected

TACH1 Minimum High Byte (0x55)

Bits <7:5> select the ADC channel for single-channel convert mode.

Table 10. 10-BIT ADC OUTPUT CODE VS. V_{IN}

ADC Output			
V_{CC} (3.3 V_{IN})	V_{CCP}	Decimal	Binary (10 Bits)
–	–	–	–
–	–	–	–
–	–	–	–
–	–	–	–

TEMPERATURE MEASUREMENT METHOD

Local Temperature Measurement

The ADT7475 contains an on-chip band gap temperature sensor whose output is digitized by the on-chip, 10-bit ADC. The 8-bit MSB temperature data is stored in the temperature registers (0x25, 0x26, and 0x27). Because both positive and negative temperatures can be measured, the temperature data is stored in Offset 64 format or twos complement format, as shown in Tables 11 and 12.

Theoretically, the temperature sensor and ADC can measure temperatures from ĭ128 C to +127 C (or ĭ64 C to +191 C in the extended temperature range) with a resolution of 0.25 C.

However, this exceeds the operating temperature range of the device, so local temperature measurements outside the ADT7475 operating temperature range are not possible.

Remote Temperature Measurement

The ADT7475 can measure the temperature of two remote diode sensors or diode-connected transistors connected to Pin 10 and Pin 11 or to Pin 12 and Pin 13.

The forward voltage of a diode or diode-connected transistor operated at a constant current exhibits a negative temperature coefficient of about –2 mV/ C. Because the absolute value of V_{BE} varies from device to device and individual calibration is required to null this out, the technique is unsuitable for mass production.

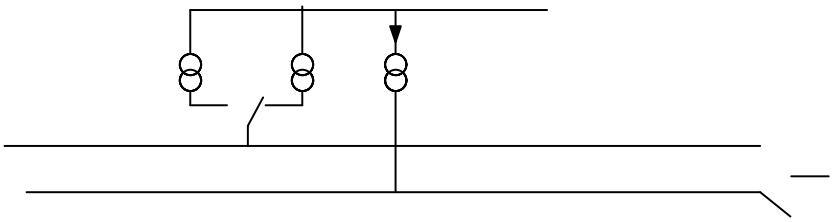


Figure 20. Signal Conditioning for Remote Diode Temperature Sensors

Noise Filtering

For temperature sensors operating in noisy environments, previous practice was to place a capacitor across the D+ pin and Dĭ pin to help combat the effects of noise. However, large capacitance's affect the accuracy of the temperature measurement, leading to a recommended maximum capacitor value of 1,000 pF.

This capacitor reduces the noise but does not eliminate it. Sometimes, this sensor noise is a problem in a very noisy environment. In most cases, a capacitor is not required because differential inputs, by their very nature, have a high immunity to noise.

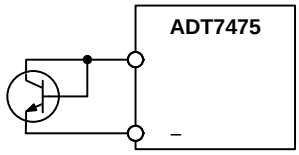


Figure 21. Measuring Temperature by Using an NPN Transistor

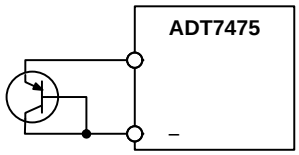


Figure 22. Measuring Temperature by Using a PNP Transistor

FACTORS AFFECTING DIODE ACCURACY

Remote Sensing Diode

The ADT7475 is designed to work with either substrate transistors built into processors or with discrete transistors. Substrate transistors are generally PNP types with the collector connected to the substrate. Discrete types can be either PNP or NPN transistors connected as a diode (base-shorted to the collector). If an NPN transistor is used, the collector and base are connected to D+ and the emitter to Dĭ. If a PNP transistor is used, the collector and base are connected to Dĭ and the emitter is connected to D+.

To reduce the error due to variations in both substrate and discrete transistors, a number of factors should be taken into consideration:

The ideality factor, n_f, of the transistor is a measure of the deviation of the thermal diode from ideal behavior. The ADT7475 is trimmed for an n_f value of 1.008. Use the following equation to calculate the error introduced at a temperature, T (C), when using a transistor whose n_f does not equal 1.008. See the processor data sheet for the n_f values.

$$\Delta = (-) \times (+)$$

To factor this in, the user can write the ΔT value to the offset register. The ADT7475 automatically adds it to or subtracts it from the temperature measurement.

Some CPU manufacturers specify the high and low current levels of the substrate transistors. The high current level of the ADT7475, I_{HIGH}, is 180 μA and the low level current, I_{LOW}, is 11 μA. If the ADT7475 current levels do not match the current levels specified by the CPU manufacturer, it might be necessary to remove an offset. The CPU's data sheet advises whether this offset needs to be removed and how to calculate it. This offset can be programmed to the offset register. If more than one offset must be considered, the algebraic sum of these offsets must be programmed to the offset register.

If a discrete transistor is used with the ADT7475, the best accuracy is obtained by choosing devices according to the following criteria:

Base-emitter voltage greater than 0.25 V at 11 μA, at the highest operating temperature.

Table 20. VOLTAGE LIMIT REGISTERS

Register	Description	Default

Table 21. TEMPERATURE LIMIT REGISTERS

Register

Interrupt Status Register 2 when this bit is set. Alternatively, Pin 5 or Pin 9 can be configured as an $\overline{\text{SMBALERT}}$ output. This automatically notifies the system supervisor of an out-of-limit condition. Reading the status registers clears the appropriate status bit as long as the error condition that caused the interrupt has cleared.

Status register bits are sticky. Whenever a status bit is set, indicating an out-of-limit condition, it remains set even if the event that caused it has gone away (until read). The only way to clear the status bit is to read the status register after the event has gone away. Interrupt status mask registers (0x74 and 0x75) allow individual interrupt sources to be masked from causing an $\overline{\text{SMBALERT}}$. However, if one of these masked interrupt sources goes out-of-limit, its associated status bit is set in the interrupt status registers.

Table 24. INTERRUPT STATUS REGISTER 1 (REG. 0X41)

Bit	Mnemonic	Description

Handling $\overline{\text{SMBALERT}}$ Interrupts

To prevent the system from being tied up servicing interrupts, it is recommended to handle the $\overline{\text{SMBALERT}}$ interrupt as follows:

1. Detect the $\overline{\text{SMBALERT}}$ assertion.
2. Enter the interrupt handler.
3. Read the status registers to identify the interrupt source.
4. Mask the interrupt source by setting the appropriate mask bit in the interrupt mask registers (0x74 and 0x75).
5. Take the appropriate action for a given interrupt source.
6. Exit the interrupt handler.
7. Periodically poll the status registers. If the interrupt status bit has cleared, reset the corresponding interrupt mask bit to 0. This causes the $\overline{\text{SMBALERT}}$ output and status bits to behave as shown in Figure 25.

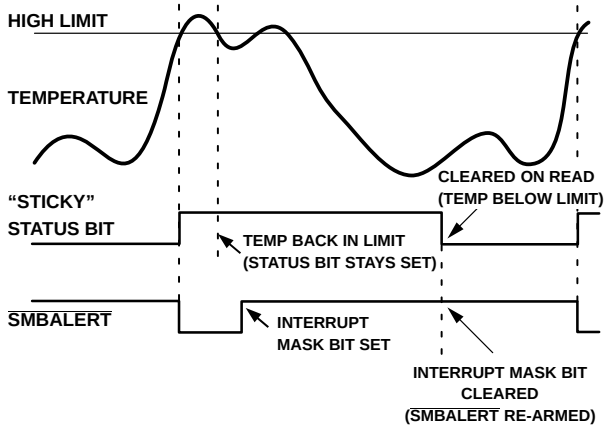


Figure 25. How Masking the Interrupt Source Affects $\overline{\text{SMBALERT}}$ Output

Masking Interrupt Sources

Interrupt Mask Register 1 (0x74) and Interrupt Mask Register 2 (0x75) allow individual interrupt sources to be masked out to prevent $\overline{\text{SMBALERT}}$ interrupts. Note that masking an interrupt source prevents only the $\overline{\text{SMBALERT}}$ output from being asserted; the appropriate status bit is set normally.

Table 26. INTERRUPT MASK REGISTER 1 (REG. 0X74)

Bit	Mnemonic	Description

Table 27. INTERRUPT MASK REGISTER 2 (REG. 0X75)

Bit	Mnemonic	Description

Enabling the $\overline{\text{SMBALERT}}$ Interrupt Output

The $\overline{\text{SMBALERT}}$ interrupt function is disabled by default. Pin 5 or Pin 9 can be reconfigured as an $\overline{\text{SMBALERT}}$ output to signal out-of-limit conditions.

Table 28. CONFIGURING PIN 5 AS $\overline{\text{SMBALERT}}$ OUTPUT

Register

Assigning $\overline{\text{THERM}}$ Functionality to a Pin

Pin 9 on the ADT7475 has four possible functions: $\overline{\text{SMBALERT}}$, $\overline{\text{THERM}}$, GPIO, and TACH4. The user chooses the required functionality by setting Bit 0 and Bit 1

When using the $\overline{\text{THERM}}$ timer, be aware of the following. After a $\overline{\text{THERM}}$ timer read (Register 0x79), the following happens:

1. The contents of the timer are cleared on read.

If the $\overline{\text{THERM}}$ timer value exceeds the $\overline{\text{THERM}}$ timer limit value, then the F4P bit (Bit 5) of Interrupt Status

Enabling and Disabling $\overline{\text{THERM}}$ on Individual Channels

$\overline{\text{THERM}}$ can be enabled/disabled for individual or combinations of temperature channels using Bits <7:5> of Configuration Register 5 (0x7C).

$\overline{\text{THERM}}$ Hysteresis

Setting Bit 0 of Configuration Register 7 (0x11) disables $\overline{\text{THERM}}$ hysteresis.

If $\overline{\text{THERM}}$ hysteresis is enabled and $\overline{\text{THERM}}$ is disabled (Bit 2 of Configuration Register 4, 0x7D), the $\overline{\text{THERM}}$ pin does not assert low when a $\overline{\text{THERM}}$ event occurs. If $\overline{\text{THERM}}$ hysteresis is disabled and $\overline{\text{THERM}}$ is disabled (Bit 2 of Configuration Register 4, 0x7D, and assuming the appropriate pin is configured as $\overline{\text{THERM}}$), the $\overline{\text{THERM}}$ pin asserts low when a $\overline{\text{THERM}}$ event occurs.

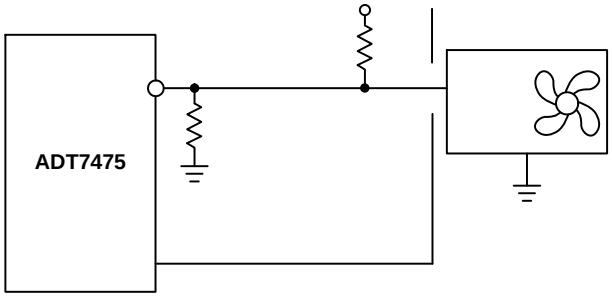


Figure 32. Driving a 4-wire Fan

input but less than 3.6 V, allowing for the voltage tolerance of the Zener. A value between 3.0 V and 3.6 V is suitable.

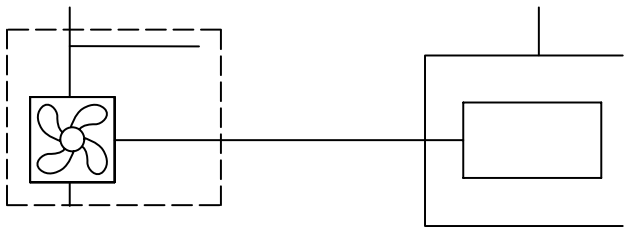


Figure 36. Fan with TACH Pullup to Voltage > 3.6 V (Example, 12 V) Clamped with Zener Diode

Reading Fan Speed from the ADT7475

The measurement of fan speeds involves a 2-register read for each measurement. The low byte should be read first. This causes the high byte to be frozen until both high and low byte registers have been read, preventing erroneous TACH readings. The fan tachometer reading registers report back the number of 11.11 μs period clocks (90 kHz oscillator) gated to the fan speed counter, from the rising edge of the first fan TACH pulse to the rising edge of the third fan TACH pulse (assuming two pulses per revolution are being counted). Because the device is essentially measuring the fan TACH period, the higher the count value, the slower the fan is actually running. A 16-bit fan tachometer reading of 0xFFFF indicates that the fan either has stalled or is running very slowly (<100 RPM).

High Limit > Comparison Performed

Because the actual fan TACH period is being measured, falling below a fan TACH limit by 1 sets the appropriate status bit and can be used to generate an $\overline{\text{SMBALERT}}$.

Fan TACH Limit Registers

The fan TACH limit registers are 16-bit values consisting of two bytes.

Table 32. FAN TACH LIMIT REGISTERS

Register	Description	Default

ADT7475

Example 2:

For a PWM duty cycle of 33%,

Value (decimal) = 33/0.39 = 85 (decimal)

Value = 85 (decimal) or 0x54 (hex)

Table 39. PWM CURRENT DUTY CYCLE REGISTERS

Register	Description	Default

By reading the PWMx current duty cycle registers, the user can keep track of the current duty cycle on each PWM output, even when the fans are running in automatic fan speed control mode or acoustic enhancement mode. See the Programming the Automatic Fan Speed Control Loop section for details.

Operating from 3.3 V Standby

The ADT7475 has been specifically designed to operate from a 3.3 V STBY supply. In computers that support S3 and S5 states, the core voltage of the processor is lowered in these states. When monitoring $\overline{\text{THERM}}$, the $\overline{\text{THERM}}$ timer should be disabled during these states.

Standby Mode

before the fail-safe timeout (4.6 seconds) lapses, then the

Step 1: Hardware Configuration

During system design, the motherboard sensing and

Step 2: Configuring the Mux

After the system hardware configuration is determined, the fans can be assigned to particular temperature channels. Not only can fans be assigned to individual channels but the behavior of the fans is also configurable. For example, fans can be run under automatic fan control, manually under software control, or at the fastest speed calculated by multiple temperature channels. The mux is the bridge between temperature measurement channels and the three PWM outputs.

Bits <7:5> (BHVR) of Register 0x5C, Register 0x5D, and Register 0x5E (PWM configuration registers) control the behavior of the fans connected to the PWM1, PWM2, and PWM3 outputs. The values selected for these bits determine how the mux connects a temperature measurement channel to a PWM output.

Automatic Fan Control Mux Options

Bits <7:5> (BHVR), Register 0x5C, Register 0x5D, and Register 0x5E.

000 = Remote 1 temperature controls PWMx
001 = Local temperature controls PWMx
010 = Remote 2 temperature controls PWMx
101 = Fastest speed calculated by local and Remote 2 temperature controls PWMx
110 = Fastest speed calculated by all three temperature channel controls PWMx

The fastest speed calculated options pertain to controlling one PWM output based on multiple temperature channels. The thermal characteristics of the three temperature zones can be set to drive a single fan. An example is the fan turning on when Remote 1 temperature exceeds 60 C or when the local temperature exceeds 45 C.

Other Mux Options

Bits <7:5> (BHVR), Register 0x5C, Register 0x5D, and Register 0x5E.

011 = PWMx runs full speed
100 = PWMx disabled (default)
111 = manual mode. PWMx is running under software control. In this mode, PWM current duty cycle registers (0x30 to 0x32) are writable and control the PWM outputs

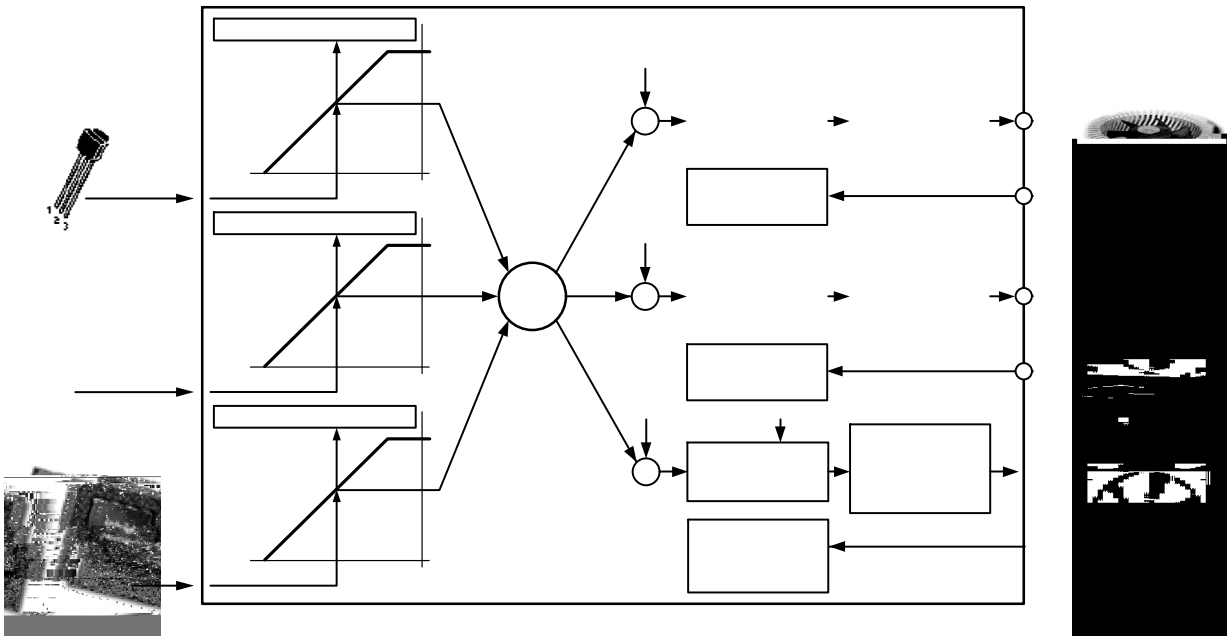


Figure 46. Assigning Temperature Channels to Fan Channels

40% duty cycle. Note that both fans turn on at exactly the same temperature, defined by T_{MIN}.

Programming the PWM

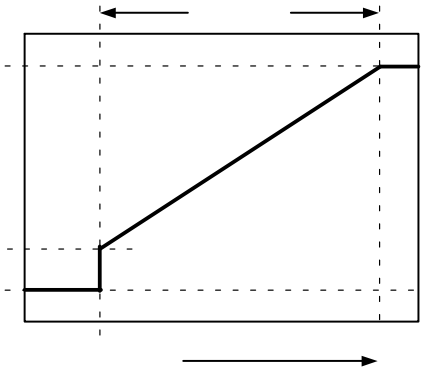


Figure 52. T_{RANGE} Parameter Affects Cooling Slope

The T_{RANGE} is determined by the following procedure:

1. Determine the maximum operating temperature for that channel (for example, 70 C).
2. Determine, experimentally, the fan speed (PWM duty cycle value) that does not exceed the temperature at the worst-case operating points. (For example, 70 C is reached when the fans are running at 50% PWM duty cycle.)
3. Determine the slope of the required control loop to meet these requirements.
4. Using the ADT7475 evaluation software, graphically program and visualize this functionality.

As PWM_{MIN} is changed, the automatic fan control slope also changes.

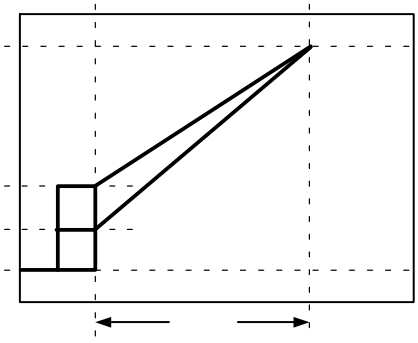


Figure 53. Adjusting PWM_{MIN} Changes the Automatic Fan Control Slope

As T_{RANGE} is changed, the slope also changes. As T_{RANGE} gets smaller, the fans reach 100% speed with a smaller temperature change.

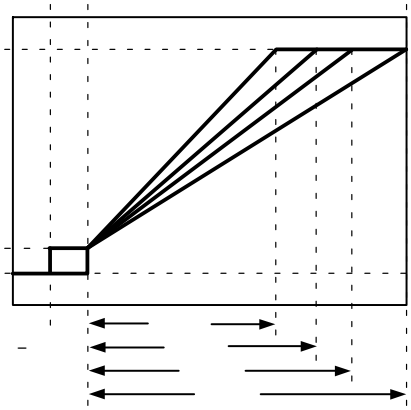


Figure 54. Increasing T_{RANGE} Changes the AFC Slope

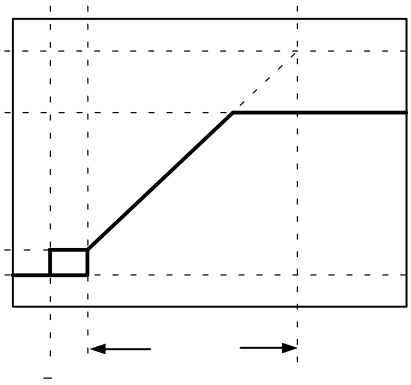


Figure 55. Changing PWM_{MAX} Does Not Change the AFC Slope

Selecting T_{RANGE}

The T_{RANGE} value can be selected for each temperature channel: Remote 1, local, and Remote 2 temperatures. Bits <7:4> (RANGE) of Register 0x5F to Register 0x61 define the T_{RANGE}

Table 43. SELECTING A T_{RANGE} VALUE

Bits <7:4>	T_{RANGE} (°C)

Actual Changes in PWM Output (Advanced Acoustics Settings)

While the automatic fan control algorithm describes the general response of the PWM output, the enhanced acoustics registers (0x62 and 0x63) can be used to set/clamp the maximum rate of change of PWM output for a given temperature zone. This means if T_{RANGE} is programmed

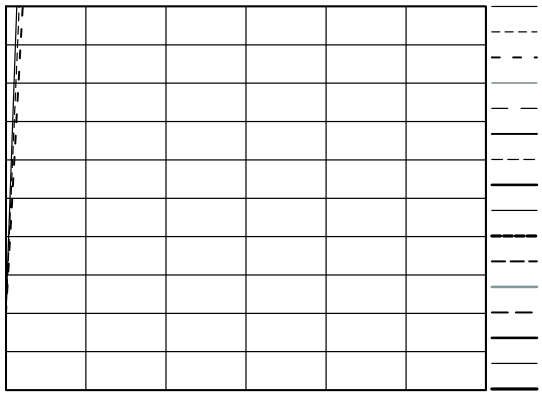


Figure 57. T_{RANGE} and % Fan Speed Slopes with PWM_{MIN} = 20%

be set up as a fail-safe, and the designer should ensure that it is not exceeded under normal system operating conditions.

Note that $T_{\overline{THERM}}$ limits are non-maskable and affect the fan speed no matter how automatic fan control settings are configured. This allows some flexibility because a T_{RANGE} value can be selected based on its slope, while a hard limit (such as 70 C) can be programmed as T_{MAX} (the temperature at which the fan reaches full speed) by setting $T_{\overline{THERM}}$ to that limit (for example, 70 C).

Table 44. $\overline{THERM}$ REGISTERS

Register	Description	Default

$\overline{THERM}$ Hysteresis

$\overline{THERM}$ hysteresis on a particular channel is configured via the hysteresis settings in Register 0x6D and Register 0x6E. For example, setting hysteresis on the Remote 1 channel also sets the hysteresis on Remote 1 $\overline{THERM}$.

Hysteresis Registers

Step 8: T_{HYST} for Temperature Channels

T_{HYST}

Enhanced Acoustics Register 1 (0x62)

Bit 7 (MIN3) = 0, PWM3 is off (0% PWM duty cycle) when temperature is below T_{MIN} ĭ T_{HYST}.

Bit 7 (MIN3) = 1, PWM3 runs at PWM3 minimum duty cycle below T_{MIN} ĭ T_{HYST}.

Bit 6 (MIN2) = 0, PWM2 is off (0% PWM duty cycle) when temperature is below T_{MIN} ĭ T_{HYST}.

Bit 6 (MIN2) = 1, PWM2 runs at PWM2 minimum duty cycle below T_{MIN} ĭ T_{HYST}.

Bit 5 (MIN1) = 0, PWM1 is off (0% PWM duty cycle) when temperature is below T_{MIN} ĭ T_{HYST}.

Bit 5 (MIN1) = 1, PWM1 runs at PWM1 minimum duty cycle below T_{MIN} ĭ T_{HYST}.

Configuration Register 6 (0x10)

Bit 0 (SLOW Remote 1), 1 slows the ramp rate for PWM changes associated with the Remote 1 temperature channel by 4.

Bit 1 (SLOW Local), 1 slows the ramp rate for PWM changes associated with the Local temperature channel by 4.

Bit 2 (SLOW Remote 2), 1 slows the ramp rate for PWM changes associated with the Remote 2 temperature channel by 4.

Bit 7 (ExtraSlow), 1 slows the ramp rate for all fans by a factor of 39.2%.

The following sec06 T i7 www.

Table 45. ADT7475 REGISTERS

Addr	R/W	Desc	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Lockable
												–
												–
												–
												–
												–
												–
												–
												–
												–
												–
												–
												–
												–
												–

Table 46. REGISTER 0X10 − CONFIGURATION REGISTER 6 (POWER-ON DEFAULT = 0X00)

Bit No.	Mnemonic	R/W	Description

Table 50. FAN TACHOMETER READING REGISTERS (POWER-ON DEFAULT = 0X00)

Register Address	R/W	Description

μ

.

Table 51. CURRENT PWM DUTY CYCLE REGISTERS (POWER-ON DEFAULT = 0X00)

Register Address	R/W	Description

Table 52. MAXIMUM PWM DUTY CYCLE REGISTERS (POWER-ON DEFAULT = 0XFF)

	R/W	Description

Table 58. FAN TACHOMETER LIMIT REGISTERS

Register Address	R/W	Description	Power-On Default

Table 59. REGISTER 0X55 − TACH1 MINIMUM HIGH BYTE (POWER-ON DEFAULT = 0XFF)

Bit No.	Mnemonic	R/W	Description

Table 61. REGISTER 0X05C, REGISTER 0X5D, AND REGISTER 0X5E − PWM CONFIGURATION REGISTERS (POWER-ON DEFAULT = 0X62)

Bit No.	Mnemonic	R/W	Description

Table 62. TEMP T_{RANGE}/PWM FREQUENCY REGISTERS

Register Address	R/W	Description	Power-On Default

Table 63. REGISTER 0X05F, REGISTER 0X60, AND REGISTER 0X61 − TEMP T_{RANGE}/PWM FREQUENCY REGISTERS (POWER-ON DEFAULT = 0XC4)

Bit No.	Mnemonic	R/W	Description

Table 64. REGISTER 0X62 − ENHANCED ACOUSTICS REGISTER 1 (POWER-ON DEFAULT = 0X00)

Bit No.	Mnemonic	R/W	Description
			When Bit 7 of Configuration Register 6 (0x10) is 0 **Time Slot Increase Time for 0% to 100%** **When Bit 7 of Configuration Register 6 (0x10) is 1** **Time Slot Increase Time for 0% to 100%**

Table 65. REGISTER 0X63 − ENHANCED ACOUSTICS REGISTER 2 (POWER-ON DEFAULT = 0X00)

Bit No.	Mnemonic	R/W	Description

Table 71. XNOR TREE TEST ENABLE REGISTER

Register Address	R/W	Bit Name	Description	Power-On Default

Table 72. REMOTE 1 TEMPERATURE OFFSET REGISTER

Register Address	R/W	Bit Name	Description	Power-On Default

Table 73. LOCAL TEMPERATURE OFFSET REGISTER

Register Address	R/W	Bit Name	Description	Power-On Default

Table 74. REMOTE 2 TEMPERATURE OFFSET REGISTER

Register Address	R/W	Bit Name	Description	Power-On Default

Table 75. REGISTER 0X73 − CONFIGURATION REGISTER 2 (POWER-ON DEFAULT = 0X00)

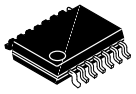
Bit No.	Mnemonic	R/W	Description
			Register 0x55, Bits <7:5>

Table 80. REGISTER 0X78 −

Table 83. REGISTER 0X7B − TACH PULSES PER REVOLUTION REGISTER (POWER-ON DEFAULT = 0X55)

Bit No.	Mnemonic	R/W	Description

Table 85. REGISTER 0X7D – CONFIGURATION REGISTER 4 (POWER-ON DEFAULT = 0X00)



SCALE 2:1

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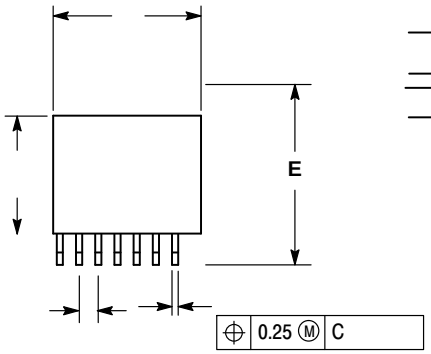
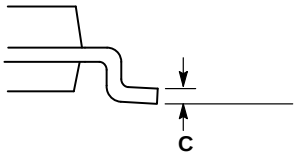
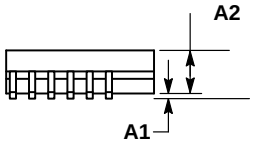
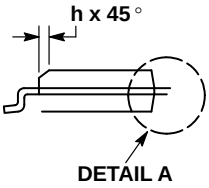




DETAIL A





DETAIL A

NOTES:

DIM	INCHES MIN	MA
A	0.053	0.069
A1	0.004	0.010
	0.008	0.012
\	0.007	0.010
	0.025 BSC	
	0.009	0.020
L	0.016	0.050
M	0	8